Advance Information

CADEKA
Amplify the Human Experience

Comlinear™ CLC1003, CLC2003, CLC4003

Low Distortion, Low Offset, RRIO Amplifiers

FEATURES

- <1mV max input offset voltage
- 0.00005% THD at 1kHz
- 3.5nV/√Hz input voltage noise >10kHz
- -90dB/-85dB HD2/HD3 at 100kHz, R_L=100Ω
- <-100dB HD2 and HD3 at 10kHz, R_L=1kΩ
- Rail-to-Rail input and output
- 70MHz unity gain bandwidth
- 13.5V/µs slew rate
- 60mA output current
- -55°C to +125°C operating temperature range
- Fully specified at 3V and ±5V supplies
- CLC1003: Lead-free SOT23-6
- Future option CLC2003: Lead-free SOIC-8
- Future option CLC4003: Lead-free TSSOP-14

APPLICATIONS

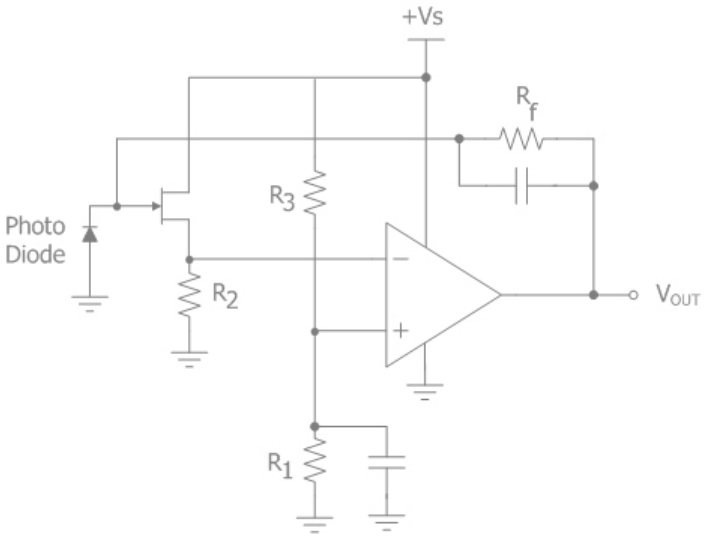
- Active filters
- Sensor interface
- High-speed transducer amp
- Medical instrumentation
- Probe equipment
- Test equipment
- Smoke detecters
- Hand-held analytic instruments

General Description

The *Comlinear* CLC1003(single), CLC2003(dual), and CLC4003 (quad) are high-performance, voltage feedback amplifiers with near precision performance, low input voltage noise, and ultra low distortion. The CLC1003 family of amplifiers offers 1mV maximum input offset voltage, 3.5nV/√Hz input voltage noise, and 0.00005% THD at 1kHz. These amplifiers also provide 70MHz gain bandwidth product and 13.5V/µs slew rate making them well suited for applications requireing precision DC performance and high AC performance. These *Comlinear* high-performance amplifiers also offer a rail-to-rail input and output, simplifying single supply designs and offering larger dynamic range possibilities. The inputs extend beyond the rails by 300mV.

The *Comlinear* CLC1003 family of amplifiers are designed to operate from 2.5V to 12V supplies. These *Comlinear* amplifiers operate over the extended temperature range of -55°C to +125°.

Typical Application - Single Supply Photodiode Amplifier



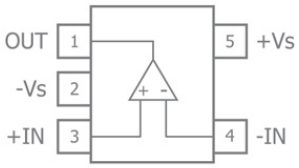
Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
CLC1003IST6X*	SOT23-5	Yes	-55°C to +125°C	Reel
CLC1003IST6*	SOT23-5	Yes	-55°C to +125°C	Rail
CLC2003ISO8X†	SOIC-8	Yes	-55°C to +125°C	Reel
CLC2003ISO8†	SOIC-8	Yes	-55°C to +125°C	Rail
CLC4003ITP14X†	TSSOP-14	Yes	-55°C to +125°C	Reel
CLC4003ITP14†	TSSOP-14	Yes	-55°C to +125°C	Rail

*Preliminary Product Information, †Future Product Offering

Moisture sensitivity level for all parts is MSL-1.

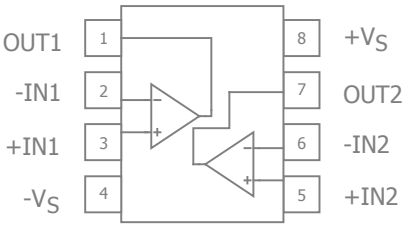
CLC1003 Pin Configuration



CLC1003 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$+V_S$	Positive supply

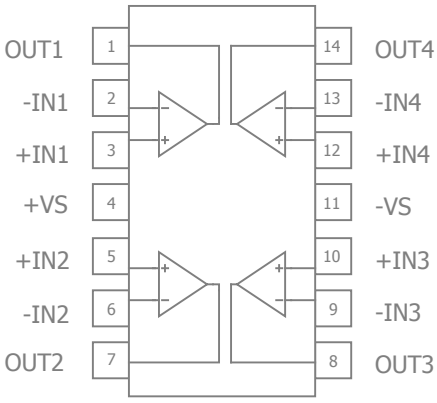
CLC2003 Pin Configuration



CLC2003 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

CLC4003 Pin Configuration



CLC4003 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$+V_S$	Positive supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	$-V_S$	Negative supply
12	+IN4	Positive input, channel 4
13	-IN4	Negative input, channel 4
14	OUT4	Output, channel 4

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Package Thermal Resistance				
5-Lead SOT23		TBD		°C/W
8-Lead SOIC		100		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOT23-5	SOIC-8
Human Body Model (HBM)	TBD	TBD
Charged Device Model (CDM)	TBD	TBD

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-55		+125	°C
Supply Voltage Range	2.5		12	V

Electrical Characteristics at +3V

T_A = 25°C, V_S = +3V, R_f = 1kΩ, R_L = 150Ω to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product	G = 10, V_{OUT} = 0.05V_{pp}		32		MHz
UGBW	Unity Gain Bandwidth	V_{OUT} = 0.05V_{pp}		64		MHz
BW_{SS}	-3dB Bandwidth	V_{OUT} = 0.05V_{pp}		23		MHz
BW_{LS}	Large Signal Bandwidth	V_{OUT} = 2V_{pp}		3.9		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		150		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		220		ns
	Settling Time to 0.01%	V_{OUT} = 1V step		250		ns
OS	Overshoot	V_{OUT} = 1V step		0		%
SR	Slew Rate	2V step		11.7		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 10kHz, R_L = 1kΩ		-98		dBc
		2V_{pp}, 100kHz, R_L = 100Ω		-85		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 10kHz, R_L = 1kΩ		-95		dBc
		2V_{pp}, 100kHz, R_L = 100Ω		-81		dBc
THD	Total Harmonic Distortion	1V_{pp}, 1kHz, G=1, R_L = 2kΩ		0.0005		%
e_n	Input Voltage Noise	> 10kHz		3.7		nV/√Hz
DC Performance						
V_{IO}	Input Offset Voltage			30		µV
dV_{IO}	Average Drift			TBD		µV/°C
I_b	Input Bias Current			130		nA
dI_b	Average Drift			TBD		nA/°C
I_{os}	Input Offset Current			5		nA
PSRR	Power Supply Rejection Ratio	DC		100		dB
A_{OL}	Open-Loop Gain	V_{OUT} = V_S / 2		110		dB
I_S	Supply Current	per channel		1.65		mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		TBD		MΩ
C_{IN}	Input Capacitance			TBD		pF
CMIR	Common Mode Input Range			TBD		V
CMRR	Common Mode Rejection Ratio	DC , V_{cm}=1.5V to 4V		80		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		TBD		mΩ
V_{OUT}	Output Voltage Swing	R_L = 150Ω		0.15 to 2.75		V
		R_L = 1kΩ		TBD		V
I_{OUT}	Output Current			±60		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		±85		mA

Notes:

1. 100% tested at 25°C

Electrical Characteristics at ±5V

T_A = 25°C, V_S = ±5V, R_f = 1kΩ, R_L = 150Ω to GND, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product	G = 10, V_{OUT} = 0.05V_{pp}		37		MHz
UGBW	Unity Gain Bandwidth	V_{OUT} = 0.05V_{pp}		70		MHz
BW_{SS}	-3dB Bandwidth	V_{OUT} = 0.05V_{pp}		25		MHz
BW_{LS}	Large Signal Bandwidth	V_{OUT} = 2V_{pp}		4.4		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		125		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		165		ns
	Settling Time to 0.01%	V_{OUT} = 1V step		180		ns
OS	Overshoot	V_{OUT} = 1V step		0		%
SR	Slew Rate	2V step		13.5		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 10kHz, R_L = 1kΩ		-125		dBc
		2V_{pp}, 100kHz, R_L = 100Ω		-90		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 10kHz, R_L = 1kΩ		-127		dBc
		2V_{pp}, 100kHz, R_L = 100Ω		-85		dBc
THD	Total Harmonic Distortion	1V_{pp}, 1kHz, G=1, R_L = 2kΩ		0.00005		%
e_n	Input Voltage Noise	> 10kHz		3.5		nV/√Hz
DC Performance						
V_{IO}	Input Offset Voltage(1)			25	<1mV	µV
dV_{IO}	Average Drift			TBD		µV/°C
I_b	Input Bias Current (1)			0.070	1.2	µA
dI_b	Average Drift			TBD		nA/°C
I_{os}	Input Offset Current (1)			1	45	nA
PSRR	Power Supply Rejection Ratio (1)	DC		100		dB
A_{OL}	Open-Loop Gain (1)	V_{OUT} = V_S / 2		115		dB
I_S	Supply Current (1)	per channel		2	2.5	mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		TBD		MΩ
C_{IN}	Input Capacitance			TBD		pF
CMIR	Common Mode Input Range			±5.3		V
CMRR	Common Mode Rejection Ratio (1)	DC , V_{cm}= -5V to 5V	70	85		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		TBD		mΩ
V_{OUT}	Output Voltage Swing	R_L = 150Ω (1)	±4.4	±4.7		V
		R_L = 1kΩ		TBD		V
I_{OUT}	Output Current			±60		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		±85		mA

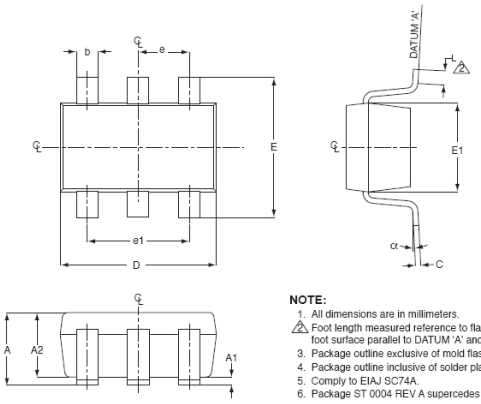
Notes:

1. 100% tested at 25°C

Mechanical Dimensions

SOT23-6 Package

SOT23-6

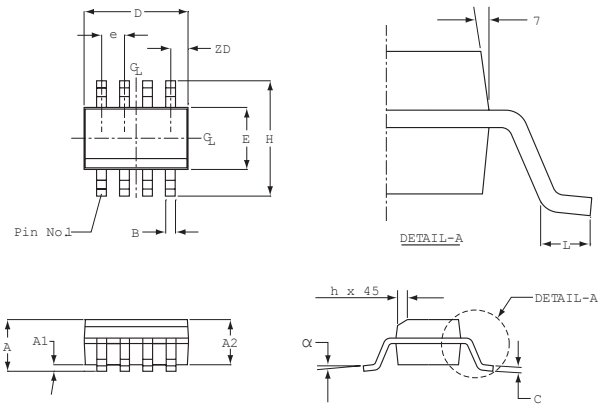


SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.25	0.50
C	0.09	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 ref	
e1	1.90 ref	
α	0°	10°

NOTE:

1. All dimensions are in millimeters.
2. Foot length measured reference to flat foot surface parallel to DATUM 'A' and lead surface.
3. Package outline exclusive of mold flash & metal burr.
4. Package outline inclusive of solder plating.
5. Comply to EIAJ SC74A.
6. Package ST 0004 REV A supercedes SOT-D-2006 REV C.

SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
	0°	8°
ZD	0.53 ref	
A2	1.37	1.57

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.10mm (.004") max.
3. Package surface finishing:
   (2.1) Top: matte (charmilles #18~30).
   (2.2) All sides: matte (charmilles #18~30).
   (2.3) Bottom: smooth or matte (charmilles #18~30).
4. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.15mm (.006) per side (D).

For additional information regarding our products, please visit CADEKA at: cadeka.com

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