Octal buffer/line driver; 3-state   74LVC241

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages up to 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC241 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment

The 74LVC241 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1$\overline{OE}$ and 2OE. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

FUNCTION TABLES

INPUTS		OUTPUT
1$\overline{OE}$	1A_n	1Y_n
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
2OE	2A_n	2Y_n
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay 1A_n to 1Y_n; 2A_n to 2Y_n	C_L = 50 pF V_{CC} = 3.3 V	4.8	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz; C_L = output load capacity in pF;

   f_o = output frequency in MHz; V_{CC} = supply voltage in V;

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC241D	20	SO	plastic	SOT163-1
74LVC241DB	20	SSOP	plastic	SOT339-1
74LVC241PW	20	TSSOP	plastic	SOT360-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1$\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	1A_0 to 1A_3	data inputs
3, 5, 7, 9	2Y_0 to 2Y_3	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	2A_0 to 2A_3	data inputs
18, 16, 14, 12	1Y_0 to 1Y_3	bus outputs
19	2OE	output enable input (active HIGH)
20	V_{CC}	positive power supply

Octal buffer/line driver; 3-state

Fig.1 Pin configuration.

Fig.2 Logic symbol.

Fig.3 IEC logic symbol.

Fig.4 Functional diagram.
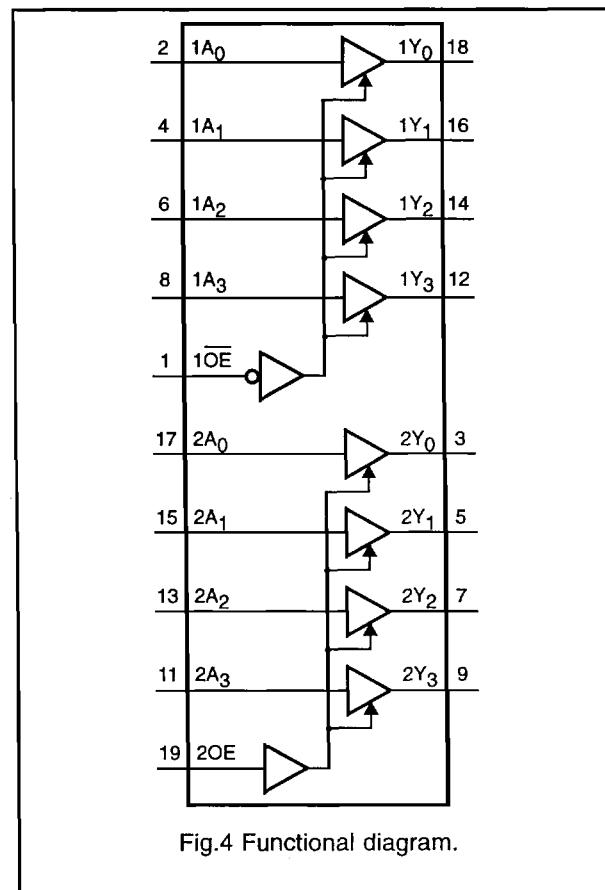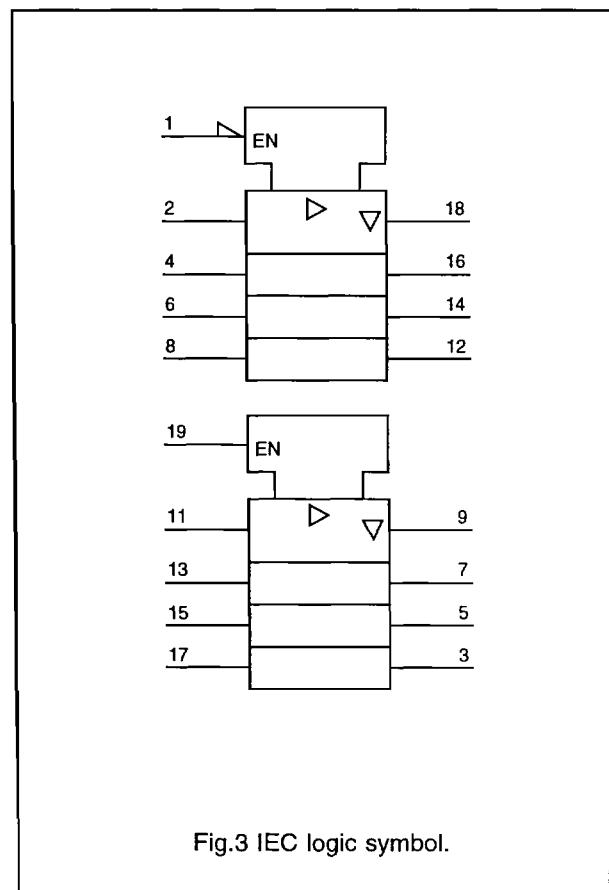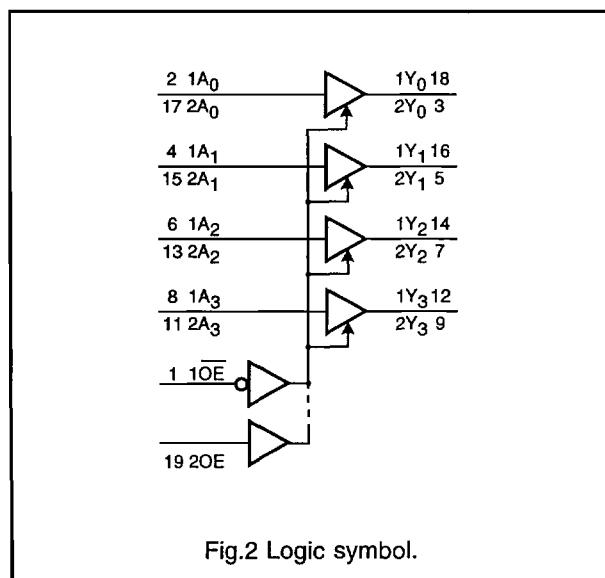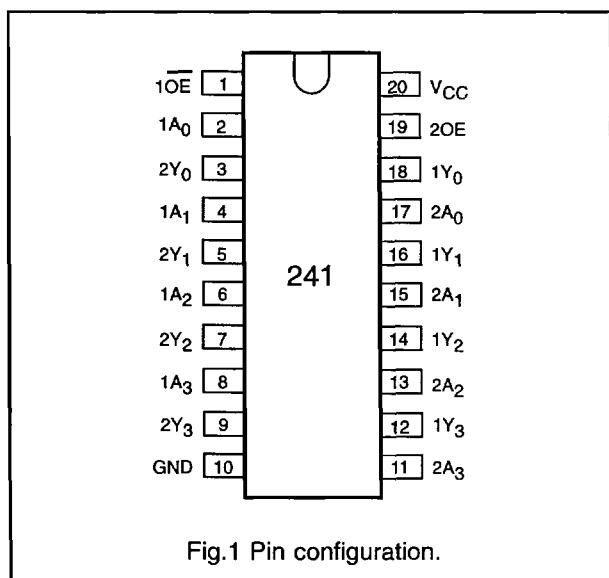
Octal buffer/line driver; 3-state

DC CHARACTERISTICS FOR 74LVC241

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC241

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay 1A$_n$ to 1Y$_n$; 2A$_n$ to 2Y$_n$	– 1.5 1.5	23 5.1 4.8*	– 7.7 7.3	ns	1.2 2.7 3.0 to 3.6	Figs 5, 8
t_{PZH}/t_{PZL}	3-state output enable time 1$\overline{OE}$ to 1Y$_n$	– 1.5 1.5	48 5.9 5.6*	– 8.5 8.1	ns	1.2 2.7 3.0 to 3.6	Figs 6, 8
t_{PHZ}/t_{PLZ}	3-state output disable time 1$\overline{OE}$ to 1Yn	– 1.5 1.5	5.8 3.8 3.6*	– 5.9 5.5	ns	1.2 2.7 3.0 to 3.6	Figs 6, 8
t_{PZH}/t_{PZL}	3-state output enable time 2OE to 2Y$_n$	– 1.5 1.5	42 5.9 5.6*	– 8.5 8.1	ns	1.2 2.7 3.0 to 3.6	Figs 7, 8
t_{PHZ}/t_{PLZ}	3-state output disable time 2OE to 2Y$_n$	– 1.5 1.5	7.5 3.8 3.6*	– 5.9 5.5	ns	1.2 2.7 3.0 to 3.6	Figs 7, 8

Notes: All typical values are measured at T_{amb} = 25 °C.

* Typical values are measured at V_{CC} = 3.3 V.

Octal buffer/line driver; 3-state
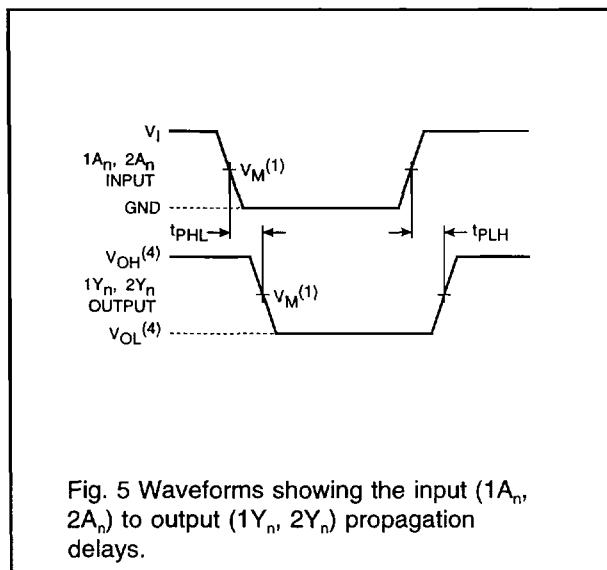
AC WAVEFORMS

Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.
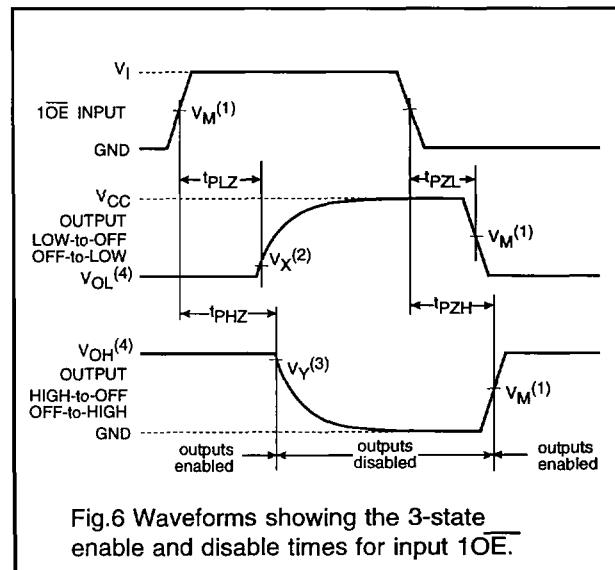
Fig.6 Waveforms showing the 3-state enable and disable times for input $1\overline{OE}$.
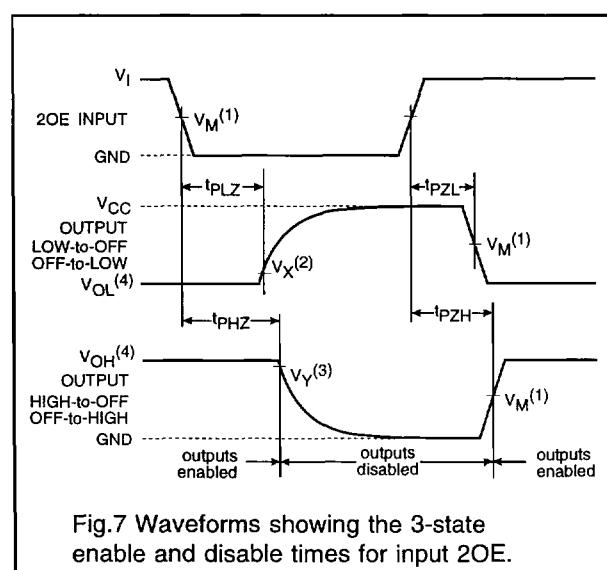
Fig.7 Waveforms showing the 3-state enable and disable times for input 2OE.
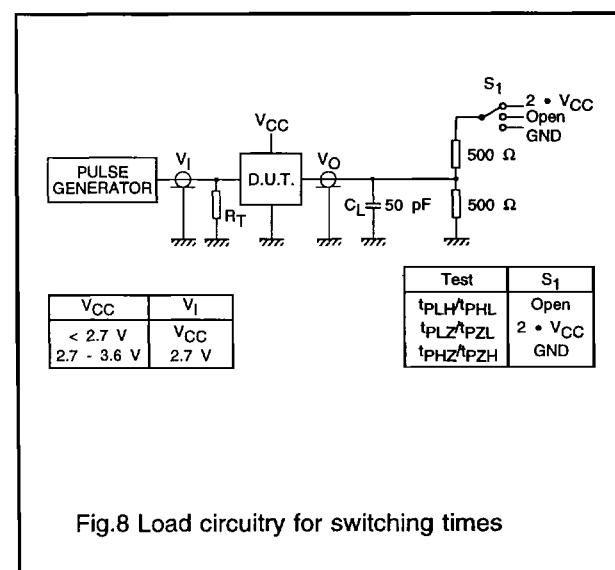
Fig.8 Load circuitry for switching times

V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.