

SN54HCT32, SN74HCT32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

D3246, NOVEMBER 1988

- Inputs are TTL-Voltage Compatible
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

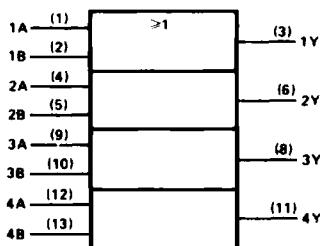
These devices contain four independent 2-input OR gates. They perform the Boolean functions $Y = \bar{A} \cdot \bar{B}$ or $Y = A + B$ in positive logic.

The SN54HCT32 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT32 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

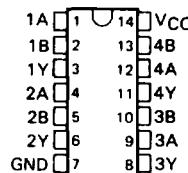
logic symbol†



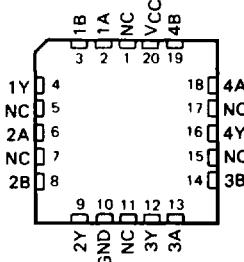
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

SN54HCT32 . . . J PACKAGE
SN74HCT32 . . . D OR N PACKAGE
(TOP VIEW)



SN54HCT32 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic diagram (each gate) (positive logic)



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HCMLos Devices

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SN54HCT32, SN74HCT32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

absolute maximum ratings over operating free-air temperature range[†]

Supply voltage, V _{CC}	-0.5 V to 7 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND pins	±50 mA
Lead temperature 1.6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1.6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	-65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

Parameter	Description	SN54HCT32			SN74HCT32			Unit
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2		2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V	0	0.8	0	0.8		V
V _I	Input voltage		0	V _{CC}	0	V _{CC}		V
V _O	Output voltage		0	V _{CC}	0	V _{CC}		V
t _{tr}	Input transition (rise and fall) times		0	500	0	500		ns
T _A	Operating free-air temperature	-55		125	-40		85	°C

SN54HCT32, SN74HCT32
QUADRUPLE 2-INPUT POSITIVE-OR GATES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HCT32		SN74HCT32		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL} , I _{OH} = -20 µA	4.5 V	4.4	4.499		4.4		4.4		V
	V _I = V _{IH} or V _{IL} , I _{OH} = -4 mA	4.5 V	3.98	4.30		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL} , I _{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
	V _I = V _{IH} or V _{IL} , I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0	5.5 V			2		40		20	µA
ΔI _{CC} [†]	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V _{CC}	5.5 V		1.4	2.4		3		2.9	mA
C _i		4.5 to 5.5 V		3	10		10		10	pF

[†]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT32		SN74HCT32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	4.5 V		15	24		36		30	ns
			5.5 V		13	22		32		27	
t _t		Y	4.5 V		9	15		22		19	ns
			5.5 V		8	14		20		17	

C _{pd}	Power dissipation capacitance per gate	No load, T _A = 25°C	20 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1 of the *High-Speed CMOS Logic Data Book*, 1988.