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Kind regards,

Team Nexperia

74LVTN16245B

3.3 V 16-bit transceiver; 3-state

Rev. 5 — 5 April 2012

Product data sheet

1. General description

The 74LVTN16245B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an output enable input (\overline{nOE}) for easy cascading and a direction input ($nDIR$) for direction control.

2. Features and benefits

- 16-bit bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Power-up 3-state
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Latch-up protection
 - ◆ JESD78B Class II exceeds 500 mA
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-----------------|-------------------|---------|---|-----------|
| | Temperature range | Name | Description | |
| 74LVTN16245BDGG | -40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |
| 74LVTN16245BBX | -40 °C to +125 °C | HXQFN60 | plastic compatible thermal enhanced extremely thin quad flat package; no leads; 60 terminals; body 4 × 6 × 0.5 mm | SOT1134-2 |



4. Functional diagram

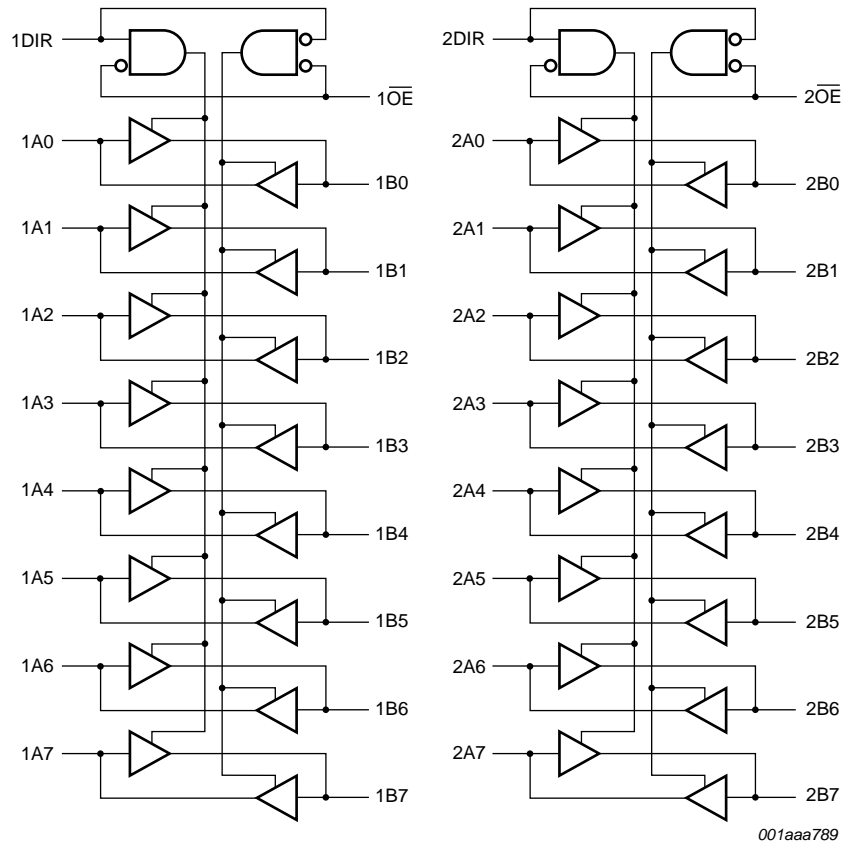


Fig 1. Logic symbol

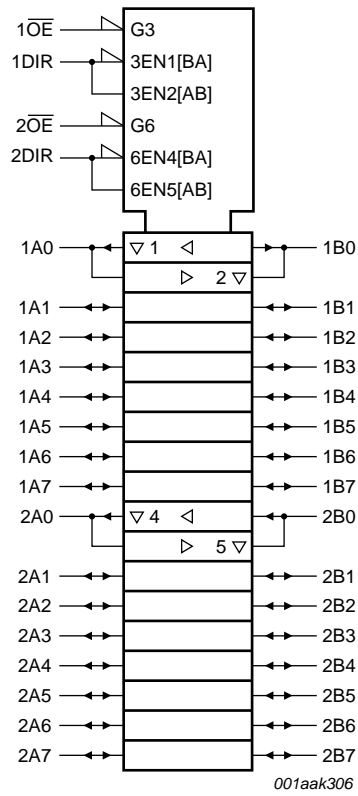
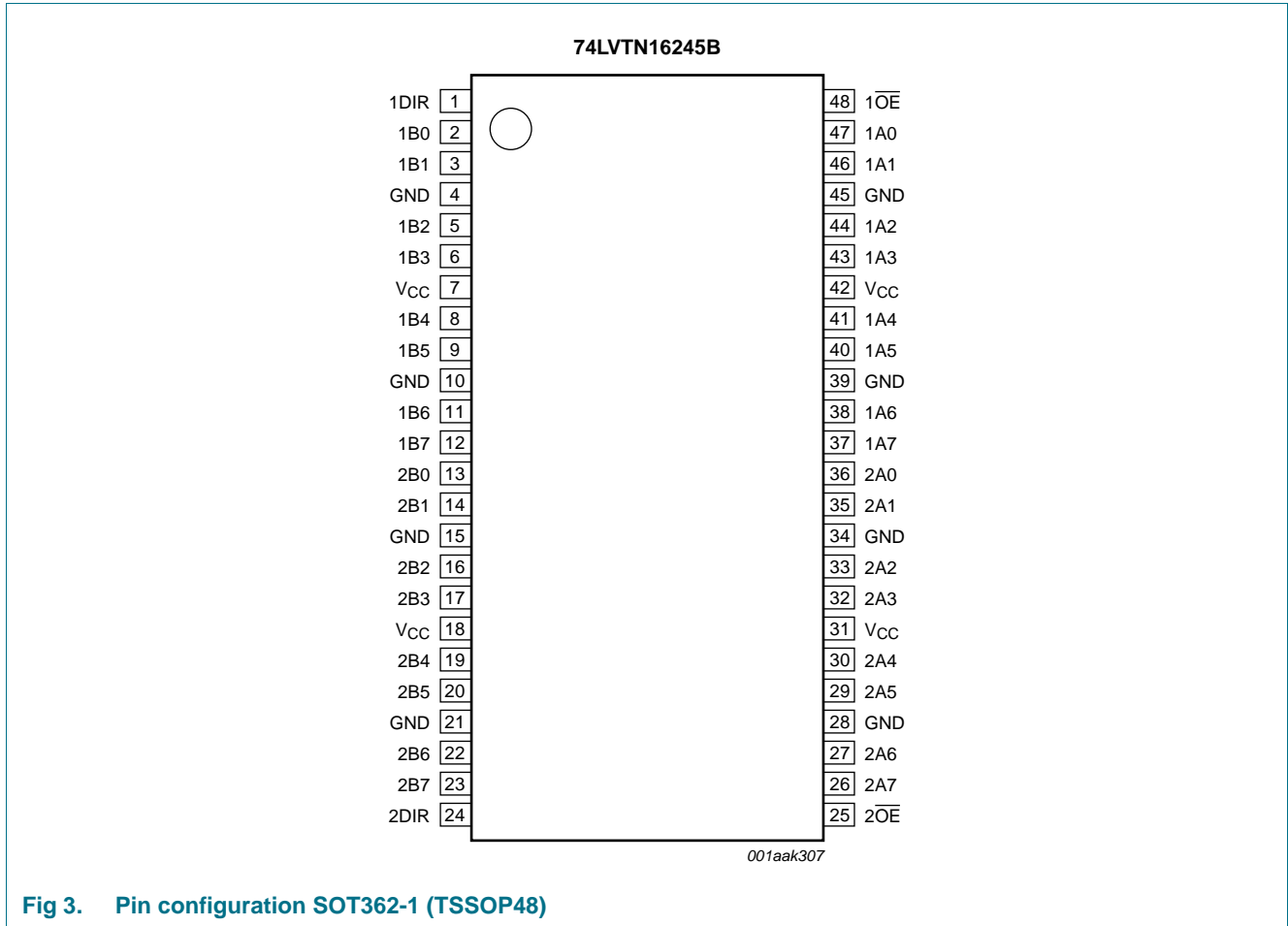
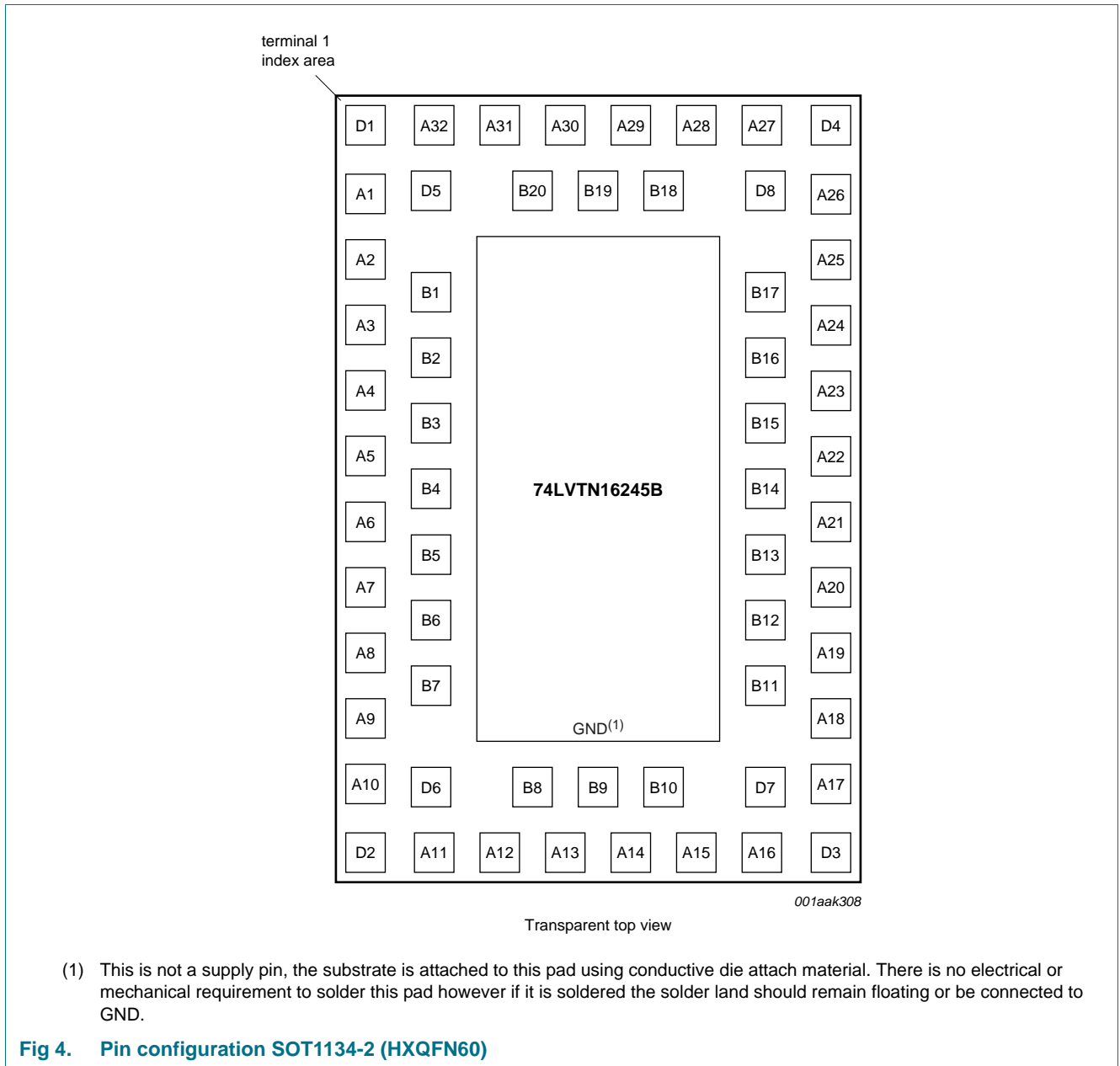


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning





5.2 Pin description

Table 2. Pin description

| Symbol | Pin | | Description |
|-----------------|--------------------------------|--|----------------------------------|
| | SOT362-1 | SOT1134-2 | |
| 1DIR, 2DIR | 1, 24 | A30, A13 | direction control input |
| 1B0 to 1B7 | 2, 3, 5, 6, 8, 9, 11, 12 | B20, A31, D5, D1, A2, B2, B3, A5 | data input/output |
| 2B0 to 2B7 | 13, 14, 16, 17, 19, 20, 22, 23 | A6, B5, B6, A9, D2, D6, A12, B8 | data input/output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | A32, A3, A8, A11, A16, A19, A24, A27 | ground (0 V) |
| V _{CC} | 7, 18, 31, 42 | A1, A10, A17, A26 | supply voltage |
| 1OE, 2OE | 48, 25 | A29, A14 | output enable input (active LOW) |
| 2A0 to 2A7 | 36, 35, 33, 32, 30, 29, 27, 26 | A21, B13, B12, A18, D3, D7, A15, B10 | data input/output |
| 1A0 to 1A7 | 47, 46, 44, 43, 41, 40, 38, 37 | B18, A28, D8, D4, A25, B16, B15, A22 | data input/output |
| n.c. | - | A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19 | not connected |

6. Functional description

Table 3. Function table [1]

| Control | | Input/output | |
|---------|------|------------------|------------------|
| nOE | nDIR | nAn | nBn |
| L | L | output nAn = nBn | input |
| L | H | input | output nBn = nAn |
| H | X | Z | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|-----------------------------------|----------|------|------|
| V _{CC} | supply voltage | | -0.5 | +4.6 | V |
| V _I | input voltage | | [1] -0.5 | +7.0 | V |
| V _O | output voltage | output in OFF-state or HIGH-state | [1] -0.5 | +7.0 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| I _{OK} | output clamping current | V _O < 0 V | -50 | - | mA |
| I _O | output current | output in LOW-state | - | 128 | mA |
| | | output in HIGH-state | -64 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| T _j | junction temperature | | [2] - | 150 | °C |

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|-------------------------------------|-------|------|------|
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +85 °C | | | |
| | | TSSOP48 package | [3] - | 500 | mW |
| | | HXQFN60 package | [4] - | 1000 | mW |

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
- [3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
- [4] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-------------------------------------|--|-----|-----|-----|------|
| V _{CC} | supply voltage | | 2.7 | - | 3.6 | V |
| V _I | input voltage | | 0 | - | 5.5 | V |
| V _{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I _{OH} | HIGH-level output current | | -32 | - | - | mA |
| I _{OL} | LOW-level output current | none | - | - | 32 | mA |
| | | current duty cycle ≤ 50 %; f _i ≥ 1 kHz | - | - | 64 | mA |
| T _{amb} | ambient temperature | in free-air | -40 | - | +85 | °C |
| Δt/ΔV | input transition rise and fall rate | outputs enabled | - | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-------------------------------------|---------------------------|---|-----------------------|--------------------|------|------|
| T _{amb} = -40 °C to +85 °C | | | | | | |
| V _{IK} | input clamping voltage | V _{CC} = 2.7 V; I _{IK} = -18 mA | -1.2 | -0.85 | - | V |
| V _{OH} | HIGH-level output voltage | I _{OH} = -100 μA; V _{CC} = 2.7 V to 3.6 V | V _{CC} - 0.2 | V _{CC} | - | V |
| | | I _{OH} = -8 mA; V _{CC} = 2.7 V | 2.4 | 2.5 | - | V |
| | | I _{OH} = -32 mA; V _{CC} = 3.0 V | 2.0 | 2.3 | - | V |
| V _{OL} | LOW-level output voltage | V _{CC} = 2.7 V | | | | |
| | | I _{OL} = 100 μA | - | 0.07 | 0.2 | V |
| | | I _{OL} = 24 mA | - | 0.3 | 0.5 | V |
| | | V _{CC} = 3.0 V | | | | |
| | | I _{OL} = 16 mA | - | 0.25 | 0.4 | V |
| | | I _{OL} = 32 mA | - | 0.3 | 0.5 | V |
| | | I _{OL} = 64 mA | - | 0.4 | 0.55 | V |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-----------------------|------------------------------------|--|------------------|--------------------|------|------|
| I _I | input leakage current | control pins | | | | |
| | | V _{CC} = 3.6 V; V _I = V _{CC} or GND | - | 0.1 | ±1 | μA |
| | | V _{CC} = 0 V or 3.6 V; V _I = 5.5 V | - | 0.1 | 10 | μA |
| | | input/output data pins; V _{CC} = 3.6 V | ^[2] | | | |
| | | V _I = 5.5 V | - | 0.1 | 20 | μA |
| | | V _I = V _{CC} | - | 0.5 | 10 | μA |
| | | V _I = 0 V | -5 | -0.1 | - | μA |
| I _{OFF} | power-off leakage current | V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V | - | 0.1 | ±100 | μA |
| I _{LO} | output leakage current | output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V | - | 75 | 125 | μA |
| I _{O(pu/pd)} | power-up/power-down output current | V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; n \overline{OE} = don't care | ^[3] - | 40 | ±100 | μA |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A | | | | |
| | | output HIGH | - | 0.07 | 0.12 | mA |
| | | output LOW | - | 4.0 | 6.0 | mA |
| | | outputs disabled | ^[4] - | 0.07 | 0.12 | mA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 3.0 V to 3.6 V; one input at V _{CC} - 0.6 V other inputs at V _{CC} or GND | ^[5] - | 0.1 | 0.2 | mA |
| C _I | input capacitance | pins nDIR and n \overline{OE} , V _O = 0 V or 3.0 V | - | 3 | - | pF |
| C _{io(off)} | off-state input/output capacitance | pins nAn and nBn, outputs disabled; V _O = GND or V _{CC} | - | 9 | - | pF |

[1] Typical values are measured at V_{CC} = 3.3 V and at T_{amb} = 25 °C.

[2] Unused pins at V_{CC} or GND.

[3] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[4] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[5] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

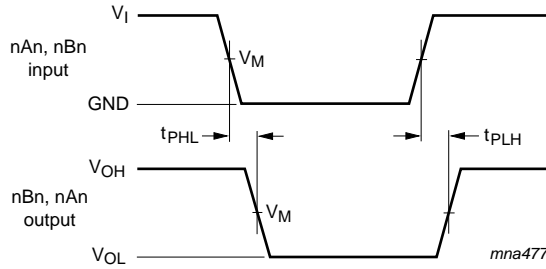
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---|-------------------------------------|--|-----|--------------------|-----|------|
| T_{amb} = -40 °C to +85 °C | | | | | | |
| t _{PLH} | LOW to HIGH propagation delay | nAn to nBn or nBn to nAn; see Figure 5 | | | | |
| | | V _{CC} = 2.7 V | - | - | 3.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 1.9 | 3.3 | ns |
| t _{PHL} | HIGH to LOW propagation delay | nAn to nBn or nBn to nAn; see Figure 5 | | | | |
| | | V _{CC} = 2.7 V | - | - | 3.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 1.7 | 3.3 | ns |
| t _{PZH} | OFF-state to HIGH propagation delay | n $\overline{\text{OE}}$ to nAn or nBn; see Figure 6 | | | | |
| | | V _{CC} = 2.7 V | - | - | 5.3 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.8 | 4.5 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | n $\overline{\text{OE}}$ to nAn or nBn; see Figure 6 | | | | |
| | | V _{CC} = 2.7 V | - | - | 5.1 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.8 | 4.1 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | n $\overline{\text{OE}}$ to nAn or nBn; see Figure 6 | | | | |
| | | V _{CC} = 2.7 V | - | - | 5.7 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.5 | 3.2 | 5.1 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | n $\overline{\text{OE}}$ to nAn or nBn; see Figure 6 | | | | |
| | | V _{CC} = 2.7 V | - | - | 4.6 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.5 | 3.0 | 4.6 | ns |

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

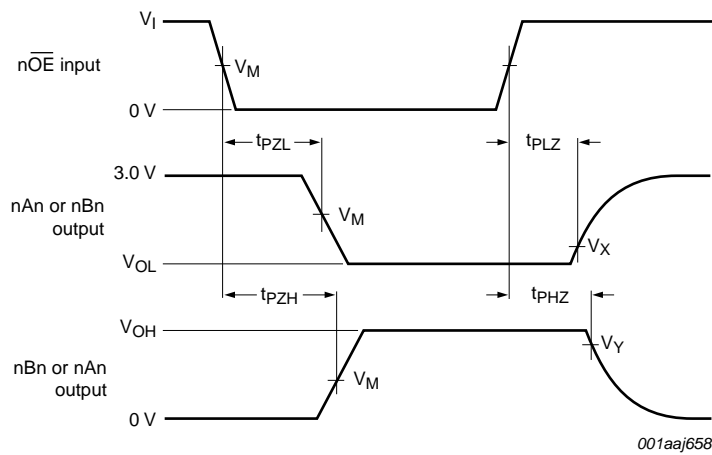
11. Waveforms



Measurements points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay input (nAn, nBn) to output (nBn, nAn)



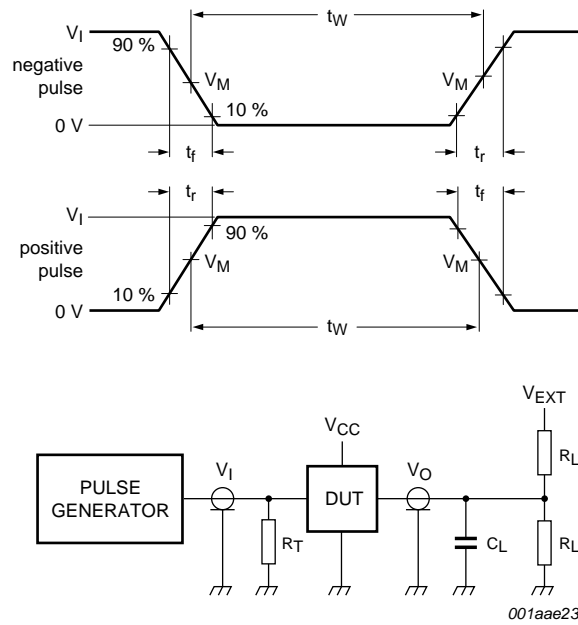
Measurements points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Enable and disable times

Table 8. Measurement points

| Input | Output | | |
|-------|--------|------------------|------------------|
| V_M | V_M | V_X | V_Y |
| 1.5 V | 1.5 V | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|---------------|--------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} | t_{PLH}, t_{PHL} |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

12. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

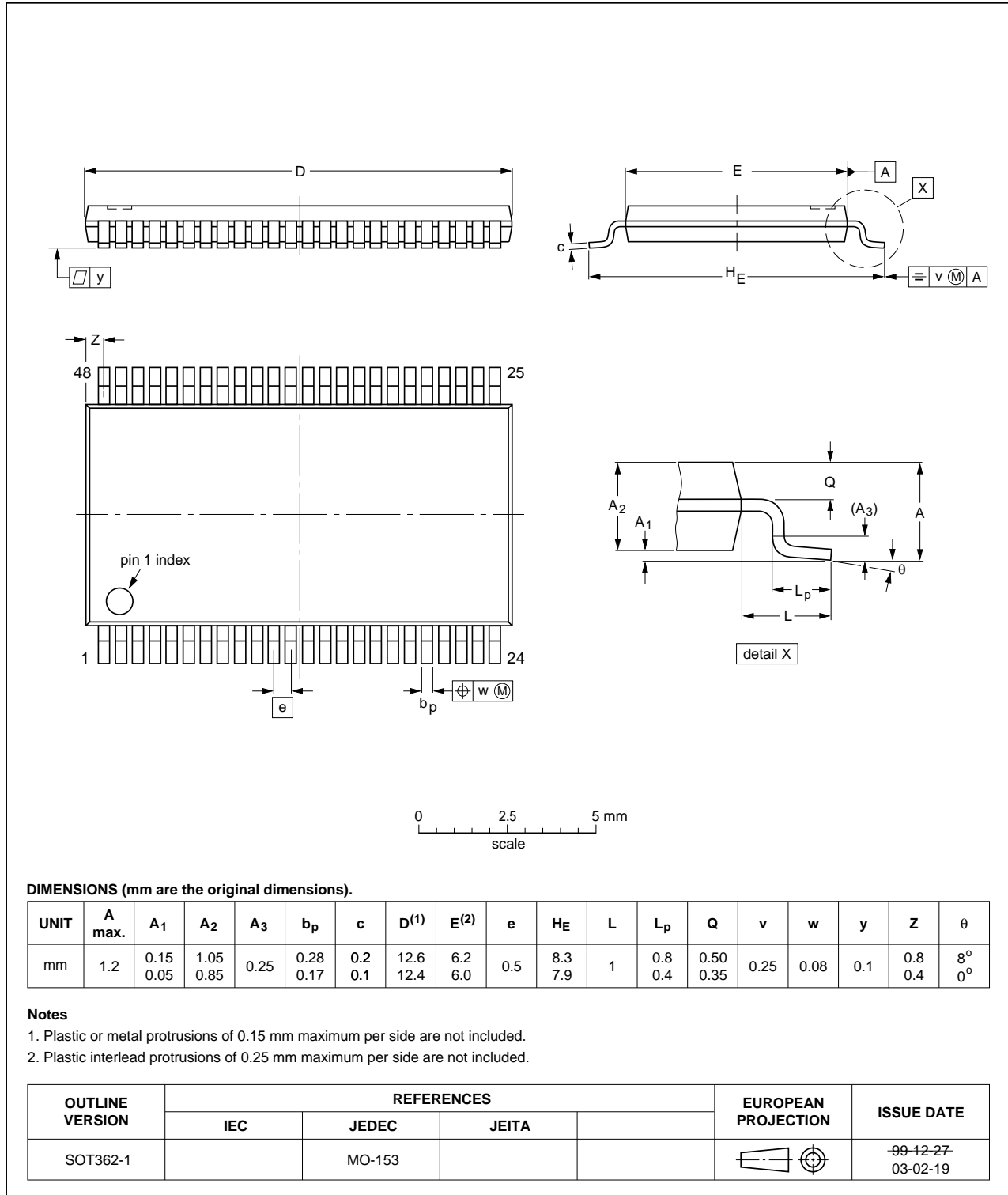


Fig 8. Package outline SOT362-1 (TSSOP48)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| BICMOS | Bipolar Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--|--------------------|---------------|------------------|
| 74LVTN16245B v.5 | 20120405 | Product data sheet | - | 74LVTN16245B v.4 |
| Modifications: | <ul style="list-style-type: none"> For type number 74LVTN16245BBX the SOT code has changed to SOT1134-2 | | | |
| 74LVTN16245B v.4 | 20111122 | Product data sheet | - | 74LVTN16245B v.3 |
| Modifications: | <ul style="list-style-type: none"> Legal pages updated. | | | |
| 74LVTN16245B v.3 | 20110615 | Product data sheet | - | 74LVTN16245B v.2 |
| 74LVTN16245B v.2 | 20100323 | Product data sheet | - | 74LVTN16245B v.1 |
| 74LVTN16245B v.1 | 20090729 | Product data sheet | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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