



Integrated Device Technology, Inc.

FAST CMOS 16-BIT LATCHED TRANSCEIVER

IDT54/74FCT16543T/AT/CT/ET
IDT54/74FCT162543T/AT/CT/ET

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **High-speed, low-power CMOS replacement for ABT functions**
 - **Typical tsk(o) (Output Skew) < 250ps**
 - **Low input and output leakage $\leq 1\mu\text{A}$ (max.)**
 - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
 - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
 - Extended commercial range of -40°C to +85°C
 - Vcc = 5V $\pm 10\%$
- **Features for FCT16543T/AT/CT/ET:**
 - High drive outputs (-32mA IOH, 64mA IOL)
 - Power off disable outputs permit "live insertion"
 - Typical VOLP (Output Ground Bounce) < 1.0V at Vcc = 5V, TA = 25°C
- **Features for FCT162543T/AT/CT/ET:**
 - Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
 - Reduced system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.6V at Vcc = 5V, TA = 25°C

DESCRIPTION:

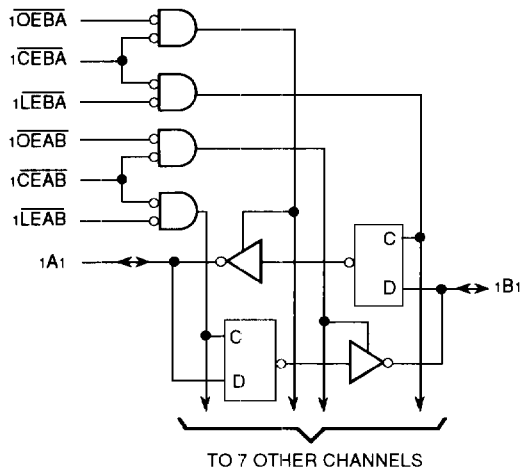
The IDT54/74FCT16543T/AT/CT/ET and IDT54/74FCT162543T/AT/CT/ET 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable ($\overline{x\text{CEAB}}$) must be LOW in order to enter data from the A port or to output data from the B port. $\overline{x\text{LEAB}}$ controls the latch function. When $\overline{x\text{LEAB}}$ is LOW, the latches are transparent. A subsequent LOW-to-HIGH transition of $\overline{x\text{LEAB}}$ signal puts the A latches in the storage mode. $\overline{x\text{OEAB}}$ performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using $\overline{x\text{CEBA}}$, $\overline{x\text{LEBA}}$, and $\overline{x\text{OEBA}}$ inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16543T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

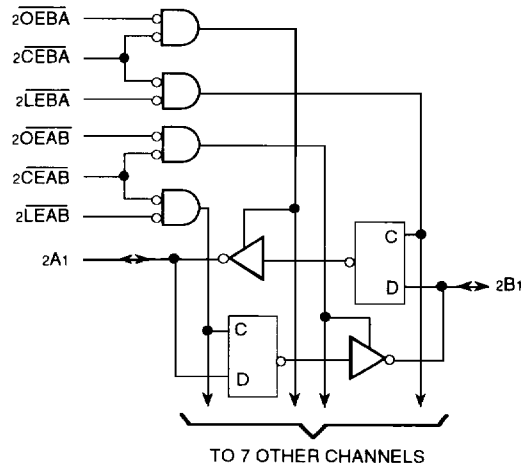
The IDT54/74FCT162543T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The IDT54/74FCT162543T/AT/CT/ET are plug-in replacements for the IDT54/74FCT16543T/AT/CT/ET and 54/74ABT16543 for on-board bus interface applications.

5

FUNCTIONAL BLOCK DIAGRAM



2618 drw 01



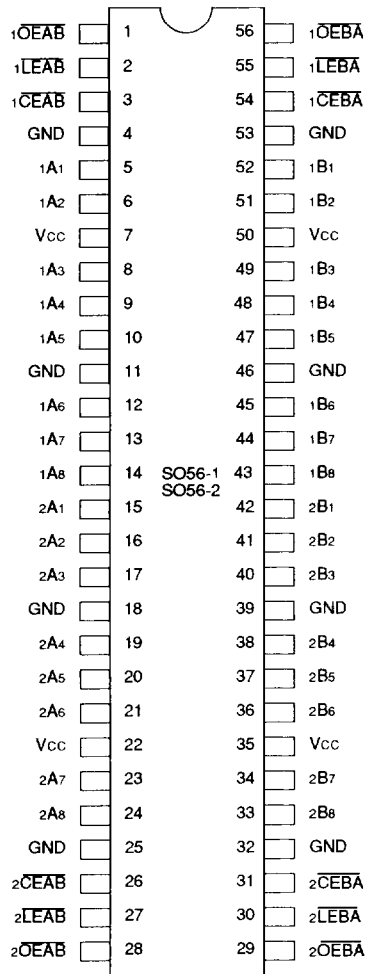
2618 drw 02

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

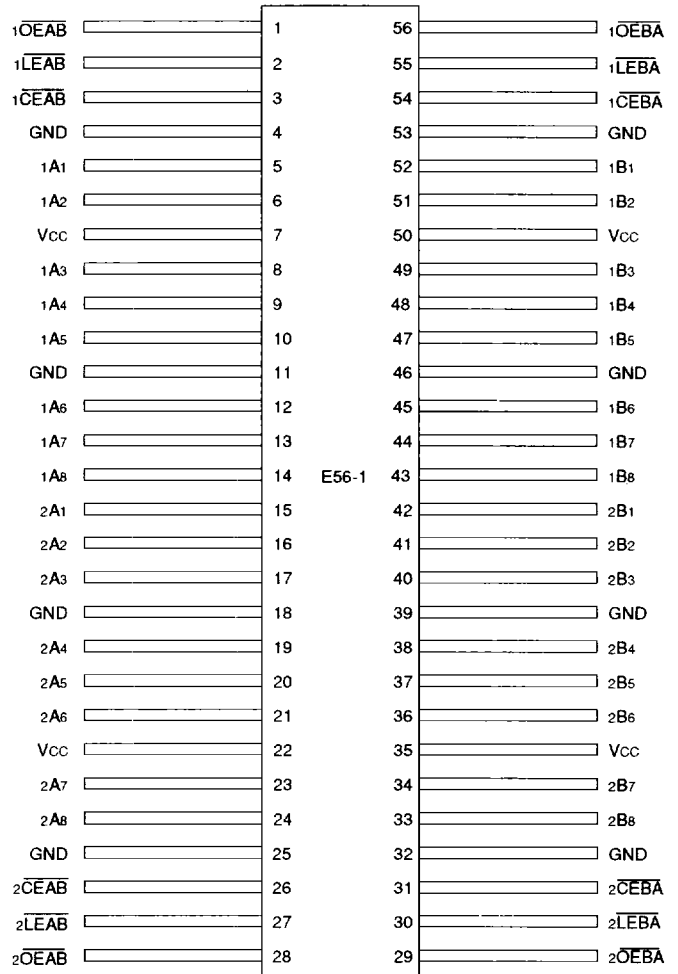
APRIL 1994

PIN CONFIGURATIONS



**SSOP
 TSSOP
 TOP VIEW**

2618 drw 03



**CERPACK
 TOP VIEW**

2618 drw 04

PIN DESCRIPTION

Pin Names	Description
xOEAB	A-to-B Output Enable Input (Active LOW)
xOEBĀ	B-to-A Output Enable Input (Active LOW)
xCEAB	A-to-B Enable Input (Active LOW)
xCEBĀ	B-to-A Enable Input (Active LOW)
xLEAB	A-to-B Latch Enable Input (Active LOW)
xLEBĀ	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

2618 tbl 01

FUNCTION TABLE^(1, 2)

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
xCEAB	xLEAB	xOEBĀ	xAx to xBx	xBx
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

2618 tbl 02

NOTES:

- * Before xLEAB LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
- A-to-B data flow shown; B-to-A flow control is the same, except using xCEBĀ, xLEBĀ and xOEBĀ.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC +0.5	-0.5 to VCC +0.5	V
TA	Operating Temperature	-40 to +85	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

2618 lmk 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6.0	pF
CIO	I/O Capacitance	VOU = 0V	3.5	8.0	pF

2618 lmk 04

NOTE:

- This parameter is measured at characterization but not tested.



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾		V _I = GND	—	—	±1	
I _{IL}	Input LOW Current (Input pins) ⁽⁵⁾	V _{CC} = Max.	V _I = GND	—	—	±1	μA
	Input LOW Current (I/O pins) ⁽⁵⁾		V _O = 2.7V	—	—	±1	
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
I _{OZL}			V _O = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		-80	-140	-225	mA
I _O	Output Drive Current	V _{CC} = Max., V _O = 2.5V ⁽³⁾		-50	—	-180	mA
V _H	Input Hysteresis	—		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}		—	5	500	μA

2618 Ink 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16543T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3mA	2.5	3.5	—	V
			I _{OH} = -12mA MIL.	2.4	3.5	—	V
			I _{OH} = -15mA COM'L.	—	—	—	—
			I _{OH} = -24mA MIL. I _{OH} = -32mA COM'L. ⁽⁴⁾	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48mA MIL.	—	0.2	0.55	V
			I _{OL} = 64mA COM'L.	—	—	—	—
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V		—	—	±1	μA

2618 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162543T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -16mA MIL.	2.4	3.3	—	V
			I _{OH} = -24mA COM'L.	—	—	—	—
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 16mA MIL.	—	0.3	0.55	V
			I _{OL} = 24mA COM'L.	—	—	—	—

2618 Ink 07

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is ± 5μA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open x_{CEAB} and $x_{OEAB} = \text{GND}$ $x_{CEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu A/$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle x_{LEAB} , x_{CEAB} and $x_{OEAB} = \text{GND}$ $x_{CEBA} = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$, Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle x_{LEAB} , x_{CEAB} and $x_{OEAB} = \text{GND}$ $x_{CEBA} = V_{CC}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 ⁽⁵⁾	

2618 tbl 08

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_C P_{NCP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CC1}, I_{CC2} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_C P = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $NCP = \text{Number of Clock Inputs at } f_C P$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16543T/162543T				FCT16543AT/162543AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	8.5	1.5	10.0	1.5	6.5	1.5	7.5	ns
tPLH tPHL	Propagation Delay xLEBA to xAx, xLEAB to xBx		1.5	12.5	1.5	14.0	1.5	8.0	1.5	9.0	ns
tPZH tPZL	Output Enable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	12.0	1.5	14.0	1.5	9.0	1.5	10.0	ns
tPHZ tPLZ	Output Disable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	9.0	1.5	13.0	1.5	7.5	1.5	8.5	ns
tsu	Set-up Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		3.0	—	3.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2.0	—	2.0	—	2.0	—	2.0	—	ns
tw	xLEBA or xLEAB Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

2618 tbl 09

Symbol	Parameter	Condition ⁽¹⁾	FCT16543CT/162543CT				FCT16543ET/162543ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	5.3	1.5	6.1	1.5	3.4	—	—	ns
tPLH tPHL	Propagation Delay xLEBA to xAx, xLEAB to xBx		1.5	7.0	1.5	8.0	1.5	3.7	—	—	ns
tPZH tPZL	Output Enable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	8.0	1.5	9.0	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	6.5	1.5	7.5	1.5	4.0	—	—	ns
tsu	Set-up Time, HIGH or LOW xAx or xBx to xLEBA or xLEAB		2.0	—	2.0	—	1.0	—	—	—	ns
th	Hold Time HIGH or LOW xAx or xBx to xLEBA or xLEAB		2.0	—	2.0	—	1.0	—	—	—	ns
tw	xLEBA or xLEAB Pulse Width LOW		5.0	—	5.0	—	3.0 ⁽⁴⁾	—	—	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	—	ns

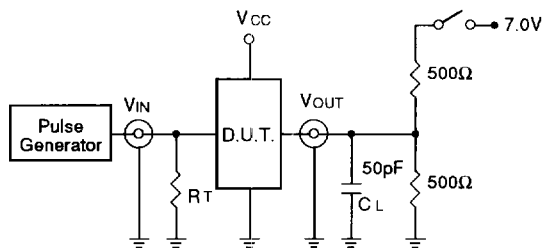
2618 tbl 10

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



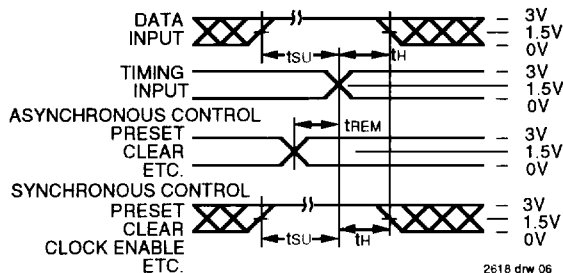
2618 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

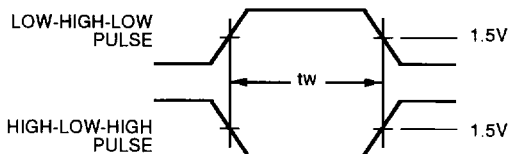
DEFINITIONS: 2618 Ink 10
 CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



2618 drw 06

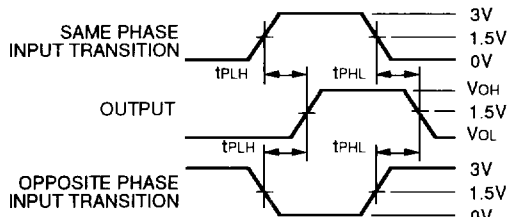
PULSE WIDTH



2618 drw 07

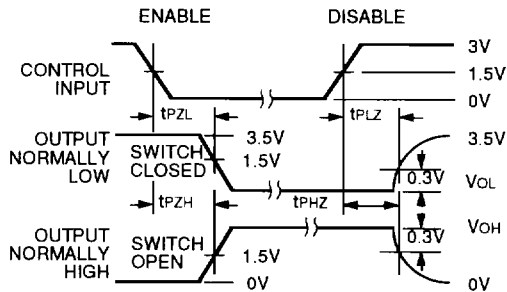
5

PROPAGATION DELAY



2618 drw 08

ENABLE AND DISABLE TIMES



2618 drw 09

- NOTES:**
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
 2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

ORDERING INFORMATION

