DUAL BINARY COUNTER

The TC74AC393 is an advanced high speed CMOS 4-BIT BINARY COUNTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

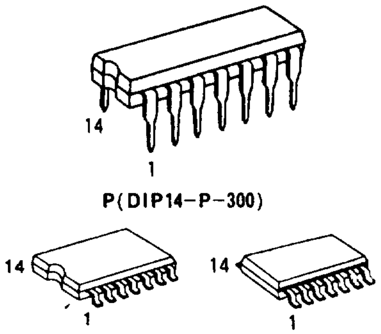
It contains two independent counter circuits in one package, so that counting or frequency division of eight binary bits can be achieved with one IC.

This device changes state on the negative going transition of the $\overline{\text{CLOCK}}$ pulse. The counter can be reset to "0" (Q0~Q3="L") by a high at the CLEAR input regardless of other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

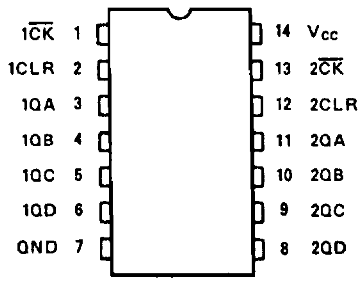
- High Speed ································ f_{MAX}= MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ············ I_{CC}=8μA(Max.)at Ta=25℃
- High Noise Immunity ··············· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ······ $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~5.5V
- Pin and Function Compatible with 74HC393



P(DIP14-P-300)

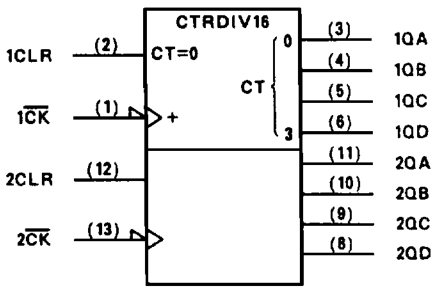
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	– – –	– – –	1.50 2.10 3.85	– – –	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	– – –	– – –	0.50 0.90 1.65	– – –	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	– – –	1.9 2.9 4.4	– – –	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 –	– – –	– – –	2.48 3.80 3.85	– – –	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	– – –	– – –	0.36 0.36 –	– – –	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	–	–	8.0	–	80.0	

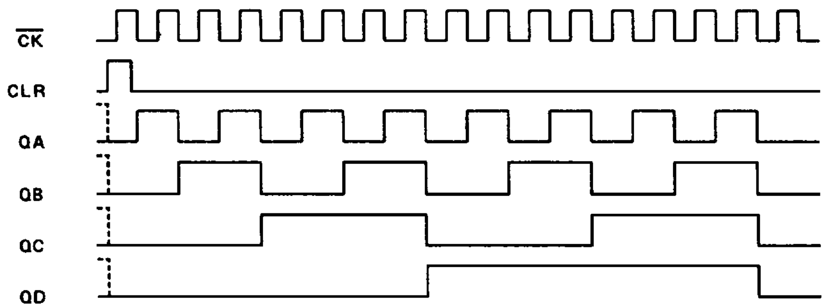
* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TRUTH TABLE

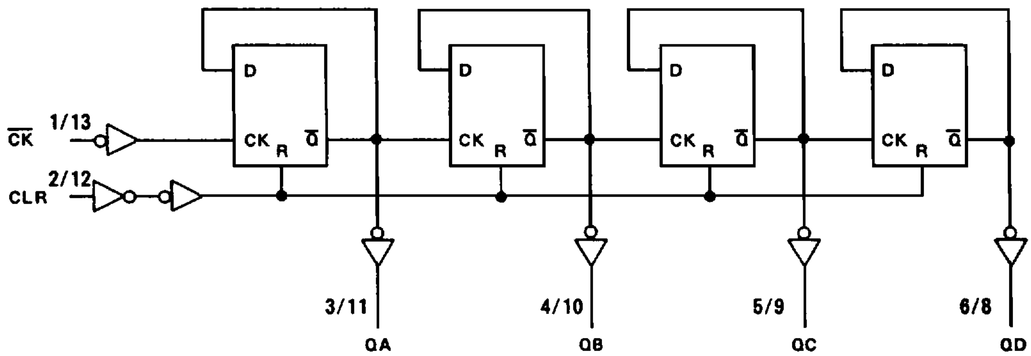
INPUTS		OUTPUTS			
$\overline{CK}$	CLR	QA	QB	QC	QD
X	H	L	L	L	L
↓ (falling edge)	L	COUNT UP			
↑ (rising edge)	L	NO CHANGE			

X : Don't care

TIMING CHART



SYSTEM DIAGRAM



TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=-40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		3.3±0.3 5.0±0.5	– –			ns
Minimum Pulse Width (CLR)	$t_{W(H)}$		3.3±0.3 5.0±0.5	– –			
Minimum Removal Time	t_{rem}		3.3±0.3 5.0±0.5	– –			

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω Input $t_r = t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=-40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK-QA)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	– –			1.0 1.0		ns
Propagation Delay Time (CK-QB)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	– –			1.0 1.0		
Propagation Delay Time (CK-QC)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	– –			1.0 1.0		
Propagation Delay Time (CK-QD)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	– –			1.0 1.0		
Propagation Delay Time (CLR-Qn)	t_{pHL}		3.3±0.3 5.0±0.5	– –			1.0 1.0		
Maximum Clock Frequency	f_{MAX}		3.3±0.3 5.0±0.5			– –		– –	MHz
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–		–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{(per circuit)}$$