CMOS ANALOG MULTIPLEXERS/DEMULTIPLEXERS

FEATURES

- Wide Range of Digital and Analog Signal Levels: Digital-3 to 15V, Analog-to $15V_{p-p}$
- Low ON-Resistance: 80Ω (typ.) over entire $15V_{p-p}$ Signal-Input Range for V_{DD}-V_{EE} = 15V
- High OFF-Resistance: Input Leakage ± 10pA (typ) @ V_{DD}-V_{EE} = 10V
- Logic-Level Conversion for Digital Addressing Signals of 3 to 15V (V_{DD}-V_{SS}= 3V to 15V) to Switch Analog Signals to $15V_{p-p}$ (V_{DD}-V_{EE} = 15V)
- Matched Switch Characteristics: ΔR_{ON} = 5Ω (typ.) for V_{DD}-V_{EE} = 18V
- Very Low Quiescent Power Dissipation under all Digital Control Input and Supply Conditions: 1μW typ. @ V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- Binary Address Decoding on Chip

DESCRIPTION

The 4051B, 4052B, and 4053B are Digitally-Controlled Analog Switches having low ON-impedance and very low OFF leakage current. Control of analog signals up to $15V_{p-p}$ can be achieved by digital signal amplitudes of 3 to 15V. For example, if V_{DD} = +5V, V_{SS} = 0V, and V_{EE} = -5V, analog signals from -5V to +5V can be controlled by digital inputs of 0 to 5V. The multiplexer circuits dissipate extremely low quiescent power over the full V_{DD} - V_{SS} and V_{DD} - V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the Inhibit input terminal all channels are OFF.

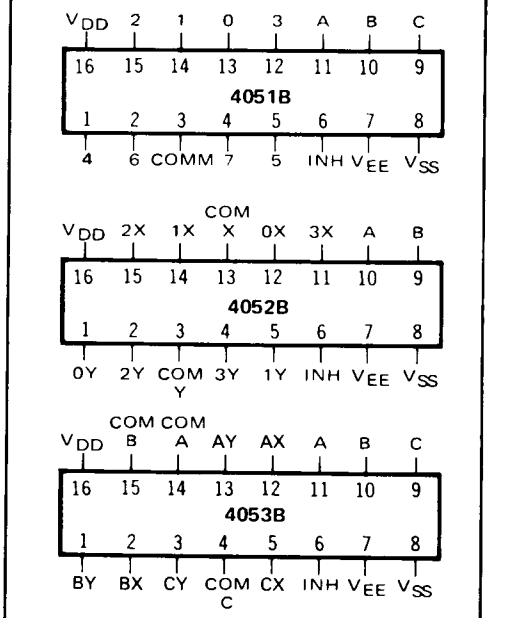
4051B is a Single 8-Channel Multiplexer having three binary Control inputs, A, B, and C, and an Inhibit input. The three binary signals select 1 of 8 channels to be turned ON and connect the input to the output.

4052B is a Differential 4-Channel Multiplexer having two binary Control inputs, A and B, and an Inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

4053B is a Triple 4-Channel Multiplexer having three separate digital Control inputs, A, B, and C and an Inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

When the devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminal(s) is (are) the input(s).

CONNECTION DIAGRAMS
(all packages)



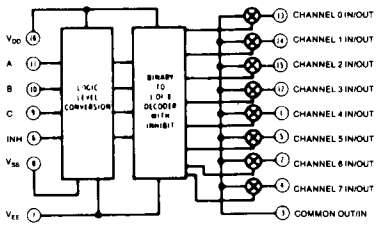
RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

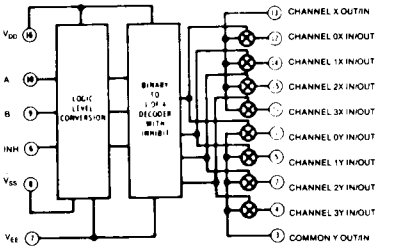
DC Supply Voltage	V_{DD} - V_{SS}	3 to 15	Vdc
	V_{DD} - V_{EE}	3 to 15	Vdc
Operating Temperature	T_A		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

NOTE: There are no restrictions on the relative magnitudes of V_{SS} and V_{EE}, providing Absolute Maximum Ratings are observed.

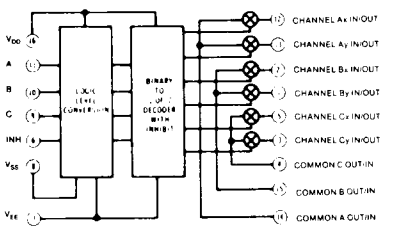
LOGIC DIAGRAMS



4051B
Single 8-Channel Multiplexer



4052B
Differential 4-Channel Multiplexer



4053B
Triple 2-Channel Multiplexer

TRUTH TABLE

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	4051	4052	4053
0	0	0	0	0	Ox, Oy	cx, bx, ax
0	0	0	1	1	1x, 1y	cx, bx, ay
0	0	1	0	2	2x, 2y	cx, by, ax
0	0	1	1	3	3x, 3y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

* = Don't care

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	V_{EE} (Vdc)	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	$V_{IN}=V_{SS}$ or V_{DD} All valid input combinations	0	+5	0	–	5	–	0.05	5	–	150	μAdc
			0	+10	0	–	10	–	0.1	10	–	300	
				+5	-5								
			0	+15	0	–	20	–	0.2	20	–	600	
				+7.5	-7.5								
MINIMUM INPUT HIGH VOLTAGE (Control and Inhibit Inputs)	V_{IH}	$V_{is}=V_{EE}$ $V_{os}=V_{DD}$ $I_{os}=10\mu A$	0 0 0	5 10 15	0 0 0	– – –	3.5 7.0 11.0	– – –	2.75 5.5 8.25	3.5 7.0 11.0	– – –	3.5 7.0 11.0	Vdc
MAXIMUM INPUT LOW VOLTAGE (Control and Inhibit Inputs)	V_{IL}	$V_{is}=V_{EE}$ $V_{os}=V_{DD}$ $I_{os}=10\mu A$	0 0 0	5 10 15	0 0 0	1.5 3.0 4.0	– – –	1.5 3.0 4.0	2.25 4.5 6.75	– – –	1.5 3.0 4.0	– – –	Vdc
SWITCH INPUT/ OUTPUT LEAKAGE Any channel OFF	I_{OFF}	$V_{IN}=V_{SS}$ or V_{DD} $V_{is}=\pm 7.5$Vdc	0	+7.5	-7.5	–	±100	–	±0.01	±100	–	± 1000	nAdc
All channels OFF	I_{OFF}	Inh = 7.5Vdc $V_{is}=\pm 7.5$Vdc	0	+7.5	-7.5								
		4051B				–	±400	–	±0.08	±400	–	±1000	nAdc
		4052B				–	±200	–	±0.04	±200	–	±1000	
		4053B				–	±100	–	±0.02	±100	–	±1000	
ON-RESISTANCE	R_{ON}	$V_{IN}=V_{SS}$ or V_{DD}	-7.5	+7.5	-7.5								
		$V_{EE} \leq V_{is} \leq V_{DD}$	0	+15	0	–	220	–	125	280	–	400	Ω
		$R_L=10k\Omega$	-5	+5	-5	–	310	–	180	400	–	590	Ω
			0	+10	0								
			-2.5	+2.5	-2.5	–	2000	–	470	2500	–	3500	Ω
			0	+5	0								
ON-RESISTANCE MATCH (Same Package)	ΔR_{ON}	$V_{IN}=V_{SS}$ or V_{DD}	-7.5	+7.5	-7.5	–	–	–	5	–	–	–	Ω
		$V_{EE} \leq V_{is} \leq V_{DD}$	0	+15	0								
		$R_L=10k\Omega$	-5	+10	-5	–	–	–	10	–	–	–	Ω
			0	+10	0								
			-2.5	+2.5	-2.5	–	–	–	50	–	–	–	Ω
			0	+5	0								

NOTES: [1] Remaining Static Characteristics are listed under "4000B Series Family Specifications".

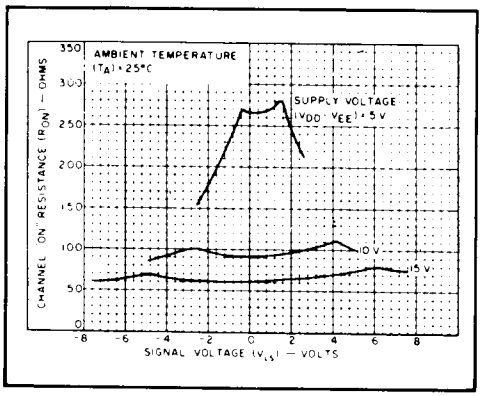
[2] T_{LOW} = -55°C for C, D, F, H device.
= -40°C for E device.
T_{HIGH} = +125°C for C, D, F, H device.
= + 85°C for E device.

ELECTRICAL CHARACTERISTICS (Continued)

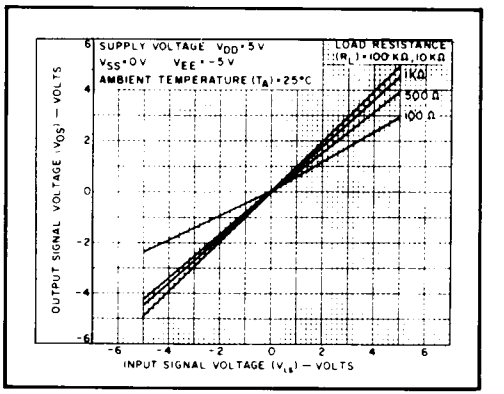
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		CONDITIONS	V_{SS} (Vdc)	V_{DD} (Vdc)	V_{EE} (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})									
PROPAGATION DELAY TIME Signal Input to Signal Output	t_{PLH} t_{PHL}	Inh = V_{SS} V_{IN}=V_{SS} or V_{DD} V_{is}= Square Wave R_L = 10kΩ	0 0 0	5 10 15	0 0 0	– – –	30 15 12.5	60 30 25	ns
BANDWIDTH (-3dB) (Sine Wave)	BW	Inh = V_{SS} R_L V_{IN} = V_{SS} 1kΩ or V_{DD} 10kΩ V_{is}=5V_{p-p} 100kΩ centered 1MΩ @ 0.0Vdc	0	+5	-5	– – – –	54 40 38 37	– – – –	MHz
INSERTION LOSS (= 20 $\log_{10} \frac{V_{os}}{V_{is}}$)		Inh = V_{SS} R_L V_{IN}=V_{SS} 1kΩ or V_{DD} 10kΩ V_{is}=5V_{p-p} 100kΩ centered 1MΩ @ 0.0Vdc	0	+5	-5	– – – –	2.3 0.2 0.1 0.05	– – – –	dB
SIGNAL DISTORTION (Sine Wave)		Inh = V_{SS} V_{IN} = V_{SS} or V_{DD} V_{is} = 5V_{p-p} centered @ 0.0Vdc f_{is} = 1.0kHz R_L = 10kΩ	-7.5 -5 -2.5	+7.5 +5 +2.5	-7.5 -5 -2.5	– – –	0.1 0.2 1.0	– – –	%
FEEDTHROUGH (-40dB)		Inh = V_{SS} R_L V_{IN}=V_{SS} 1kΩ or V_{DD} 10kΩ V_{is}=5V_{p-p} 100kΩ centered 1MΩ @0.0Vdc	0	+5	-5	– – – –	1250 140 18 2	– – – –	kHz
CROSSTALK (-40dB) Between two switches		Inh = V_{SS} V_{IN}= V_{SS} or V_{DD} V_{is}= 5V_{p-p} centered @ 0.0Vdc R_L = 1.0kΩ	0	+5	-5	–	1.0	–	MHz
CAPACITANCE Input	C_{is}	Inh = V_{DD}	0	+5	-5	–	5	–	pF
Common	C_{os}	4051B 4052B 4053B	0	+5	-5	– – –	30 18 10	– – –	pF
Feedthrough	C_{ios}		0	+5	-5	–	0.2	–	pF
CONTROL INPUTS									
PROPAGATION DELAY TIME[1] Turn on	t_{PLH}, t_{PHL}	Inh = V_{SS} $V_{EE} \leq V_{is} \leq V_{DD}$ R_L = 10kΩ	0 0 0 0 -2.5 0	+7.5 +15 +5 +10 +2.5 +5	-7.5 0 -5 0 -2.5 0	– – – – – –	160 120 225 160 400 360	320 240 450 320 800 720	ns
INHIBIT INPUT									
PROPAGATION DELAY TIME Turn on	t_{PLH}, t_{PHL}	V_{IN} =V_{SS} or V_{DD} V_{is} = V_{DD} R_L = 10kΩ	0 0 0 0 -2.5 0	+7.5 +15 +5 +10 +2.5 +5	-7.5 0 -5 0 -2.5 0	– – – – – –	160 120 200 160 400 360	320 240 400 320 800 720	ns
INHIBIT RECOVERY TIME[2]	t_{rel}	V_{IN}=V_{SS} or V_{DD} $V_{EE} \leq V_{is} \leq V_{DD}$ R_L = 10kΩ	0 0 0 0 -2.5 0	+7.5 +15 +5 +10 +2.5 +5	-7.5 0 -5 0 -2.5 0	– – – – – –	150 80 200 105 300 225	300 160 400 210 600 450	ns

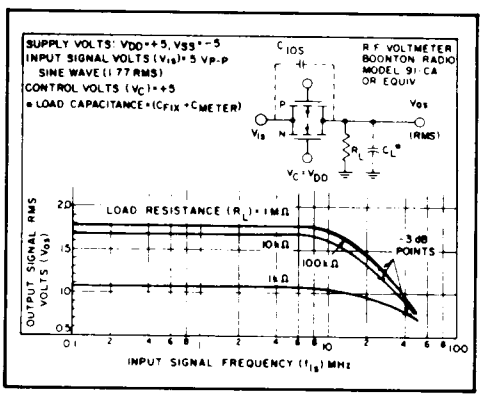
Notes: [1] Channel Overlap time — interval following change of control input during which two channels may be ON simultaneously.
[2] Interval following removal of Inhibit during which channel information is invalid.



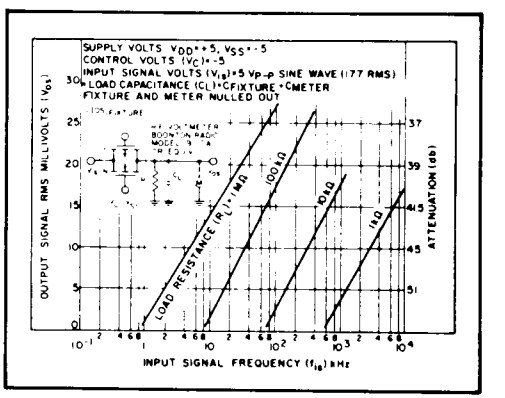
Typical Channel "ON" resistance vs. signal voltage



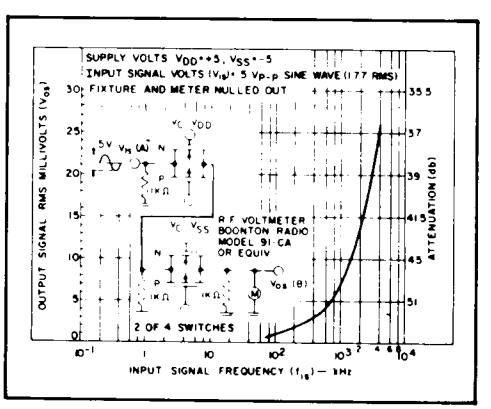
Typical "ON" characteristics



Typ. switch frequency response-switch "ON"



Typ. feedthru vs. freq. – switch "OFF"



Typ. crosstalk between switch circuits in the same package

SCHEMATIC DIAGRAM
OF ONE SWITCH