**Integrated Circuit Systems, Inc.**

# ICS95V857I

# 2.5V Industrial Temperature Wide Range Frequency Clock Driver (45MHz - 233MHz)

**Recommended Application:**
- DDR Memory Modules / Zero Delay Board Fan Out
- Provides complete DDR registered DIMM solution with ICSSSTVF16857, ICSSSTVF16859 or ICSSSTV32852

**Product Description/Features:**
- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution (SSTL_2)
- Feedback pins for input to output synchronization
- PD# for power management
- Spread Spectrum-tolerant inputs
- Auto PD when input signal removed
- Industrial temperature (-40°C to +85°C) compliant

**Specifications:**
- Meets or exceeds JEDEC standard #82-1 for registered DDR clock driver
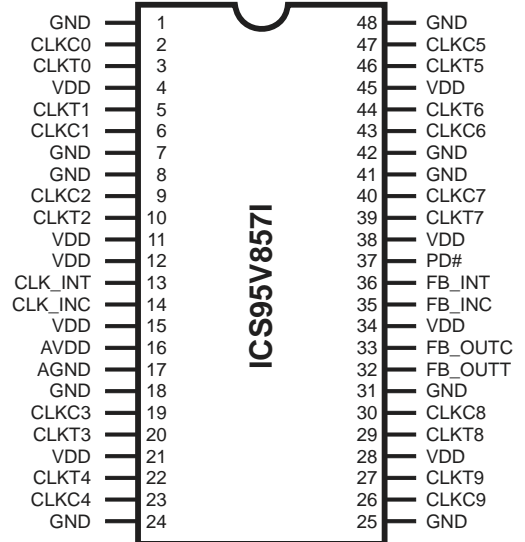- Covers all DDR1 speed grades

**Switching Characteristics:**
- CYCLE - CYCLE jitter: <60ps
- OUTPUT - OUTPUT skew: <60ps
- Period jitter: ±30ps
- DUTY CYCLE: 49.5% - 50.5%

## Pin Configuration



| | | | | |
|---|---|---|---|---|
| GND | 1 | | 48 | GND |
| CLKC0 | 2 | | 47 | CLKC5 |
| CLKT0 | 3 | | 46 | CLKT5 |
| VDD | 4 | | 45 | VDD |
| CLKT1 | 5 | | 44 | CLKT6 |
| CLKC1 | 6 | | 43 | CLKC6 |
| GND | 7 | | 42 | GND |
| GND | 8 | | 41 | GND |
| CLKC2 | 9 | | 40 | CLKC7 |
| CLKT2 | 10 | | 39 | CLKT7 |
| VDD | 11 | | 38 | VDD |
| VDD | 12 | | 37 | PD# |
| CLK_INT | 13 | | 36 | FB_INT |
| CLK_INC | 14 | | 35 | FB_INC |
| VDD | 15 | | 34 | VDD |
| AVDD | 16 | | 33 | FB_OUTC |
| AGND | 17 | | 32 | FB_OUTT |
| GND | 18 | | 31 | GND |
| CLKC3 | 19 | | 30 | CLKC8 |
| CLKT3 | 20 | | 29 | CLKT8 |
| VDD | 21 | | 28 | VDD |
| CLKT4 | 22 | | 27 | CLKT9 |
| CLKC4 | 23 | | 26 | CLKC9 |
| GND | 24 | | 25 | GND |

**48-Pin TSSOP/TVSOP**

6.10 mm Body, 0.50 mm Pitch = TSSOP
4.40 mm Body, 0.40 mm Pitch = TVSOP

## Block Diagram



## Functionality

| INPUTS | | | | OUTPUTS | | | | PLL State |
|---|---|---|---|---|---|---|---|---|
| AVDD | PD# | CLK_INT | CLK_INC | CLKT | CLKC | FB_OUTT | FB_OUTC | |
| GND | H | L | H | L | H | L | H | Bypassed/off |
| GND | H | H | L | H | L | H | L | Bypassed/off |
| 2.5V (nom) | L | L | H | Z | Z | Z | Z | off |
| 2.5V (nom) | L | H | L | Z | Z | Z | Z | off |
| 2.5V (nom) | H | L | H | L | H | L | H | on |
| 2.5V (nom) | H | H | L | H | L | H | L | on |
| 2.5V (nom) | X | <20MHz)[1] | | Z | Z | Z | Z | off |
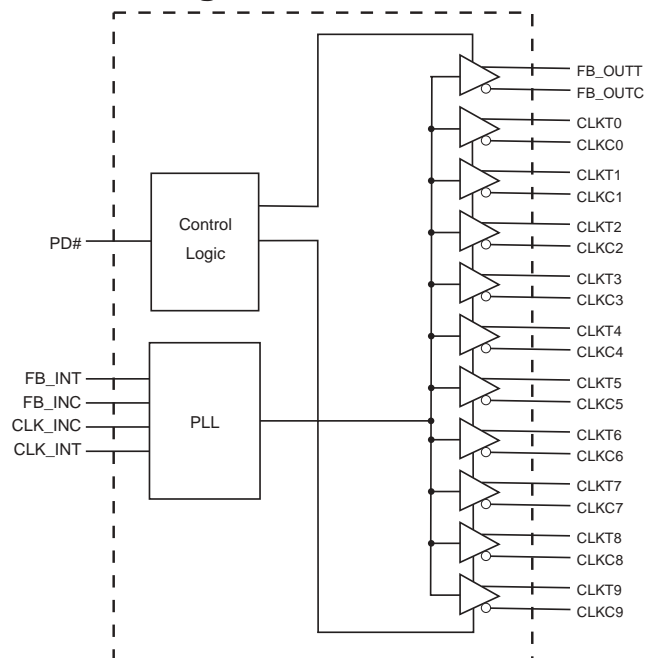
## Pin Configuration
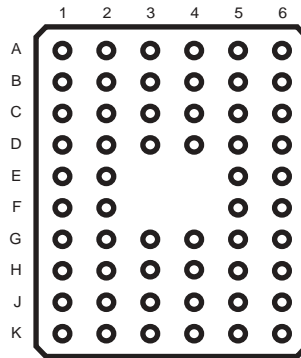


**56-Ball BGA**

|   | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | CLKT0 | CLKC0 | GND | GND | CLKC5 | CLKT5 |
| B | CLKC1 | CLKT1 | VDD | VDD | CLKT6 | CLKC6 |
| C | GND | GND | NC | NC | GND | GND |
| D | CLKT2 | CLKC2 | NC | NC | CLKC7 | CLKT7 |
| E | VDD | VDD | NB | NB | VDD | PD# |
| F | CLK_INT | CLK_INC | NB | NB | FB_INC | FB_INT |
| G | VDD | AVDD | NC | NC | FB_OUTC | VDD |
| H | AGND | GND | NC | NC | GND | FB_OUTT |
| J | CLKC3 | CLKT3 | VDD | VDD | CLKT8 | CLKC8 |
| K | CLKT4 | CLKC4 | GND | GND | CLKC9 | CLKT9 |
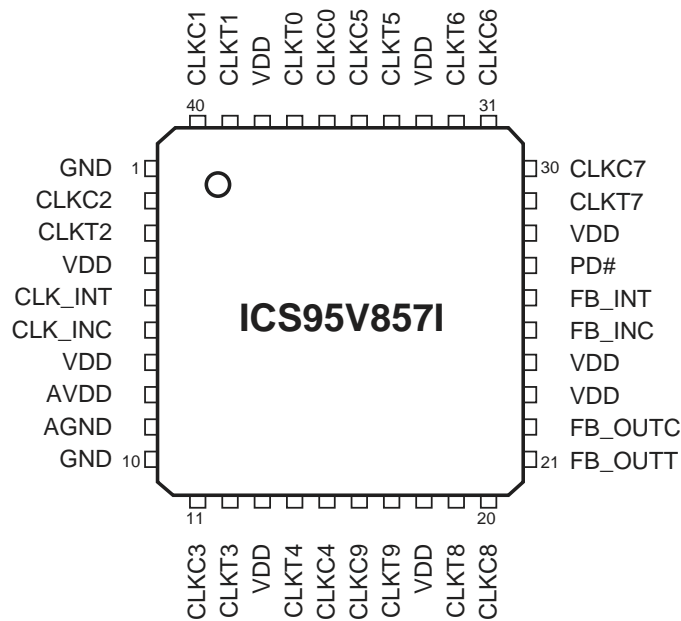


**40-Pin MLF**

## Pin Descriptions

| PIN NAME | TYPE | DESCRIPTION |
|---|---|---|
| VDD | PWR | Power supply, 2.5V |
| GND | PWR | Ground |
| AVDD | PWR | Analog power supply, 2.5V |
| AGND | PWR | Analog ground |
| CLKT(9:0) | OUT | "True" Clock of differential pair outputs |
| CLKC(9:0) | OUT | "Complementary" clocks of differential pair outputs |
| CLK_INC | IN | "Complementary" reference clock input |
| CLK_INT | IN | "True" reference clock input |
| FB_OUTC | OUT | "Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC |
| FB_OUTT | OUT | "True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT |
| FB_INT | IN | "True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error |
| FB_INC | IN | "Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error |
| PD# | IN | Power Down. LVCMOS input |

This PLL Clock Buffer is designed for a $V_{DD}$ of 2.5V, an $AV_{DD}$ of 2.5V and differential data input and output levels.

The **ICS95V857I** is a zero delay buffer that distributes a differential clock input pair (CLK_INC, CLK_INT) to ten differential pair of clock outputs (CLKT[0:9], CLKC[0:9]) and one differential pair feedback clock output (FB_OUT, FB_OUTC). The clock outputs are controlled by the input clocks (CLK_INC, CLK_INT), the feedback clocks (FB_INT, FB_INC), the 2.5-V LVCMOS input (PD#) and the Analog Power input ($AV_{DD}$). When input (PD#) is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are tri-stated. When $AV_{DD}$ is grounded, the PLL is turned off and bypassed for test purposes.

When the input frequency is less than the operating frequency of the PLL, appproximately 20MHz, the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as when the (PD#) input is low. When the input frequency increases to greater than approximately 20 MHz, the PLL will be turned back on, the inputs and outputs will be enabled and PLL will obtain phase lock between the feedback clock pair (FB_INT, FB_INC) and the input clock pair (CLK_INC, CLK_INT).

The PLL to the **ICS95V857I** clock driver uses the input clocks (CLK_INC, CLK_INT) and the feedback clocks (FB_INT, FB_INC) provide high-performance, low-skew, low-jitter, output differential clocks (CLKT[0:9], CLKC[0:9]). The **ICS95V857I** is also able to track Spread Spectrum Clock (SSC) for reduced EMI.

The **ICS95V857I** is characterized for operation from -40°C to 85°C.

# ICS95V857I

## Absolute  Maximum  Ratings

Supply Voltage (VDD & AVDD). . . . . . . . . . . -0.5V to 4.6V
Logic Inputs . . . . . . . . . . . . . . . . . . . . . . . GND −0.5 V to  $V_{DD}$ + 0.5 V
Ambient Operating Temperature . . . . . . . . . . -40°C to +85°C
Storage Temperature . . . . . . . . . . . . . . . . . . −65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = -40 - 85°C; Supply Voltage $A_{VDD}$, $V_{DD}$ = 2.5 V +/- 0.2V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Current | $I_{IH}$ | $V_I$ = $V_{DD}$ or GND | 5 | | | μA |
| Input Low Current | $I_{IL}$ | $V_I$ = $V_{DD}$ or GND | | | 5 | μA |
| Operating Supply Current | $I_{DD2.5}$ | $C_L$ = 0pf @ 200MHz | | | 148 | mA |
| | $I_{DDPD}$ | $C_L$ = 0pf | | | 100 | μA |
| High Impedance Output Current | $I_{OZ}$ | $V_{DD}$ = 2.7V, Vout = $V_{DD}$ or GND | | | ±10 | mA |
| Input Clamp Voltage | $V_{IK}$ | $V_{DD}$ = 2.3V Iin = -18mA | | | -1.2 | V |
| High-level output voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | $V_{DD}$ - 0.1 | | | V |
| | | $I_{OH}$ = -12 mA | 1.7V | | | V |
| Low-level output voltage | $V_{OL}$ | $I_{OL}$ =1 mA | | | 0.1 | V |
| | | $I_{OH}$ =12 mA | | | 0.6 | V |
| Input Capacitance[1] | $C_{IN}$ | $V_I$ = GND or $V_{DD}$ | 2.5 | | 3.5 | pF |

[1]Guaranteed by design at 233MHz, not 100% tested in production.

## Recommended Operating Condition (see note1)

$T_A$ = -40 - 85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$, $A_{VDD}$ | | 2.3 | 2.5 | 2.7 | V |
| Low level input voltage | $V_{IL}$ | CLKT, CLKC, FB_INC | | 0.4 | $V_{DD}/2 - 0.18$ | V |
| | | PD# | -0.3 | | 0.7 | V |
| High level input voltage | $V_{IH}$ | CLKT, CLKC, FB_INC | $V_{DD}/2 + 0.18$ | 2.1 | | V |
| | | PD# | 1.7 | | $V_{DD} + 0.6$ | V |
| DC input signal voltage (note 2) | $V_{IN}$ | | -0.3 | | $V_{DD} + 0.3$ | V |
| Differential input signal voltage (note 3) | $V_{ID}$ | DC - CLKT, FB_INT | 0.36 | | $V_{DD} + 0.6$ | V |
| | | AC - CLKT, FB_INT | 0.7 | | $V_{DD} + 0.6$ | V |
| Output differential cross-voltage (note 4) | $V_{OX}$ | | $V_{DD}/2 - 0.15$ | | $V_{DD}/2 + 0.15$ | V |
| Input differential cross-voltage (note 4) | $V_{IX}$ | | $V_{DD}/2 - 0.2$ | $V_{DD}/2$ | $V_{DD}/2 + 0.2$ | V |
| High level output current | $I_{OH}$ | | | | -6.4 | mA |
| Low level output current | $I_{OL}$ | | | | 5.5 | mA |
| Operating free-air temperature | $T_A$ | | -40 | | 85 | °C |

**Notes:**
1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VT is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of $V_{DD}$ and is the voltage at which the differential signal must be crossing.

## Timing Requirements

$T_A$ = -40 - 85°C; Supply Voltage $A_{VDD}$, $V_{DD}$ = 2.5 V +/- 0.2V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Max clock frequency | $freq_{op}$ | 2.5V±0.2V @ 25°C | 45 | 233 | MHz |
| Application Frequency Range | $freq_{App}$ | 2.5V±0.2V @ 25°C | 95 | 210 | MHz |
| Input clock duty cycle | $d_{tin}$ | | 40 | 60 | % |
| CLK stabilization | $T_{STAB}$ | | | 15 | µs |

## Switching Characteristics (see note 3)

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Low-to high level propagation delay time | $t_{PLH}$[1] | CLK_IN to any output | | 5.5 | | ns |
| High-to low level propagation delay time | $t_{PLL}$[1] | CLK_IN to any output | | 5.5 | | ns |
| Output enable time | $t_{EN}$ | PD# to any output | | 5 | | ns |
| Output disable time | tdis | PD# to any output | | 5 | | ns |
| Period jitter | $T_{jit (per)}$ | 100MHz to 200MHz | -30 | | 30 | ps |
| Half-period jitter | t(jit_hper) | 100MHz to 200MHz | -75 | | 30 | ps |
| Input clock slew rate | $t_{sl(i)}$ | | 1 | | 4 | V/ns |
| Output clock slew rate | $t_{sl(o)}$ | | 1 | | 2.5 | V/ns |
| Cycle to Cycle Jitter[1] | $T_{cyc}$-$T_{cyc}$ | 100MHz to 200MHz | | | 60 | ps |
| Phase error | $t_{(phase error)}$[4] | | -50 | 0 | 50 | ps |
| Output to Output Skew | $T_{skew}$ | | | | 60 | ps |

**Notes:**
1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=$t_{wH}$/$t_c$, where the cycle ($t_c$) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.

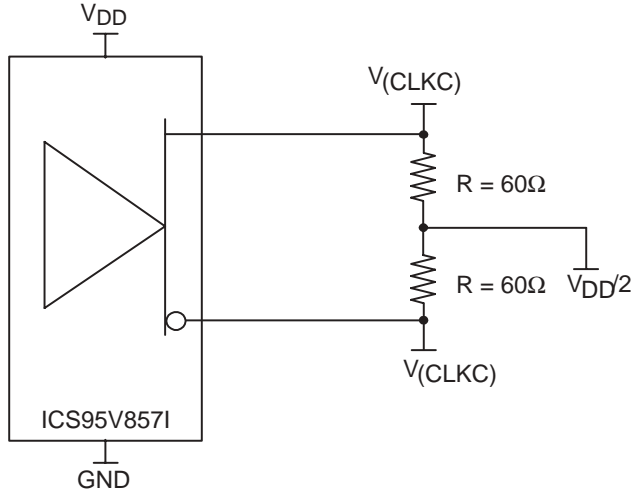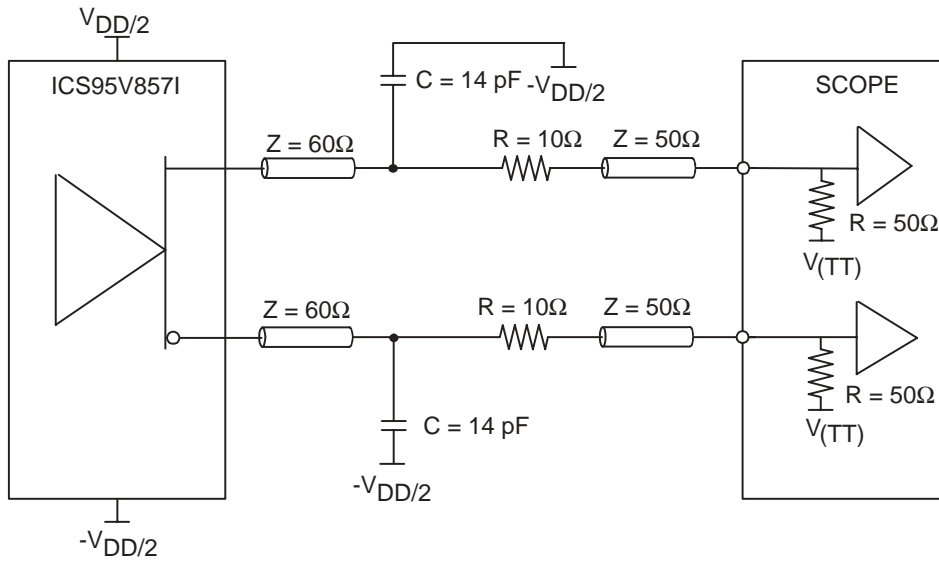**Parameter Measurement Information**



**Figure 1. IBIS Model Output Load**



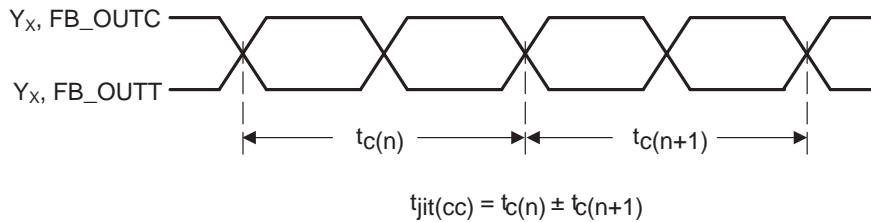NOTE: $V_{(TT)} = GND$

**Figure 2. Output Load Test Circuit**



$$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$$

**Figure 3. Cycle-to-Cycle Jitter**

**Parameter Measurement Information**

CLK_INC

CLK_INT

FB_INC

FB_INT

$t_{(\emptyset)}$ n

$t_{(\emptyset)}$ n+1

$$t_{(\emptyset)} = \frac{\sum_{1}^{n = N} t_{(\emptyset)\, n}}{N}$$

(N is a large number of samples)

**Figure 4. Static Phase Offset**

$Y_X\#$

$Y_X$

$Y_X$, FB_OUTC

$Y_X$, FB_OUTT

$t_{(SK\_O)}$

**Figure 5. Output Skew**

$Y_X$, FB_OUTC

$Y_X$, FB_OUTT

$Y_X$, FB_OUTC

$Y_X$, FB_OUTT

$\frac{1}{f_O}$

$t_{(jit\_per)} = t_{C(n)} - \frac{1}{f_O}$
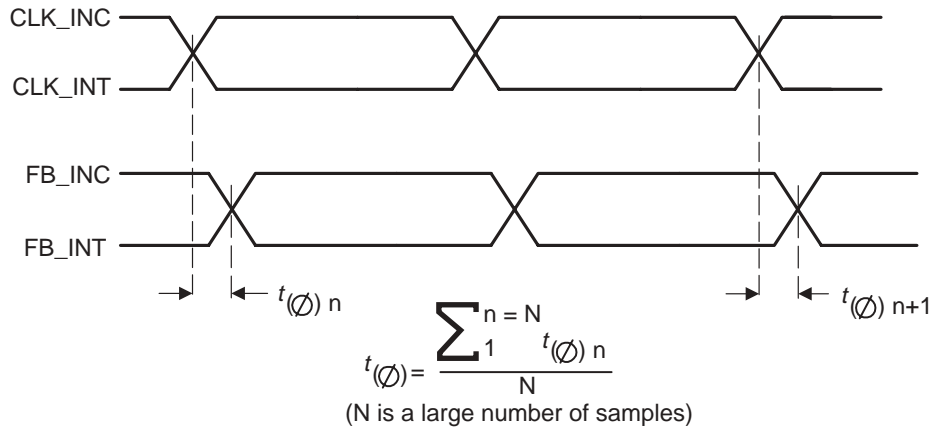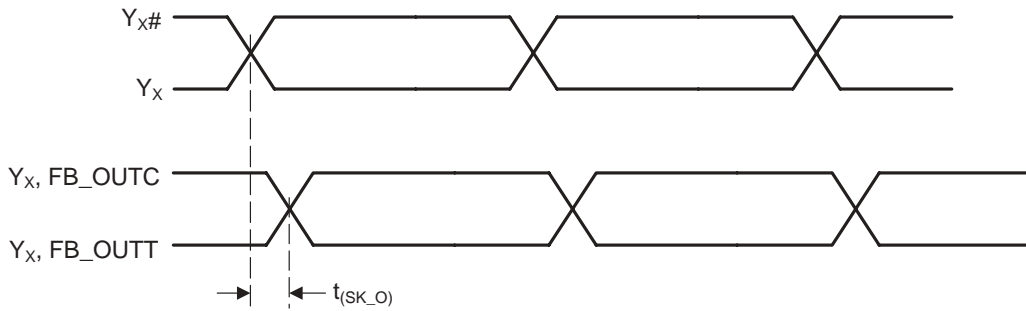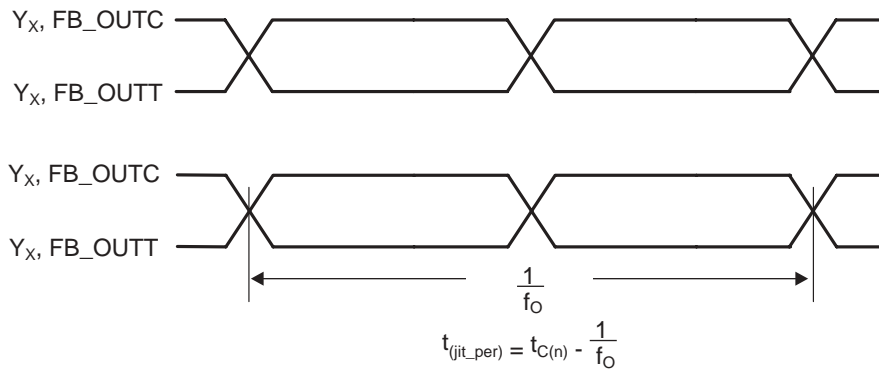
**Figure 6. Period Jitter**

**Parameter Measurement Information**



$$t_{(jit\_Hper)} = t_{(jit\_Hper\_n)} - \frac{1}{2xf_O}$$
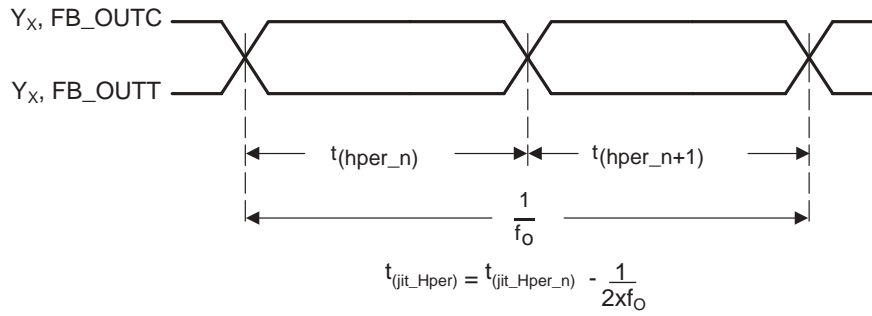
**Figure 7. Half-Period Jitter**
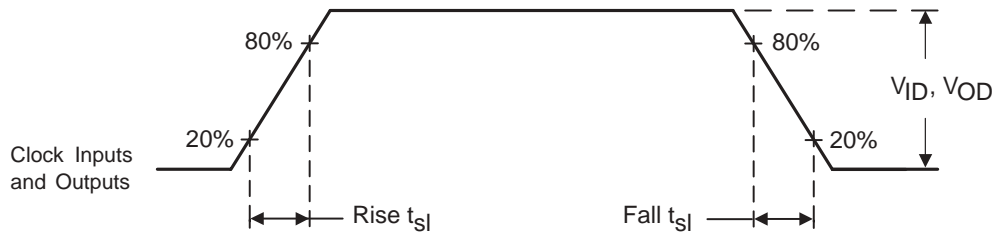


**Figure 8. Input and Output Slew Rates**

# ICS95V857I

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 48 | 12.40 | 12.60 | .488 | .496 |

Reference Doc.: JEDEC Publication 95, M O-153

10-0039
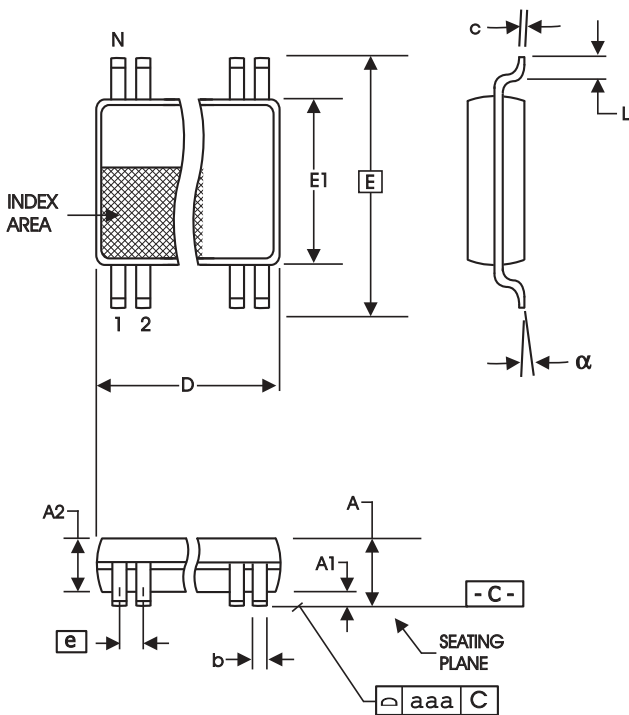
**6.10 mm. Body, 0.50 mm. pitch TSSOP**
**(240 mil)      (0.020 mil)**

## Ordering Information

**ICS XXXX y G LF- T**

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

Example:

**ICS95V857AGIT**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.13 | 0.23 | .005 | .009 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | .169 | .177 |
| e | 0.40 BASIC | | 0.016 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.08 | -- | .003 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 48 | 9.60 | 9.80 | .378 | .386 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0037

**4.40 mm. Body, 0.40 mm. pitch TSSOP**

**(173 mil)**        **(16 mil)**

## Ordering Information

**ICS XXXX y L LF- T**

**Designation for tape and reel packaging**

**Lead Free (Optional)**

**Package Type**
L = TSSOP (TVSOP)

**Revision Designator** (will not correlate with datasheet revision)

**Device Type**

**Prefix**
ICS = Standard Device
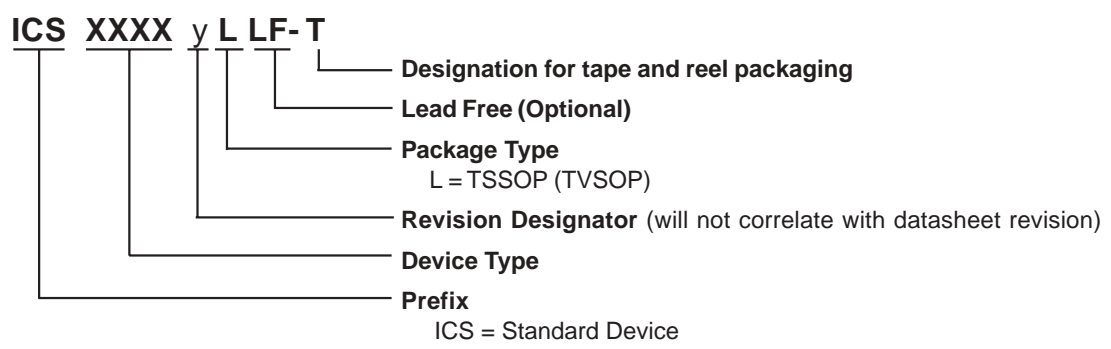
Example:

**ICS95V857ALIT**
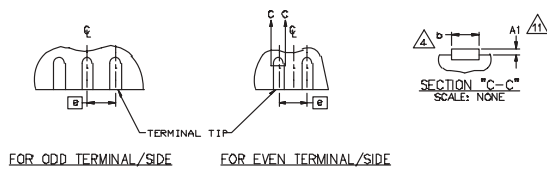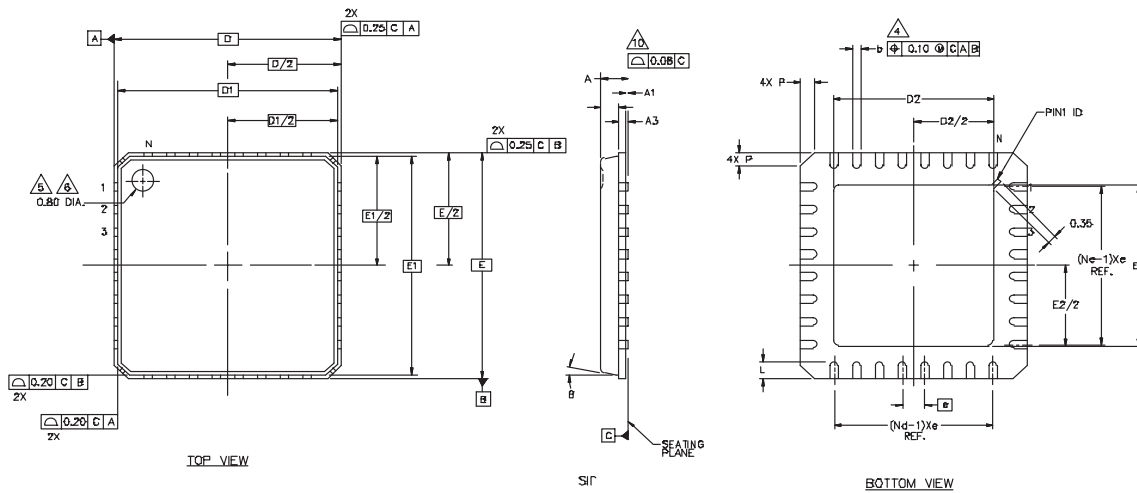
**40-Pin MLF**

| Symbol | Common Dimensions | | |
|---|---|---|---|
| A | - | 0.85 | 0.90 |
| A1 | 0.00 | 0.01 | 0.05 |
| A2 | - | 0.65 | 0.80 |
| A3 | 0.20 REF | | |
| D | 6.00 BSC | | |
| D1 | 5.75 BSC | | |
| E | 6.00 BSC | | |
| E1 | 5.75 BSC | | |
| Q | | | 12 |
| P | 0.24 | 0.42 | 0.60 |
| R | 0.13 | 0.17 | 0.23 |
| **Pitch Varation D** | | | |
| e | 0.50 BSC | | |
| N | 40 | | |
| Nd | 10 | | |
| Ne | 10 | | |
| L | 0.30 | 0.40 | 0.50 |
| b | 0.18 | 0.23 | 0.30 |
| Q | 0.00 | 0.20 | 0.45 |
| D2 | 2.75 | 2.90 | 3.05 |
| E2 | 2.75 | 2.90 | 3.05 |

# Ordering Information

**ICS XXXX y K LF-T**

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  K = MLF
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

Example:

**ICS95V857AKIT**
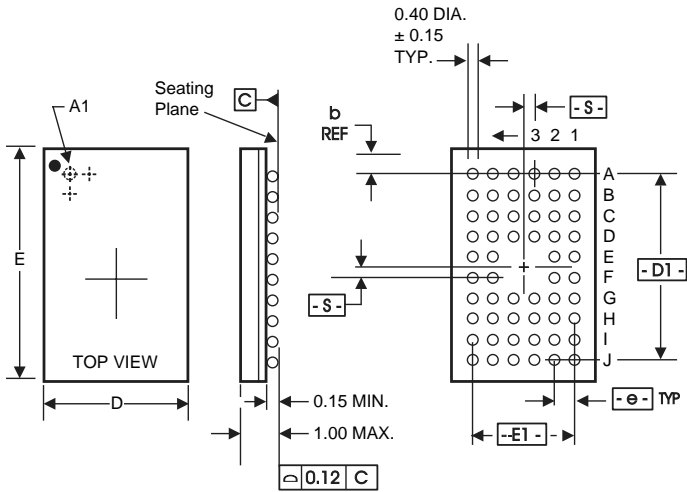
| SYMBOL | MIN. | NOM. | MAX. |
|--------|------|------|------|
| A | 0.86 | 0.93 | 1.00 |
| A1 | 0.15 | 0.18 | 0.21 |
| A2 | 0.71 | 0.75 | 0.79 |
| D | 4.40 | 4.50 | 4.60 |
| E | 6.90 | 7.00 | 7.10 |
| I | 0.625 REF. | | |
| J | 0.575 REF. | | |
| M | 6X10 | | |
| aaa | | | 0.10 |
| bbb | | | 0.10 |
| ccc | | | 0.10 |
| b | 0.35 | 0.40 | 0.45 |
| e | 0.65 TYP. | | |

## Ordering Information

**ICS XXXX y H LF- T**

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  H = BGA
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

Example:

**ICS95V857AHIT**

0820A—08/02/04