



# 3.3V CMOS 18-BIT UNIVERSAL BUS TRANS- CEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16500

## FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{sk(0)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of - 40°C to + 85°C
- $V_{cc} = 3.3V \pm 0.3V$ , Normal Range
- $V_{cc} = 2.7V$  to 3.6V, Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin

## Drive Features for ALVCH16500:

- High Output Drivers: ±24mA
- Suitable for heavy loads

## APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

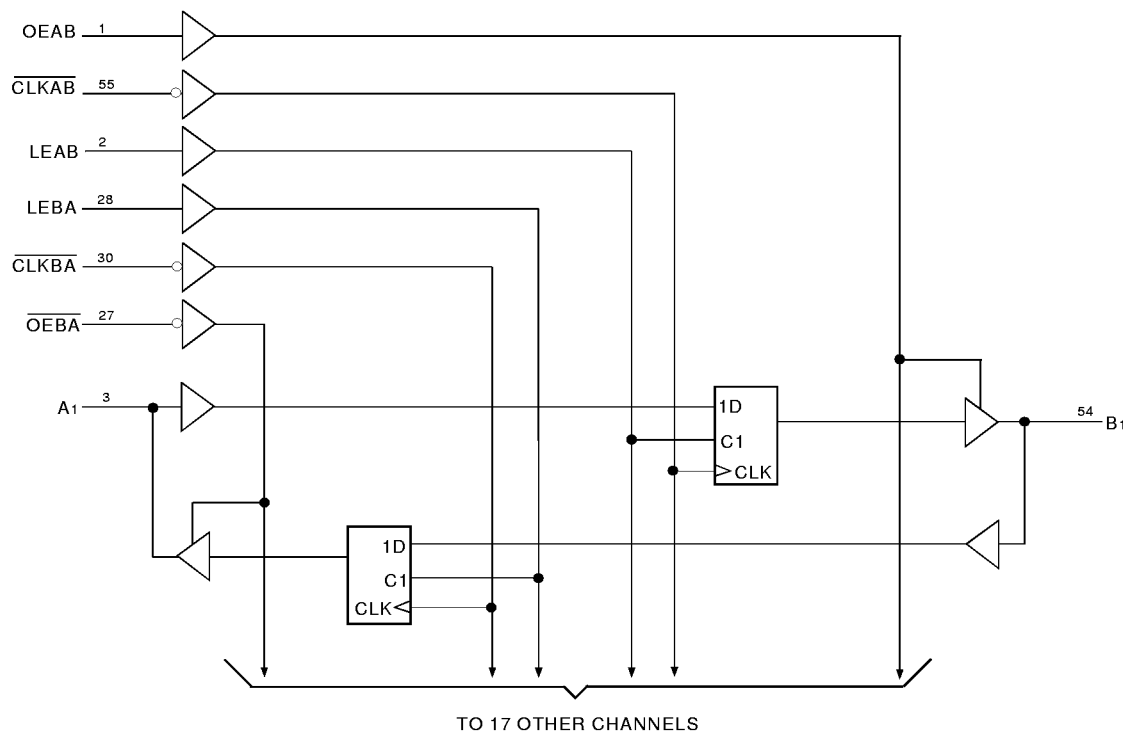
## DESCRIPTION:

This 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. Data flow in each direction is controlled by output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ), latch enable ( $\overline{LEAB}$  and  $\overline{LEBA}$ ) and clock ( $\overline{CLKAB}$  and  $\overline{CLKBA}$ ) inputs. For A-to-B data flow, the device operates in transparent mode when  $\overline{LEAB}$  is high. When  $\overline{LEAB}$  is LOW, the A data is latched if  $\overline{CLKAB}$  is held at a high or low logic level. If  $\overline{LEAB}$  is LOW, the A bus data is stored in the latch/flip-flop on the high-to-low transition of  $\overline{CLKAB}$ .  $\overline{OEAB}$  performs the output enable function on the B port. Data flow from B port to A port is similar but requires using  $\overline{OEBA}$ ,  $\overline{LEBA}$  and  $\overline{CLKBA}$ . Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The ALVCH16500 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16500 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

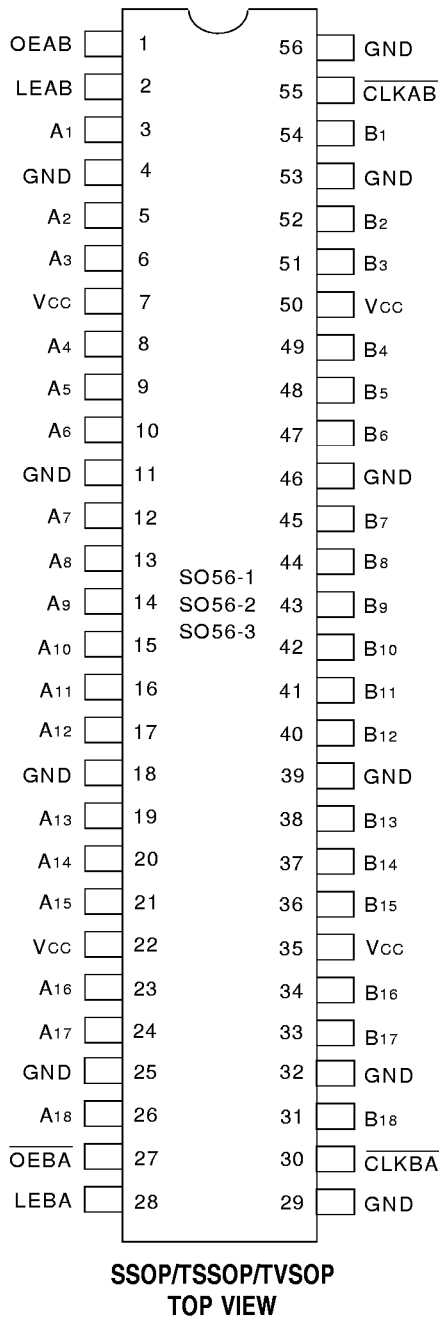
## Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

APRIL 1999

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V <sub>TERM</sub> (2)	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
V <sub>TERM</sub> (3)	Terminal Voltage with Respect to GND	- 0.5 to V <sub>CC</sub> + 0.5	V
T <sub>STG</sub>	Storage Temperature	- 65 to + 150	°C
I <sub>OUT</sub>	DC Output Current	- 50 to + 50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	± 50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	- 50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A <sub>x</sub>	A-to-B Data Inputs or B-to-A 3-State Outputs <sup>(1)</sup>
B <sub>x</sub>	B-to-A Data Inputs or A-to-B 3-State Outputs <sup>(1)</sup>

### NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

### NOTE:

- As applicable to the device type.

## FUNCTION TABLE (1, 2)

Inputs				Output
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	L or H	X	B <sub>0</sub> <sup>(3)</sup>

### NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses  $\overline{OEBA}$ ,  $\overline{LEBA}$ , and  $\overline{CLKBA}$ .
2. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
↓ = HIGH-to-LOW Transition
3. Output level before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = - 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = V <sub>CC</sub>	—	—	± 5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = GND	—	—	± 5	
I <sub>OZH</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = V <sub>CC</sub>	—	—	± 10	μA
I <sub>OZL</sub>			V <sub>O</sub> = GND	—	—	± 10	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = - 18mA		—	- 0.7	- 1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V		—	0.1	40	μA
I <sub>CC</sub>		V <sub>IN</sub> = GND or V <sub>CC</sub>					
I <sub>CC</sub>							
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	750	μA

### NOTE:

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

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### BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3.0V	V <sub>I</sub> = 2.0V	- 75	—	—	μA
			V <sub>I</sub> = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	- 45	—	—	μA
			V <sub>I</sub> = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	± 500	μA

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**NOTES:**

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

### OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = - 0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = - 6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = - 12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3.0V		2.4	—	
		V <sub>CC</sub> = 3.0V	I <sub>OH</sub> = - 24mA	2	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3.0V	I <sub>OL</sub> = 24mA	—	0.55	

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**NOTE:**

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = - 40°C to + 85°C.

## OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	V <sub>CC</sub> = 2.5V ± 0.2V	V <sub>CC</sub> = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C <sub>L</sub> = 0pF, f = 10MHz	40	51	pF
CPD	Power Dissipation Capacitance Outputs disabled		6	6	pF

## SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>MAX</sub>		150	—	150	—	150	—	MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ax to Bx or Bx to Ax	1	5.1	—	4.7	1	3.9	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEBA to Ax or LEAB to Bx	1	5.9	—	5.5	1	4.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{\text{CLKBA}}$ to Ax or $\overline{\text{CLKAB}}$ to Bx	1	6.6	—	6.6	1.1	5.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{\text{OEBA}}$ to Ax	1	6.2	—	6.2	1	5.2	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OEAB to Bx	1	5.7	—	5.4	1	4.6	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{\text{OEBA}}$ to Ax	1	5.4	—	4.6	1	4.3	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OEAB to Bx	1	6.1	—	5.7	1.5	5	ns
t <sub>SU</sub>	Set-up Time, HIGH or LOW, Ax to $\overline{\text{CLKAB}}$ or Bx to $\overline{\text{CLKBA}}$	1.7	—	1.4	—	1.3	—	ns
t <sub>H</sub>	Hold Time, HIGH or LOW, Ax to CLKAB or Bx to $\overline{\text{CLKBA}}$	1.7	—	1.6	—	1.3	—	ns
t <sub>SU</sub>	Set-up Time, HIGH or LOW, Ax to LEAB or Bx to LEBA	$\overline{\text{CLK}}$ LOW	1.9	—	1.6	—	1.4	ns
		$\overline{\text{CLK}}$ HIGH	1.1	—	1	—	1	ns
t <sub>H</sub>	Hold Time, HIGH or LOW, Ax to LEAB or Bx to LEBA	$\overline{\text{CLK}}$ LOW	1.6	—	1.5	—	1.2	ns
		$\overline{\text{CLK}}$ HIGH	2	—	1.8	—	1.5	ns
t <sub>w</sub>	Pulse Width, LE HIGH	3.3	—	3.3	—	3.3	—	ns
t <sub>w</sub>	Pulse Width, $\overline{\text{CLK}}$ HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t <sub>SK(o)</sub>	Output Skew <sup>(2)</sup>	—	—	—	—	—	500	ps

### NOTES:

1. See test circuits and waveforms.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .
2. Skew between any two outputs of the same package and switching in the same direction.

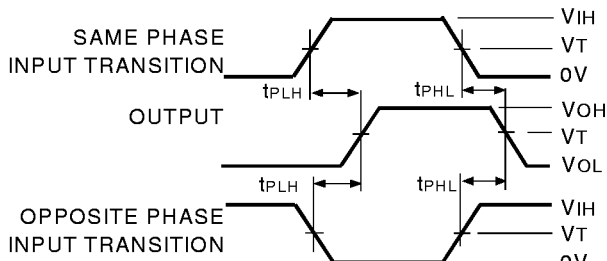
## TEST CIRCUITS AND WAVEFORMS:

### TEST CONDITIONS

Symbol	V <sub>cc</sub> (1)= 3.3V±0.3V	V <sub>cc</sub> (1)= 2.7V	V <sub>cc</sub> (2)= 2.5V±0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>cc</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>cc</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>cc</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF

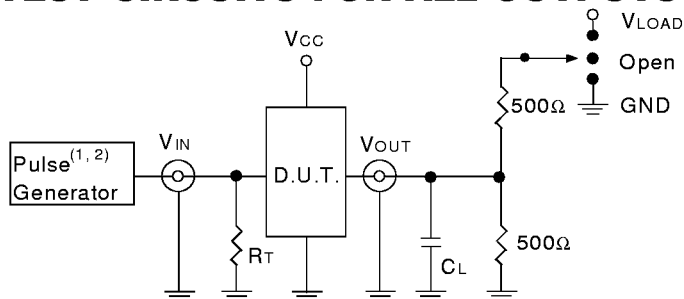
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### PROPAGATION DELAY



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### TEST CIRCUITS FOR ALL OUTPUTS



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#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

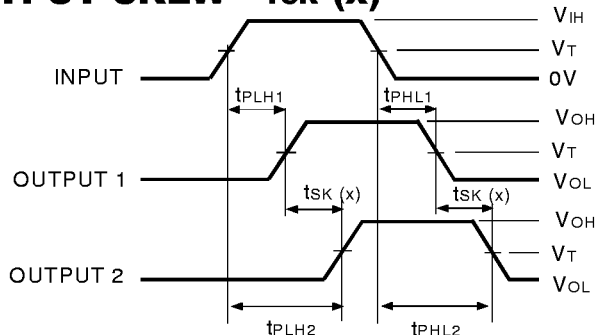
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other tests	Open

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### OUTPUT SKEW - t<sub>SK</sub>(x)



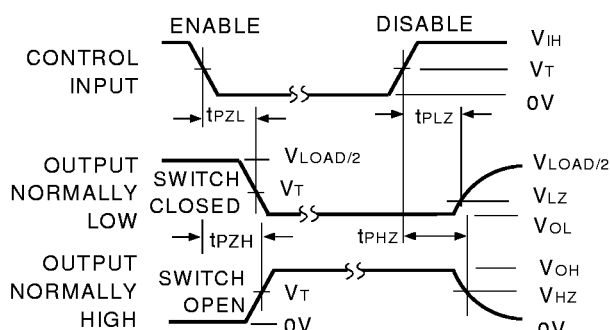
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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#### NOTES:

1. For t<sub>SK</sub>(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.

### ENABLE AND DISABLE TIMES

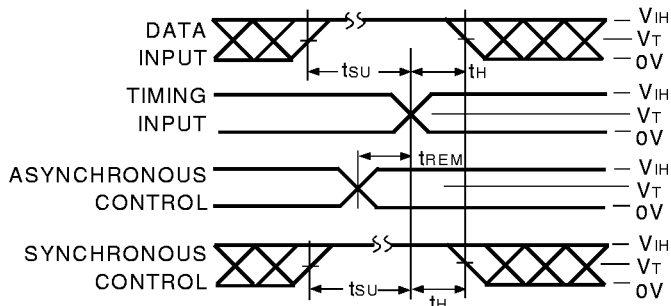


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#### NOTE:

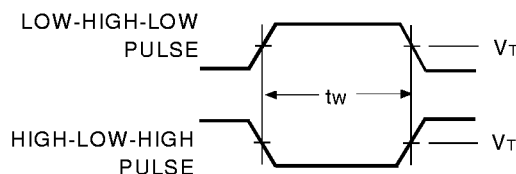
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SET-UP, HOLD, AND RELEASE TIMES



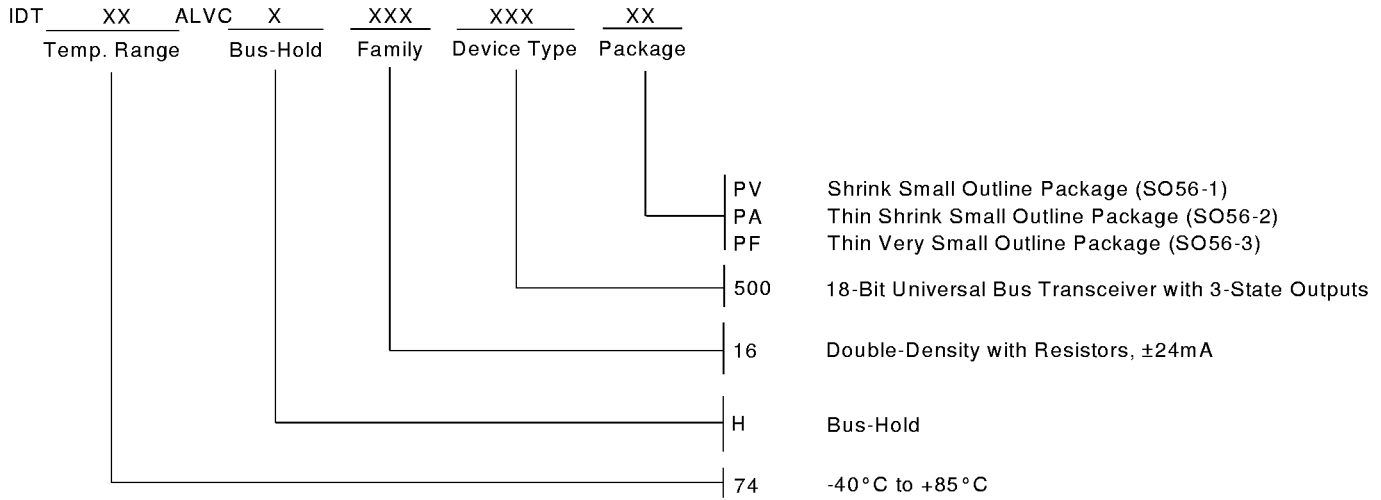
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### PULSE WIDTH



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