PRELIMINARY

PERICOM

PS381/PS383/PS385

Precision, 17V Analog Switches

Features

- Low On-Resistance (17Ω typ) Minimizes Distortion and Error Voltages
- Low Glitching Reduces Step Errors in Sample-and-Holds. Charge Injection, <1 pC typ
- Single Supply (+3V to +15V) or Split-Supply (±3V to±8V) Operation
- Improved Second Sources for MAX381/MAX383/MAX385
- On-Resistance Matching Between Channels, 0.2 Ω typ
- On-Resistance Flatness, <2 Ω typ
- Low Off-Channel Leakage, <2.5nA @+85°C
- TTL/CMOS Logic Compatible
- Rail-to-Rail Analog Signal Dynamic Range
- Low Power Consumption (<10µW)

Applications

- Instrumentation, ATE
- Sample-and-Holds
- Audio Switching and Routing
- Telecommunication Systems
- PBX, PABX
- Battery-Powered Systems

Description

The PS381/PS383/PS385 are improved high precision, medium voltage analog switches designed to operate with +3V to ±8V power supplies. The PS381 has two normally open (NO) switches.

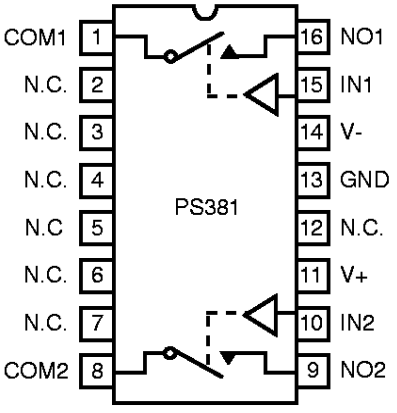
The PS383 is a dual, single-pole double-throw (SPDT) switch. The PS385 is a dual, double-pole single-throw (DPST) function. Each switch conducts current equally well in either direction when on. In the off state each switch blocks voltages up to the power-supply rails.

With +5V power supplies, the PS381/PS383/PS385 guarantee <35Ω on-resistance. On-resistance matching between channels is within 2Ω. On-resistance flatness is less than 4Ω over the specified range. All three devices guarantee low leakage currents (<200 pA @25°C, <2.5nA @+85°C) and fast switching speeds (t_{ON} < 175ns). Break-before-make switching action protects against momentary crosstalk (PS383).

These switches are fully specified for single +5V operation, with <65Ω R_{ON}, <2Ω R_{ON} match, and <6Ω R_{ON} flatness.

For operation below 5V the PI5A381A/PI5A383A/PI5A385A are also recommended.

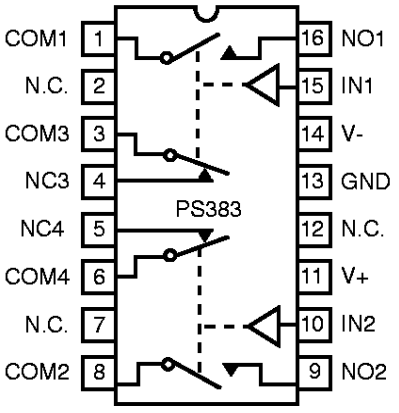
Functional Diagrams, Pin Configurations, and Truth Tables



Top View

N.C = No Connect.

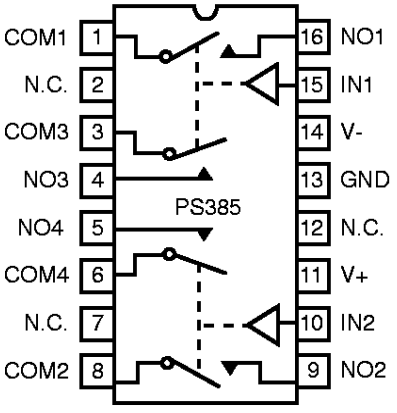
PS381	
Logic	Switch
0	OFF
1	ON



Top View

Switches shown for logic "0" input

PS383		
Logic	SW3, SW4	SW1, SW2
0	ON	OFF
1	OFF	ON



Top View

PS385	
Logic	Switch
0	OFF
1	ON

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Absolute Maximum Ratings

Voltages Referenced to V-

V+ ..... -0.3V to +17V

GND ..... -0.3V to +17V

V_{IN}, V_{COM}, V_{NC}, V_{NO} (Note 1) ..... (V-)-2V to (V+)+2V
or 30mA, whichever occurs first

Current (any terminal) 30mA

Peak Current, COM, NO, NC
(pulsed at 1ms, 10% duty cycle) 100mA

ESD per Method 3015.7 ..... >2000V

Thermal Information

Continuous Power Dissipation (T_A=+70°C)

Plastic DIP (derate 10.5mW/°C above +70°C) 800mW

Narrow SO (derate 8.7mW/°C above +70°C) 650mW

Storage Temperature ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Note 1: Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating

Caution: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Dual Supplies

(V± = ± 5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp. (°C)	Min(2)	Typ(1)	Max(2)	Units
Analog Switch							
Analog Signal Range (3)	V_{ANALOG}		Full	V-		V+	V
On Resistance	R_{ON}	V+ = 4.5V, V- = -4.5V, V_{NO} or V_{NC} = ±3.5V, I_{COM} = -10mA,	25		20	35	Ω
			Full			45	
On-Resistance Match Between Channels(4	ΔR_{ON}	V_{NO} or V_{NC} = ±3V, I_{COM} = -10mA, V+ = 5V, V- = -5V	25		0.5	2	
			Full			4	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{COM} = -10mA, V_{NO} or V_{NC} = ±3V, 0V	25			4	
			Full			6	
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ± 4.5V, V_{NC} or V_{NO} = ∓4.5V	25	-0.2	-0.01	0.2	nA
			Full	-2.5		2.5	
COM Off Leakage Current(6)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ± 4.5V, V_{NO} or V_{NC} = ∓4.5V	25	-0.2	-0.01	0.2	
			Full	-2.5		2.5	
COM On Leakage Current(7)	$I_{COM(ON)}$	V+ = 5.5V , V- = -5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ±4.5V	25	-0.4	-0.04	0.4	
			Full	-5		5	

Electrical Specifications - Dual Supplies (continued)

(V+=+5V±10%, GND=0V, V_{INH}=2.4V, V_{INL}=0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Logic Input							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V	Full	-1.0	0.005	1.0	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		-1.0	0.005	1.0	
Logic High Input Voltage	V_{AH}			2.4			V
Logic Low Input Voltage	V_{AL}					0.8	
Dynamic							
Turn-On Time	t_{ON}	V_{COM} = ±3V, Figure 2	25		100	175	ns
			Full			225	
Turn-Off Tim e	t_{OFF}		25		60	100	
			Full			150	
Break-Before-Make TimeDelay	t_D	PS383 only, Figure 3	25	10	20		
Charge Injection	Q	C_L=1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4	25		2	5	pC
Off Isolation(7)	OIRR	R_L = 100Ω, C_L= 5pF, f = 1MHz, Figure 5			72		dB
Crosstalk (8)	X_{TALK}	R_L = 50Ω, C_L= 5pF, f = 1MHz, Figure 6			90		
NC or NO Off Capacitance	$C_{(OFF)}$	f =1MHz, Figure 7			12		pF
COM Off Capacitance	$C_{COM(OFF)}$	f =1MHz, Figure 7			12		
COM On Capacitance	$C_{COM(ON)}$	f =1MHz, Figure 8			39		
Supply							
Power-Supply Range	V+, V-			±3		±8	V
Positive Supply Current	I+	V+ = 5.5V, V- = -5.5V, V_{IN} = 0V or V+, all channels on or off	Full	-1	0.06	1	µA
NegativeSupply Current	I-			-1	-0.01	1	

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = \Delta R_{ON}max - \Delta R_{ON}min$
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
7. Off Isolation = $20\log_{10} [V_{COM} / (V_{NO} or V_{NO})]$. See figure 5.
8. Between any two switches. See figure 6.
9. Leakage testing at single supply is guaranteed by testing with dual supplies.

Electrical Specifications - Single +5V Supply

(V+ = +5V ±10%, V- = 0V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min(1)	Typ(2)	Max(1)	Units
Analog Switch							
Analog Switch Range(3)	V_{ANALOG}			0V		V+	V
On-Resistance	R_{ON}	V+ = 5.0V, V- = 0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V,	25		25	65	Ω
			Full			75	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V	25		0.5	2	
			Full			4	
On-Resistance Flatness (5)	$R_{FLAT(ON)}$	V+ = 5V, V- = 0V I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V, 2V, 1V	25			6	
			Full			8	
NO or NC Off Leakage Current(9)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V- = 0V V_{COM} = 0V, V_{NO} or V_{NC} = 4.5V	25	-0.2	0.01	0.2	nA
			Full	-2.5		2.5	
COM Off Leakage Current(9)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, V_{NO} or V_{NC} = 0V	25	-0.2	0.01	0.2	
			Full	-2.5		2.5	
COM On Leakage Current(9)	$I_{COM(ON)}$	V_{COM} = 4.5V V_{NO} or V_{NC} = 4.5V V+ = 5.5V, V- = 0V	25	-0.4	-0.04	0.4	
			Full	-5		5	
Digital Logic Input							
Input Current with Input Voltage High	I_{INH}	V_{IN} =2.4V, all others =0.8V	Full	-1	0.005	1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} =0.8V, all others =2.4V		-1	0.005	1	
Dynamic							
Turn-On Time	t_{ON}	V_{COM} = 3V, Figure 2	25		160	250	ns
			Full			300	
Turn-Off Time	t_{OFF}		25		60	125	
			Full			175	
Break-Before-Make Time Delay(3)	t_D	PS383 only	25	10	20		
Charge Injection(3)	V_{CTE}	CL = 1nF, V_{GEN} = 0V, R_{GEN} =0VΩ, Figure 4	25		2	5	pC
Supply							
Power-Supply Range	V+			2.7		16	V
Positive Supply Current	I+	V+ = 5.5V, V_{IN} = 0V or V+, all channels on or off	Full	-1	0.01	1	µA
Negative Supply Current	I-		Full	-1	-0.01	1	

Electrical Specifications - Single +3.3V Supply

(V+ = +3V to 3.6V, GND = 0V, V_{NH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp°C	Min[2]	Typ[2]	Max[2]	Units
Analog Switch							
Analog Switch Range[3]	V_{ANALOG}		Full	0		V+	V
Channel On-Resistance	R_{ON}	V+ = 3V, V- = 0V I_{COM} = 1mA, V_{NO} or V_{NC} = 1.5V	25		75	185	Ω
			Full			250	
NO or NC Off Leakage Current[9]	$I_{NC(OFF)}$ or $I_{NC(OFF)}$	V_{COM} = 0V, V_{NO} or V_{NC} = 3V, V+ = 3.6V, V-= 0V	25	-0.2	-0.01	0.2	nA
			Full	-2.5		2.5	
COM Off Leakage Current[9]	$I_{COM(OFF)}$	V_{COM} =3V, V_{NO} or V_{NC} = 0V, V+ = 3.6V, V-= 0V	25	-0.2	-0.01	0.2	
			Full	-2.5		2.5	
COM On Leakage Current[9]	$I_{COM(ON)}$	V_{COM} =3V, V_{NO} or V_{NC} = 3V, V+ = 3.6V, V-= 0V	25	-0.4	-0.04	0.4	
			Full	-5		5	
Digital Logic Input							
Input Current with Input Voltage High	I_{INH}	V_{IN} =2.4V, all others = 0.8V	Full	-1	0.005	1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} =0.8V, all others = 2.4V		-1	0.005	1	
Dynamic							
Turn-On-Time[3]	t_{ON}	V_{COM} = 1.5V Figure 2	25			400	ns
Turn-Off-Time[3]	$t_{(OFF)}$	V_{COM} = 1.5V Figure 2	25			150	
Break-Before-Make Time Delay[3]	t_D	PS383 only	25	10	20		
Charge Injection[3]	Q	C_L = 1nF, V_{GEN} =0V, R_{GEN} =0Ω	25		1	5	pC
Supply							
Power-Supply Range	V+			2.7		16	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or V+, V+ =3.6V, V- = 0V	Full	-1	0.01	1	µA
Negative Supply Current	I-			-1	-0.01	1	

Test Circuits/Timing Diagrams

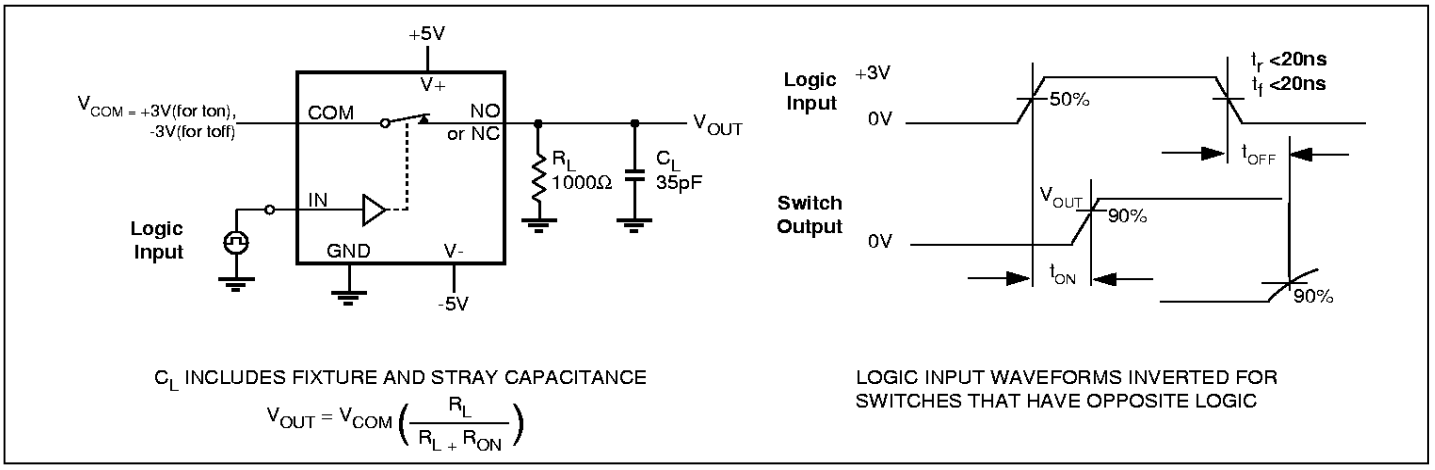

Figure 2. Switching Time

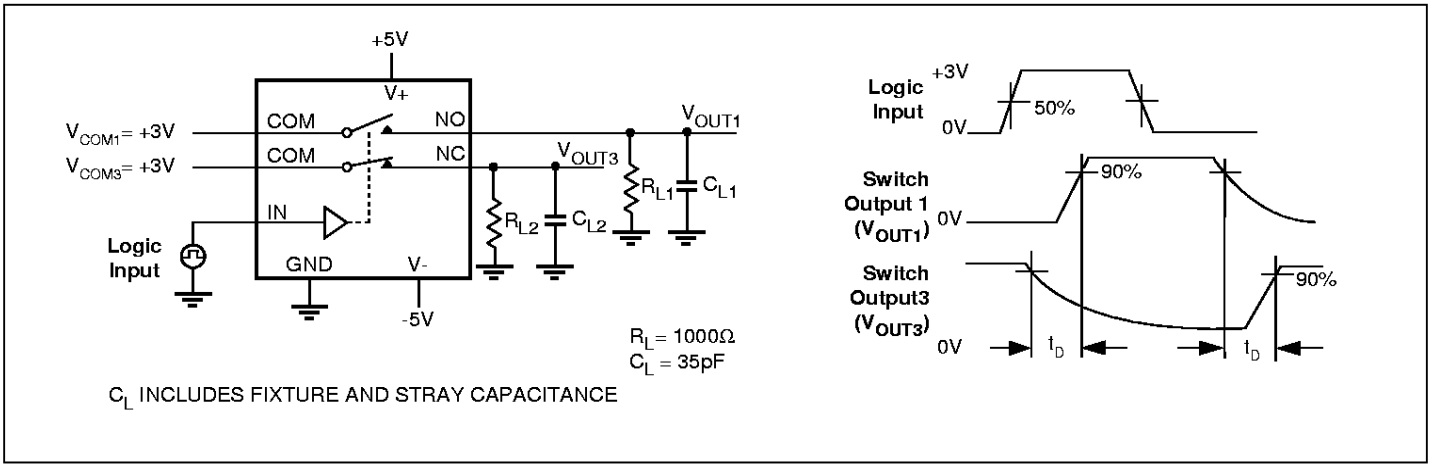

Figure 3. Break-Before-Make Interval (PS383 only)

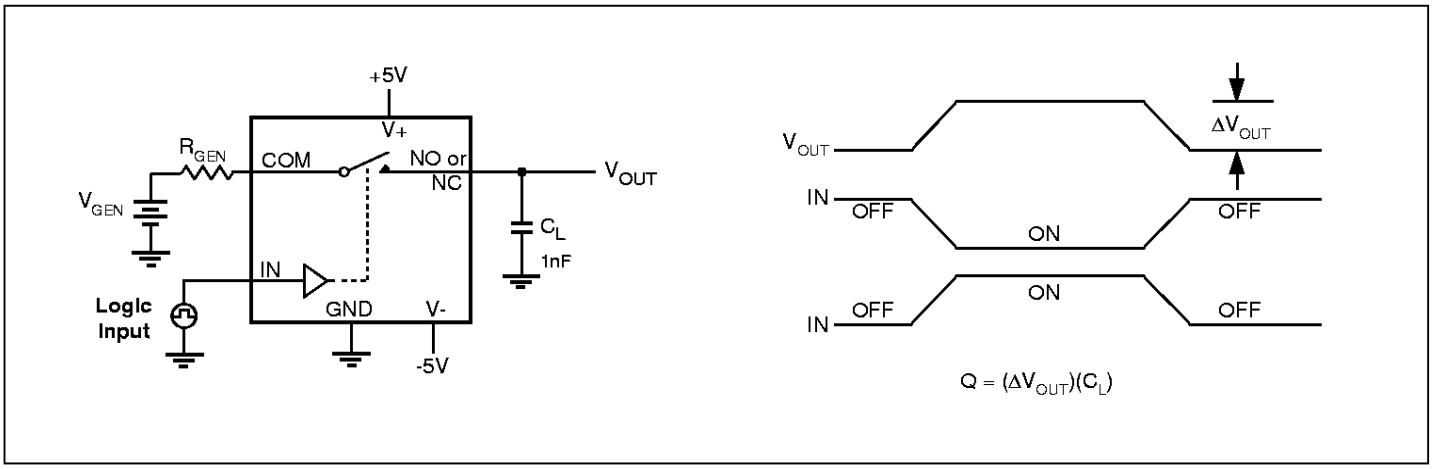

Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

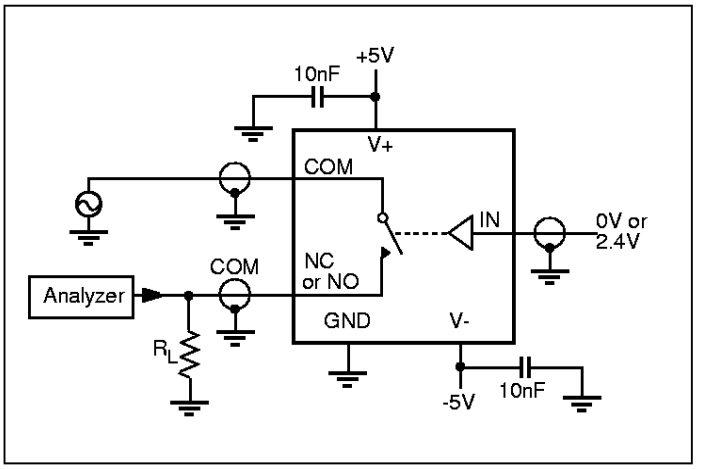

Figure 5. Off Isolation

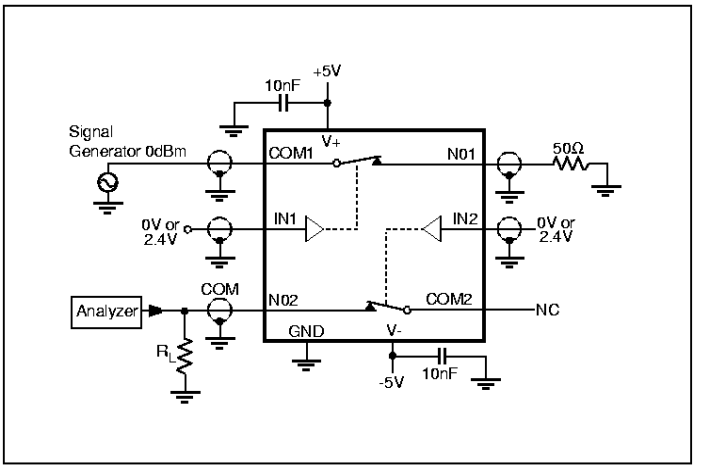

Figure 6. Crosstalk

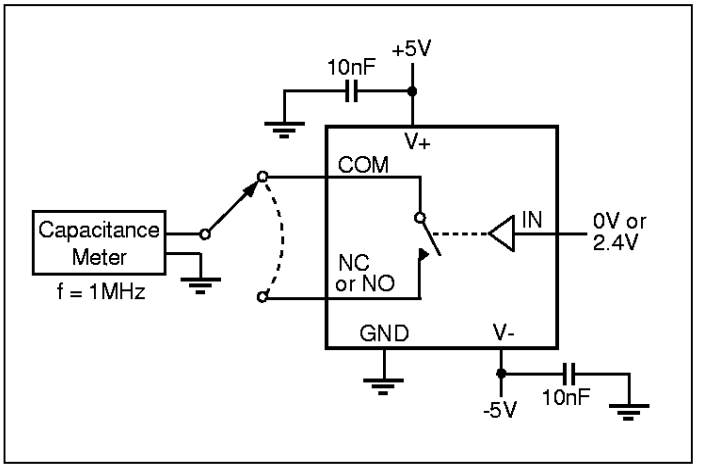

Figure 7. Channel-Off Capacitance

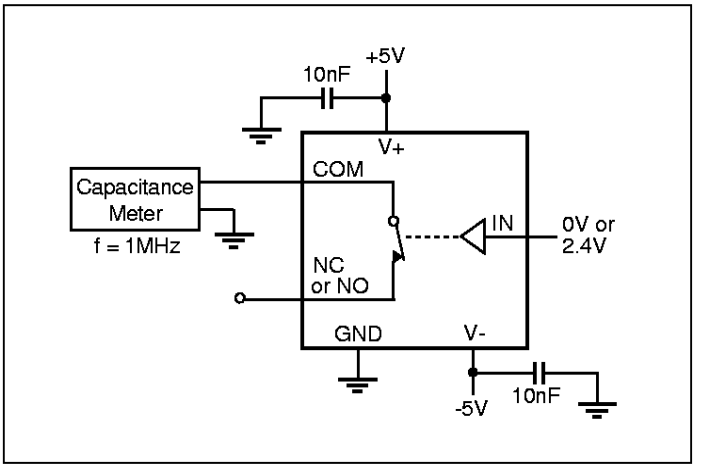

Figure 8. Channel-On Capacitance

Ordering Information

PART	Temp. Range	Package
PS381CPE	0°C to +70°C	16 Plastic DIP
PS381CSE	0°C to +70°C	16 Narrow SO
PS381EPE	-40°C to +85°C	16 Plastic DIP
PS381ESE	-40°C to +85°C	16 Narrow SO
PS383CPE	0°C to +70°C	16 Plastic DIP
PS383CSE	0°C to +70°C	16 Narrow SO
PS383EPE	-40°C to +85°C	16 Plastic DIP
PS383ESE	-40°C to +85°C	16 Narrow SO
PS385CPE	0°C to +70°C	16 Plastic DIP
PS385CSE	0°C to +70°C	16 Narrow SO
PS385EPE	-40°C to +85°C	16 Plastic DIP
PS385ESE	-40°C to +85°C	16 Narrow SO

Applications Information

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V-, and then logic inputs. If power-supply sequencing is not possible, add two small signal diodes or two current limiting resistors in series with the supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range, but low switch resistance and low leakage characteristics are unaffected.

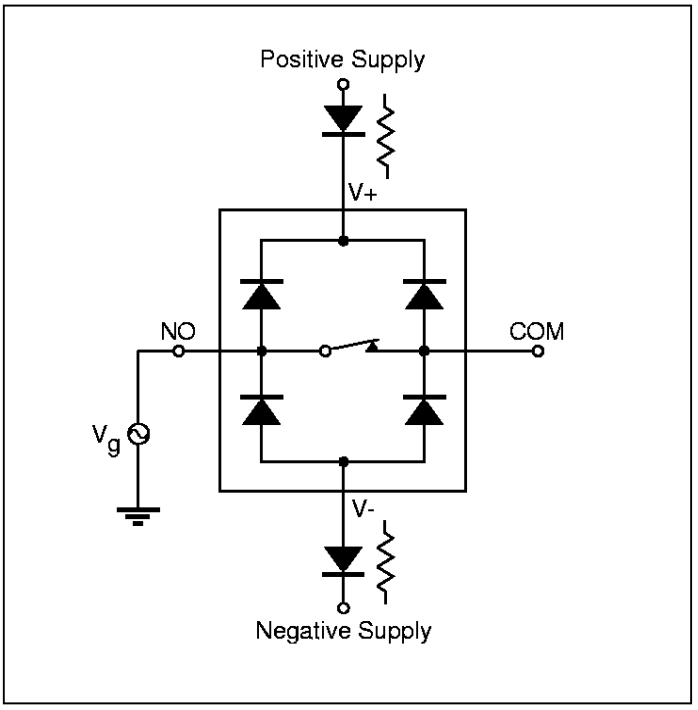

Figure 1. Overvoltage protection is accomplished using two external blocking diodes or two current limiting resistors.