3.3V CMOS 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16270

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of – 40°C to + 85°C
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- V_{CC} = 2.5V ± 0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16270:

- High Output Drivers: ±24mA
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

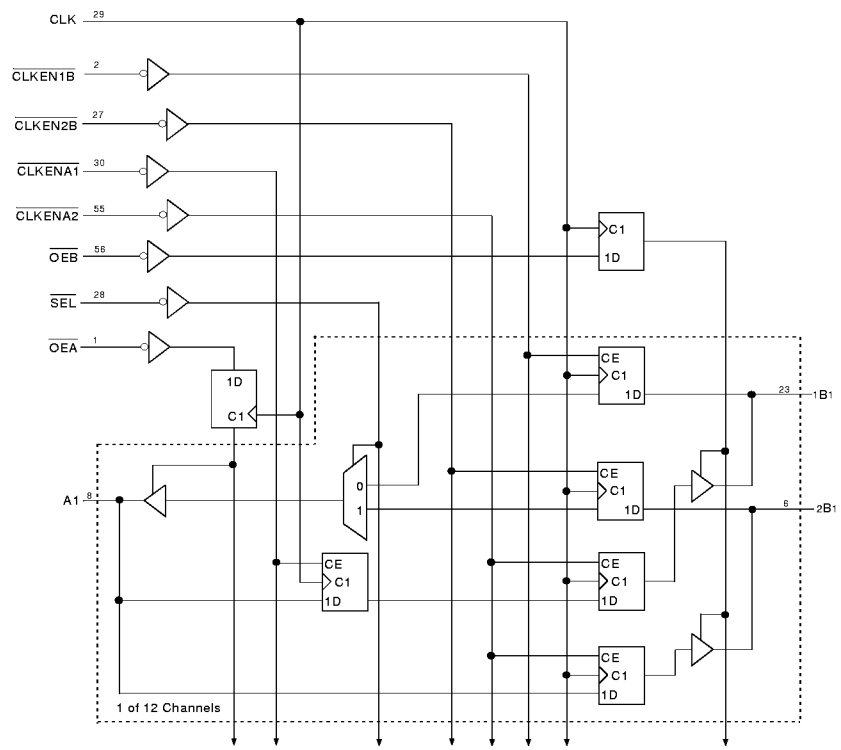
This registered bus exchanger is built using advanced dual metal CMOS technology. The ALVCH16270 is used in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

This device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{CLKEN}$) inputs are low. The select ($\overline{SEL}$) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of the $\overline{CLKENA}$ input allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B-port. Data flow is controlled by the active-low output enables ($\overline{OEA}$ and $\overline{OEB}$). The control terminals are registered to synchronize the bus-direction changes with CLK.

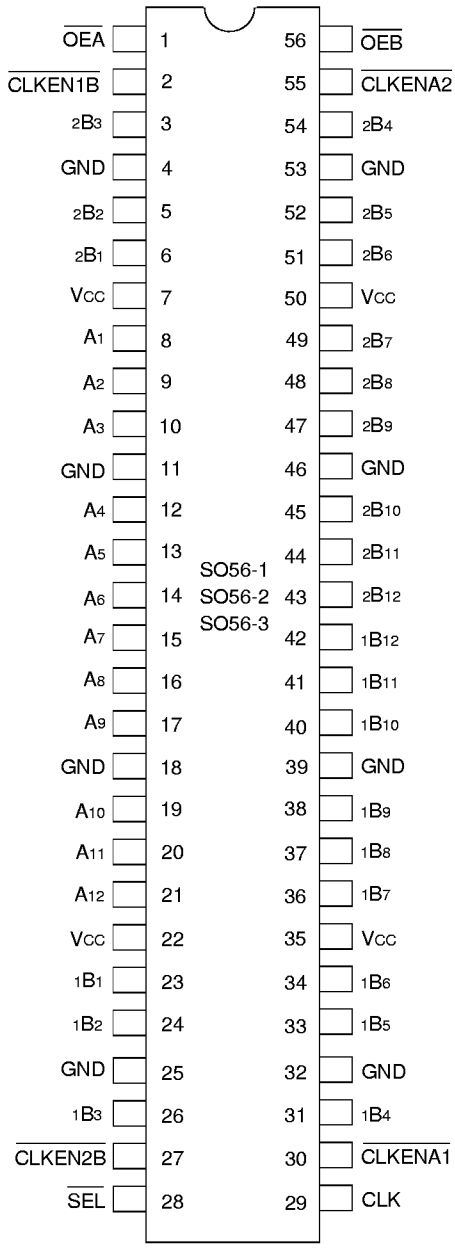
The ALVCH16270 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16270 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

FUNCTION TABLES(1)

OUTPUT ENABLE

Inputs			Outputs	
CLK	$\overline{OEA}$	$\overline{OEB}$	Ax	1Bx, 2Bx
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB}$ = L AND $\overline{OEA}$ = H)

Inputs				Outputs	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	Ax	1Bx	2Bx
L	H	↑	L	$1B_0$(2)	$2B_0$(2)
L	H	↑	H	$1B_0$(2)	$2B_0$(2)
L	L	↑	L	L(3)	L
L	L	↑	H	H(3)	H
H	L	↑	L	$1B_0$(4)	L
H	L	↑	H	$1B_0$(4)	H
H	H	X or ↑	X	$1B_0$(2)	$2B_0$(2)

B-TO-A STORAGE ($\overline{OEA}$ = L AND $\overline{OEB}$ = H)

Inputs						Outputs
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	$\overline{SEL}$	1Bx	2Bx	Ax
H	X	X	H	X	X	A_0(2)
X	H	X	L	X	X	A_0(2)
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition
2. Output level before the indicated steady-state input conditions were established.
3. Two CLK edges are needed to propagate data.
4. Data present at the output of the first register.

PIN DESCRIPTION

Pin Names	I/O	Description
$A_{X(1:12)}$	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.(1)
$_{1}B_{X(1:12)}$	I/O	Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory.(1)
$_{2}B_{X(1:12)}$	I/O	Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory.(1)
CLK	I	Clock Input
$\overline{CLKENA1}$	I	Clock Enable Input for the A-1B Register. If $\overline{CLKENA1}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).
$\overline{CLKENA2}$	I	Clock Enable Input for the A-2B Register. If $\overline{CLKENA2}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).
$\overline{CLKEN1B}$	I	Clock Enable Input for the 1B-A Register. If $\overline{CLKEN1B}$ is LOW during the rising edge of CLK, data will be clocked into register 1B-A (Active LOW).
$\overline{CLKEN2B}$	I	Clock Enable Input for the 2B-A Register. If $\overline{CLKEN2B}$ is LOW during the rising edge of CLK, data will be clocked into register 2B-A (Active LOW).
$\overline{SEL}$	I	1B or 2B Port Selection. When HIGH during the rising edge of CLK, $\overline{SEL}$ enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, $\overline{SEL}$ enables data transfer from 2B Port to A Port.
$\overline{OEA}$	I	Synchronous Output Enable for A Port (Active LOW)
$\overline{OEB}$	I	Synchronous Output Enable for B Port (Active LOW)

NOTE:
1. These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to V_{CC} + 0.5	V
T_{STG}	Storage Temperature	– 65 to + 150	°C
I_{OUT}	DC Output Current	– 50 to + 50	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	9	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	7	9	pF

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NOTE:
1. As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40° C to +85° C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	± 5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	± 5	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	± 10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	± 10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

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NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3.0V	V_I = 2.0V	– 75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	– 45	—	—	µA
I_{BHL}			V_I = 0.7V	45	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	± 500	µA
I_{BHLO}							

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NOTES:
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	Vcc = 2.5V ± 0.2V	Vcc = 3.3V ± 0.3V	Unit
			Typical	Typical	
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	87	120	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		80.5	118	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		150	—	150	—	150	—	Mhz
t_{PLH} t_{PHL}	Propagation Delay CLK to xBx	1.5	5.9		5.8	1.1	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay CLK to Ax	1.2	5.4		5.4	1	4.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{SEL}$ to Ax	1.4	6.2		6.4	1	5.5	ns
t_{PZH} t_{PZL}	Output Enable Time CLK to xBx	1.5	7		6.8	1	6	ns
t_{PZH} t_{PZL}	Output Enable Time CLK to Ax	1.5	7		6.8	1	6	ns
t_{PHZ} t_{PLZ}	Output Disable Time CLK to xBx	1.9	7.2		6.5	1.1	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time CLK to Ax	1.9	7.2		6.5	1.1	5.8	ns
t_{SU}	Set-Up Time, Ax data before CLK↑	4.1		3.8		3.1		ns
t_{SU}	Set-Up Time, Bx data before CLK↑	0.9		1.2		0.9		ns
t_{SU}	Set-Up Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK↑	3.5		3.2		2.7		ns
t_{SU}	Set-Up Time, $\overline{CLKEN1B}$ or $\overline{CLKEN2B}$ before CLK↑	3.4		3		2.6		ns
t_{SU}	Set-Up Time, $\overline{OEB}$ or $\overline{OEA}$ before CLK↑	4.4		3.9		3.2		ns
t_H	Hold Time, Ax data after CLK↑	0		0		0.2		ns
t_H	Hold Time, Bx data after CLK↑	1.4		1		1.7		ns
t_H	Hold Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK↑	0		0.1		0.3		ns
t_H	Hold Time, $\overline{CLKEN1B}$ or $\overline{CLKEN2B}$ after CLK↑	0		0		0.6		ns
t_H	Hold Time, $\overline{OEB}$ or $\overline{OEA}$ after CLK↑	0		0		0.1		ns
t_W	Pulse Width, CLK HIGH or LOW	3.3		3.3		3.3		ns
$t_{SK(o)}$	Output Skew(2)	—	—	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V±0.3V	$V_{CC}^{(1)}$= 2.7V	$V_{CC}^{(2)}$= 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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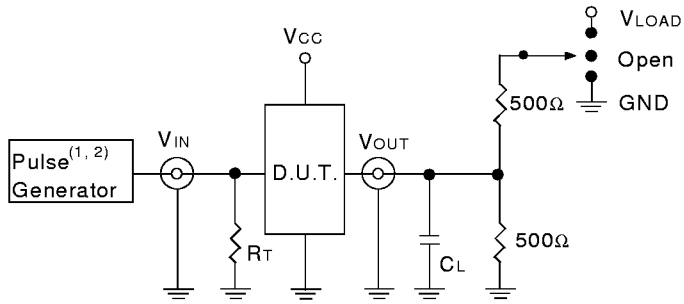
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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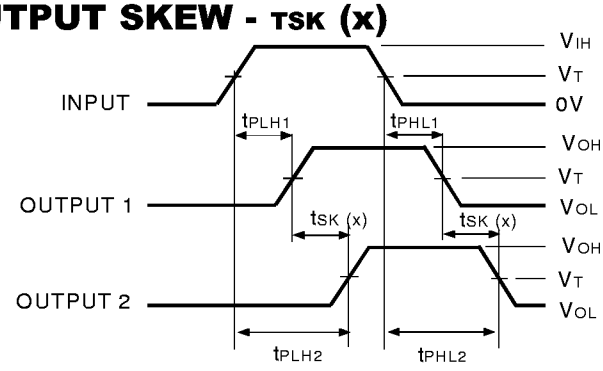
OUTPUT SKEW - t_{SK} (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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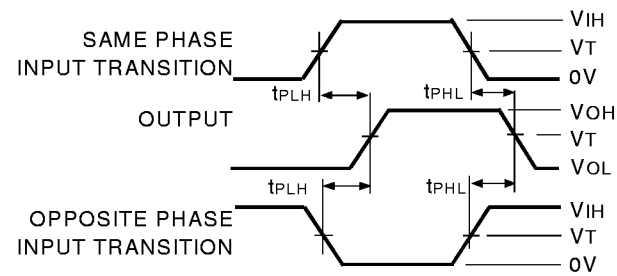
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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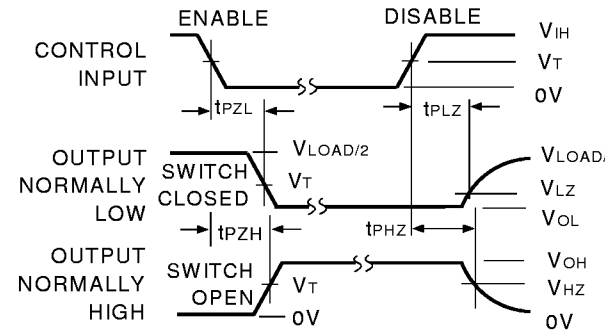
ENABLE AND DISABLE TIMES



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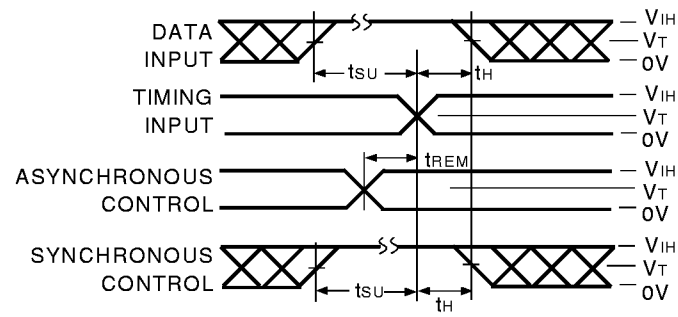
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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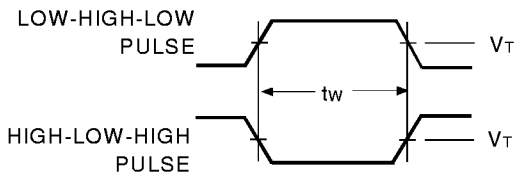
PULSE WIDTH



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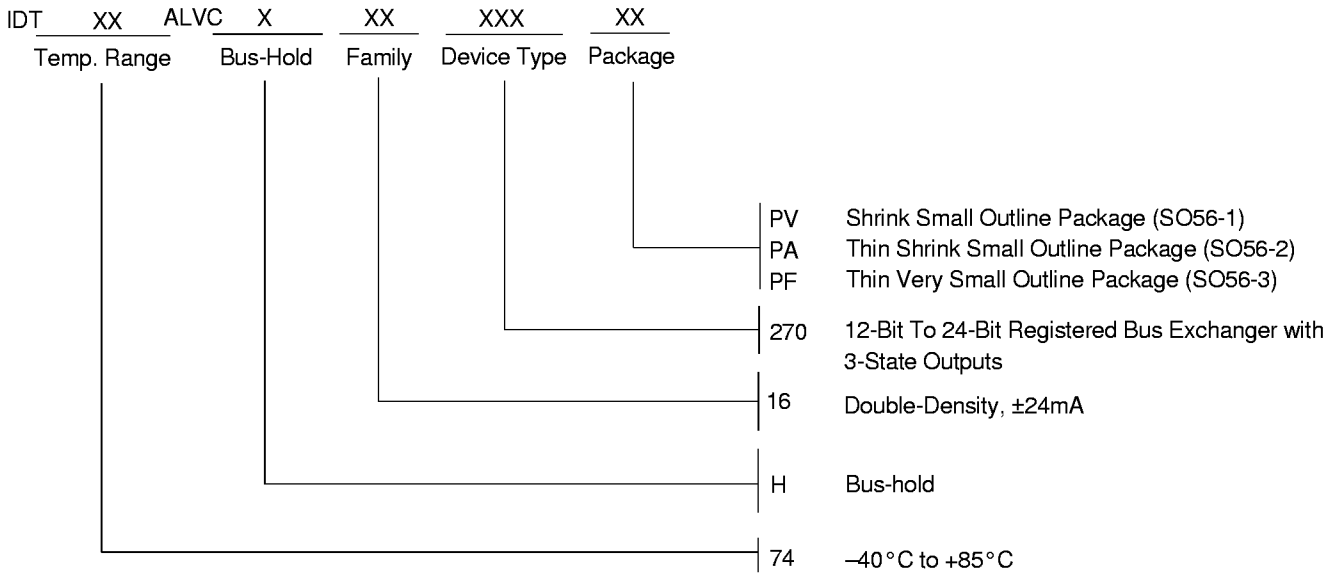
ORDERING INFORMATION



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