Octal latched transceiver with dual enable (3-State) 54ABT543

FEATURES

- Combines 54ABT245 and 54ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +48mA/-24mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883C Method 3015.6 and 200V per Machine Model

DESCRIPTION

The 54ABT543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 54ABT543 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 48mA.

FUNCTIONAL DESCRIPTION

The 54ABT543 contain two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

ORDERING INFORMATION

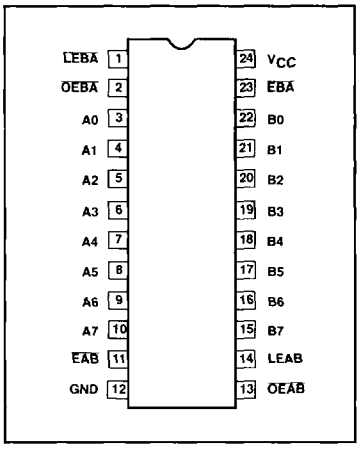
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-Pin Ceramic DIP	54ABT543/BLA	GDIP3-T24
28-Pin Ceramic LLCC	54ABT543/B3A	CQCC2-N28

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

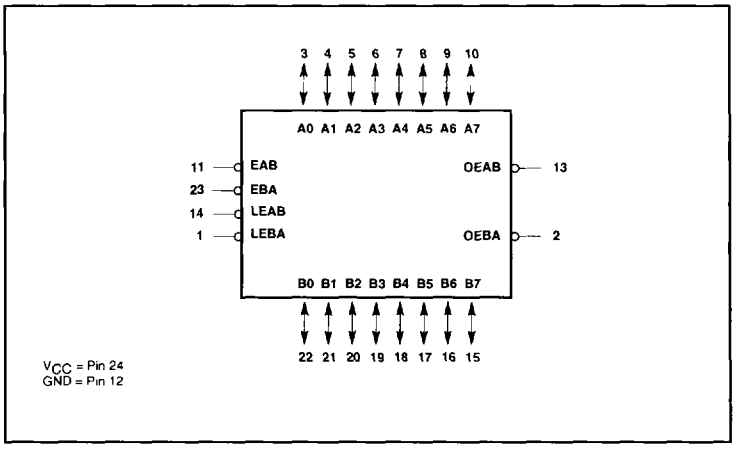
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 1	$\overline{LEAB}/\overline{LEBA}$	A to B/B to A Latch Enable input (Active Low)
11, 23	$\overline{EAB}/\overline{EBA}$	A to B/B to A Enable input (Active Low)
13, 2	$\overline{OEAB}/\overline{OEBA}$	A to B/B to A Output Enable input (Active Low)
3, 4, 5, 6, 7, 8, 9, 10	A0 - A7	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	B0 - B7	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

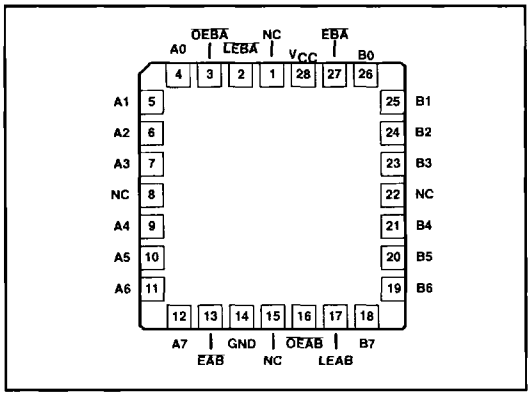
PIN CONFIGURATION



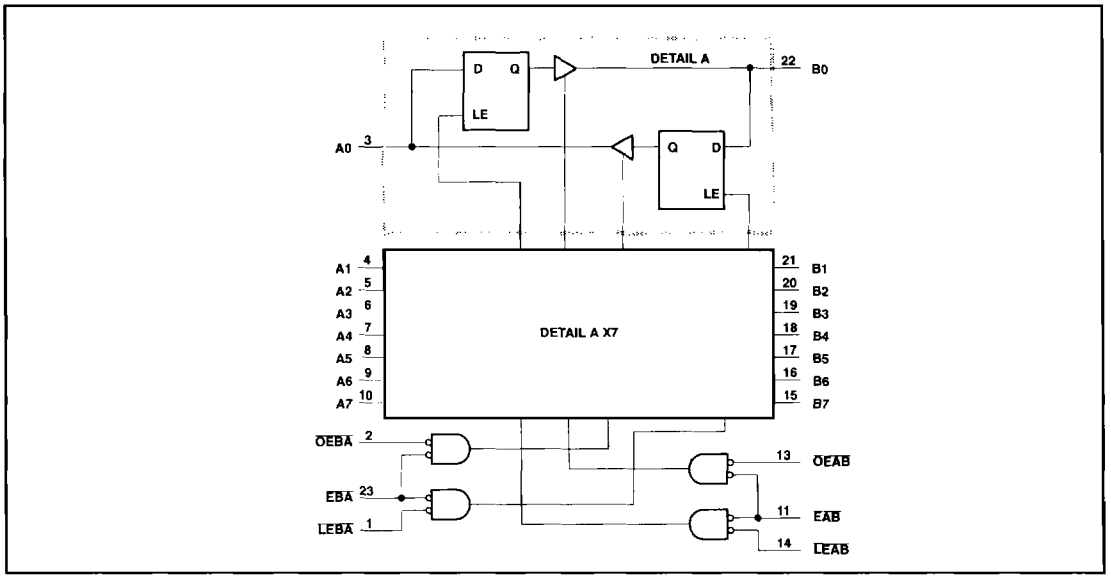
LOGIC SYMBOL



LLCC LEAD CONFIGURATION



LOGIC DIAGRAM



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FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	EXX	$\overline{LEXX}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disable + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ = Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
X = Don't care
NC = No change
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	96	mA
T_{stg}	Storage temperature range		–65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–55	+125	°C

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: V_{CC} = MAX, V_I = V_{IL} or V_{IH}, T_{amb} = –55 to +125 °C)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V, I_{IK} = -18mA		–0.9	–1.2	V
V_{OH}	High-level output to voltage		V_{CC} = 4.5V; I_{OH} = -3mA	2.5	3.5		V
			V_{CC} = 5.0V; I_{OH} = -3mA	3.0	3.5		V
			V_{CC} = 4.5V; I_{OH} = -24mA	2.0	2.6		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 48mA		0.42	0.55	V
I_I	Input leakage current	Control pins	V_I = GND or 5.5V		±0.01	±1.0	µA
		Data pins[8]	V_I = GND or 5.5V		±5	±100	µA
I_{IH} + I_{OZH}	3-State output High current		V_O = 2.7V, V_I = V_{IL} or 3.0V[9]		0.5	5.0	µA
I_{IL} + I_{OZL}	3-State output Low current		V_O = 0.5V, V_I = V_{IL} or 3.0V[9]		–0.5	–5.0	µA
I_O	Short-circuit output current[4]		V_O = 2.5V, V_I = GND or V_{CC}	–50	–80	–180	mA
I_{CCH}	Quiescent supply current		Outputs High, V_I = GND or V_{CC}		50	250	µA
I_{CCL}			Outputs Low, V_I = GND or V_{CC}		20	30	mA
I_{CCZ}			Outputs 3-State, V_I = GND or V_{CC}		50	250	µA
ΔI_{CC}	Additional supply current per input pin[5]		One input at 3.4V, other inputs at V_{CC} or GND		0.3	1.5	mA
I_{OFF}	Power OFF leakage current		V_{CC} = 0.0V; V_I or V_O ≤ 4.5V	–100		100	µA
			T_{amb} = 25°C	–1.0		1.0	
I_{CEX}	Output HIGH leakage current		V_{CC} = 5.5V; V_O = 5.5V			5.0	µA

AC ELECTRICAL CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –55°C to +125°C, V_{CC} = +5.0V ± 0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 2	1.9 1.6	4.4 4.4	5.1 5.1	1.9 1.6	6.4 6.2	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	Waveform 1, 2	1.6 1.6	4.1 4.6	5.1 5.4	1.6 1.6	6.6 6.4	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn	Waveform 4 Waveform 5	1.4 2.5	3.9 5.0	4.5 5.8	1.2 1.8	6.0 7.2	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to An or $\overline{OEAB}$ to Bn	Waveform 4 Waveform 5	2.5 2.5	5.9 5.5	5.8 6.1	3.3 2.5	6.5 7.6	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to An or $\overline{EAB}$ to Bn	Waveform 4 Waveform 5	1.4 2.0	3.9 5.0	4.7 5.7	1.3 2.1	6.2 7.4	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to An or $\overline{EAB}$ to Bn	Waveform 4 Waveform 5	3.4 3.0	5.9 5.5	6.0 6.2	3.3 3.0	7.0 7.0	ns ns

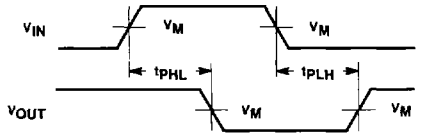
AC SETUP REQUIREMENTS[6]

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −55°C to +125°C, V_{CC} = +5.0V ± 10%		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	Waveform 3	3.5 3.0			3.5 3.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	Waveform 3	0.5 0.5			0.5 0.5		ns ns
$t_s(H)$ $t_s(L)$	Setup time An to $\overline{EAB}$, Bn to $\overline{EBA}$	Waveform 3	3.0 2.5			3.3 2.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time An to $\overline{EAB}$, Bn to $\overline{EBA}$	Waveform 3	0.5 0.5			0.5 0.5		ns ns
$t_w(L)$[7]	Latch enable pulse width, Low	Waveform 3	3.5			3.5		ns

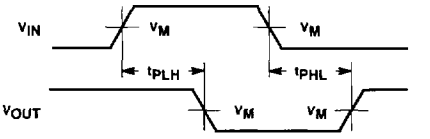
NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
5. This is the increase in supply current for each input at 3.4V.
6. t_{set} and t_{hold} limits that are less than 3ns are guaranteed, but only tested to 3.0ns due to tester limitations.
7. t_w limits that are less than 6.0ns are guaranteed, but only tested to 6.0ns due to tester limitations.
8. Input leakage on transceiver data pins also includes I_{OZH} or I_{OZL} current from the output circuitry.
9. To accommodate tester limitations, I_{OZ} tests are tested with V_{IH} = 3.0V, but 2.0V V_{IH} is guaranteed.

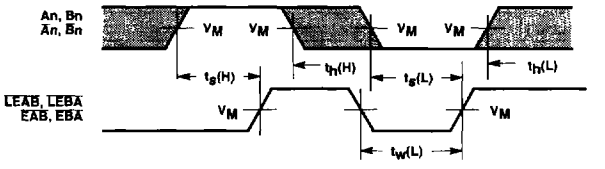
AC WAVEFORMS



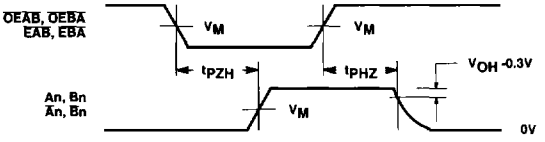
Waveform 1. Propagation Delay for Inverting Output



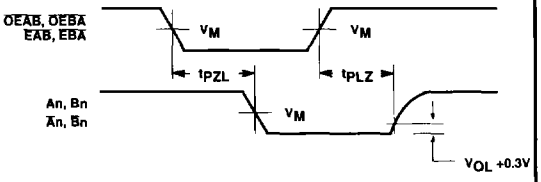
Waveform 2. Propagation Delay for Non-Inverting Output



Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width



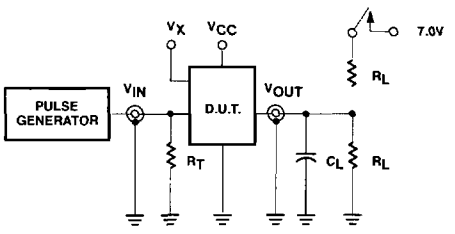
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



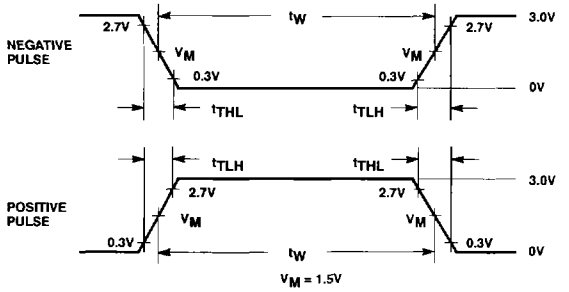
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE REQUIREMENTS					
Family	**Amplitude**	**Rep. Rate**	**t_W**	**t_R**	**t_F**
54ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.