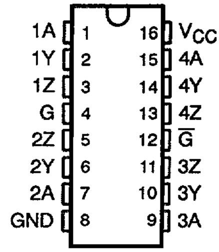
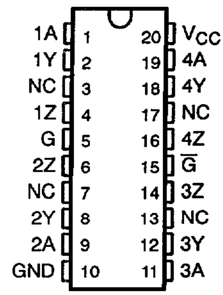
SLLS038A – D2596, OCTOBER 1980 – REVISED FEBRUARY 1993

- **Meets EIA Standards RS-422-A and RS-485**
- **Meets CCITT Recommendations V.11 and X.27**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Active-High and Active-Low Enables**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**
- **Functionally Interchangeable With AM26LS31**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75172 is a monolithic quad differential line driver with 3-state outputs. It is designed to meet the requirements of EIA Standards RS-422-A and RS-485 and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

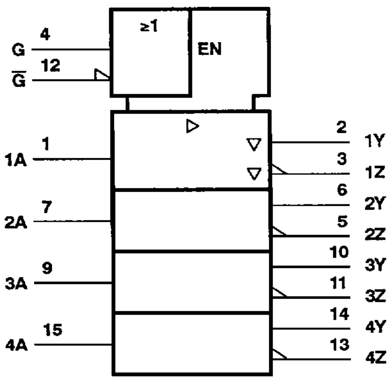
The SN75172 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

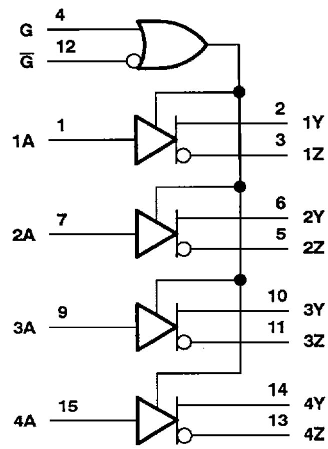
H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			−7 to 12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA					−1.5	V
V_O	Output voltage	$I_O = 0$			0		6	V
V_{OH}	High-level output voltage	$V_{IH} = 2$ V,	$V_{IL} = 0.8$ V,	$I_{OH} = -33$ mA		3.7		V
V_{OL}	Low-level output voltage	$V_{IH} = 2$ V,	$V_{IL} = 0.8$ V,	$I_{OH} = 33$ mA		1.1		V
$\|V_{OD1}\|$	Differential output voltage	$I_O = 0$			1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1		1/2 V_{OD1} or 2¶			V
		$R_L = 54\ \Omega$,	See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2			1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡	$R_L = 54\ \Omega$ or $100\ \Omega$,		See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage§						+3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡						±0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7$ V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V					±100	μA
I_{IH}	High-level input current	$V_I = 2.7$ V					20	μA
I_{IL}	Low-level input current	$V_I = 0.5$ V					−360	mA
I_{OS}	Short-circuit output current	$V_O = -7$ V					−180	mA
		$V_O = V_{CC}$					180	
		$V_O = 12$ V					500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			38	60	mA
			Outputs disabled			18	40	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In EIA Standard RS-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
NOTE 2: See Figure 3-5 of EIA Standard RS-485.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t ($R_L = 100\ \Omega$)	V_t ($R_L = 54\ \Omega$)
$\|V_{OD2}\|$		V_t (Test Termination) Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\bar{V}_t\|\|$	$\|\|V_t\| - \|\bar{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \bar{V}_{os}\|$	$\|V_{os} - \bar{V}_{os}\|$
I_{OS}	$\|I_{sa}\|, \|I_{sb}\|$	
I_O	$\|I_{xa}\|, \|I_{xb}\|$	I_{ia}, I_{ib}

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{dD}	Differential-output delay time	R_L = 54 Ω,	See Figure 2		45	65	ns
t_{tD}	Differential-output transition time				80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4		45	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3		78	115	ns
t_{PLZ}	Output disable time from low level9	R_L = 110 Ω,	See Figure 3		18	30	ns

PARAMETER MEASUREMENT INFORMATION

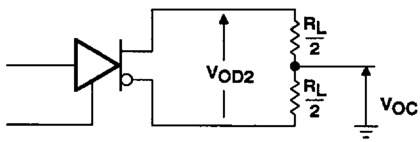


Figure 1. Differential and Common-Mode Output Voltages

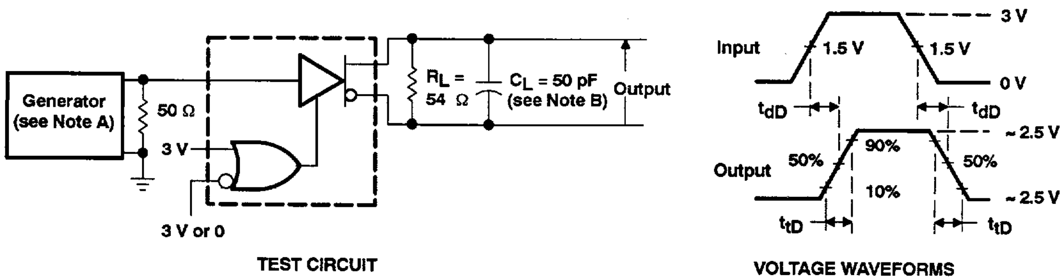
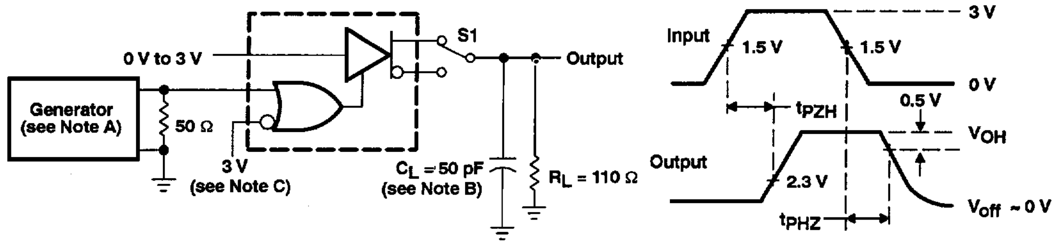


Figure 2. Differential-Output Test Circuit and Voltge Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.

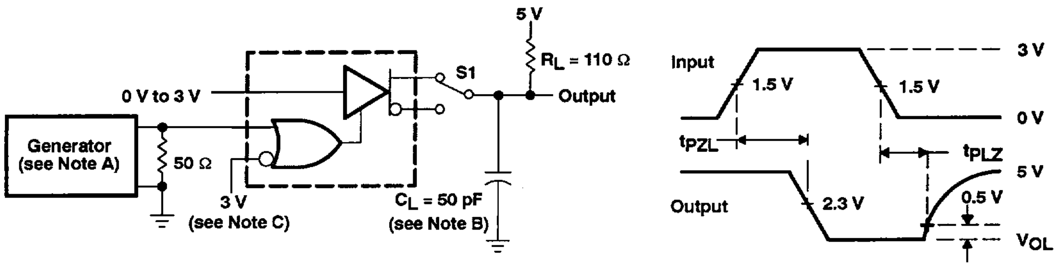
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 3. Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. Test Circuit and Voltage Waveforms

NOTES: C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.

D. C_L includes probe and stray capacitance.

E. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

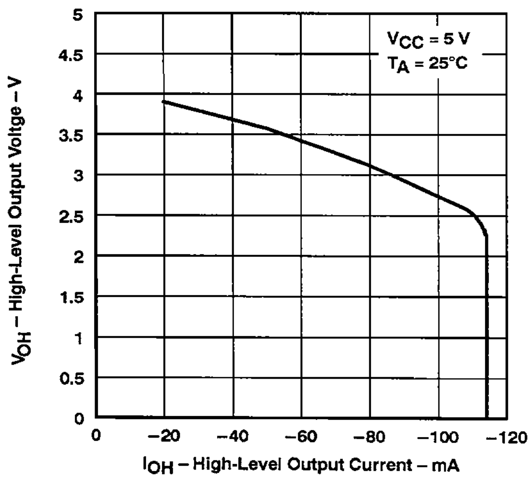


Figure 5

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

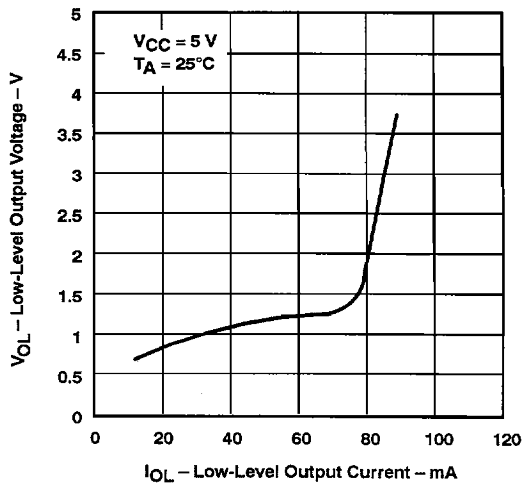


Figure 6

DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

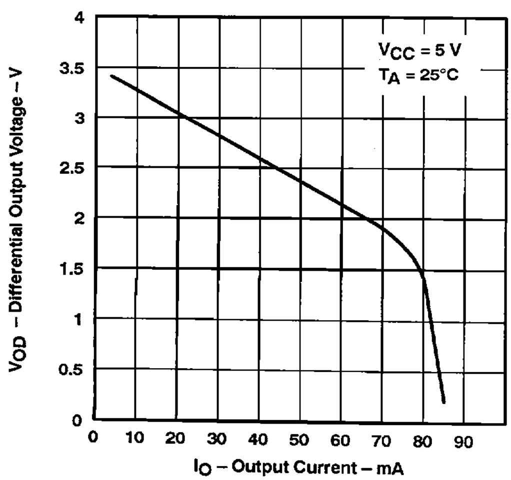


Figure 7

OUTPUT CURRENT vs OUTPUT VOLTAGE

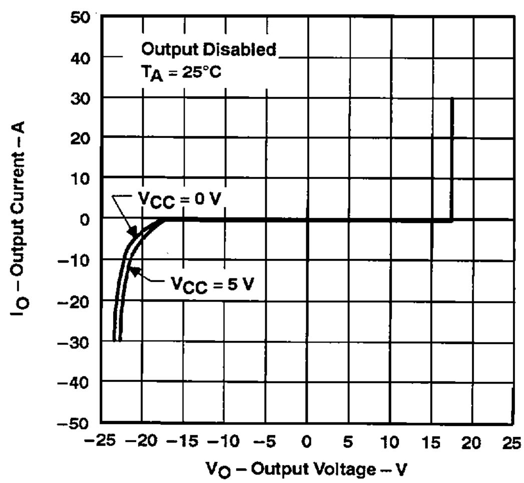


Figure 8

TYPICAL CHARACTERISTICS

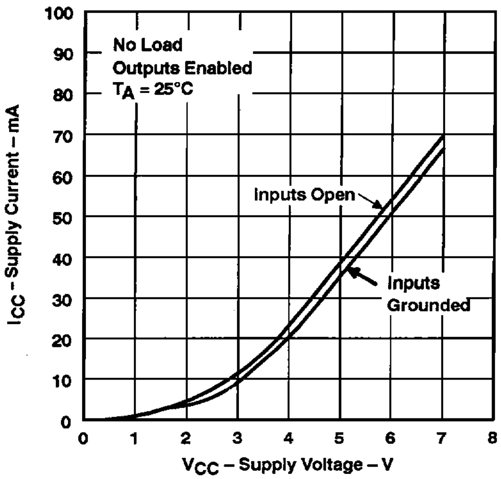


Figure 9

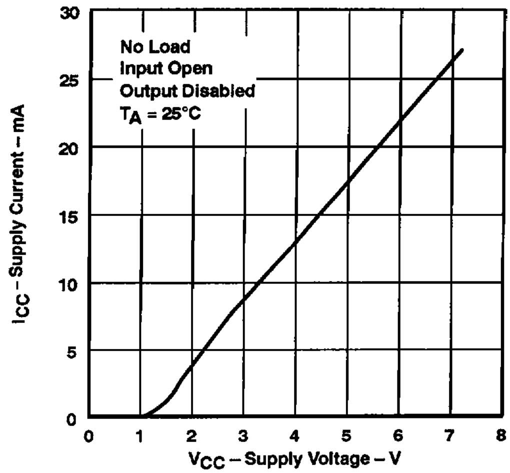
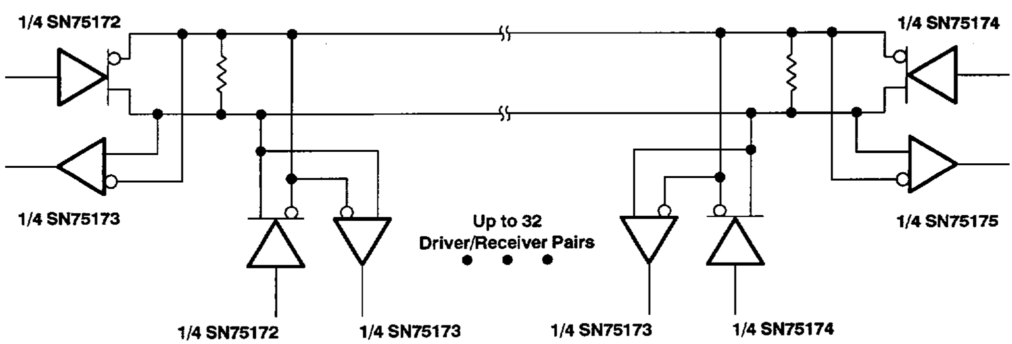


Figure 10

APPLICATION INFORMATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 11