

POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS ¹	54 FAMILY		SERIES 64H		SERIES 64L		SERIES 64S		SERIES 74S		UNIT
		SERIES 64	SERIES 74	SERIES 64H	SERIES 74H	SERIES 64L	SERIES 74L	SERIES 64S	SERIES 74S	SERIES 64S	SERIES 74S	
Supply voltage, V _{CC}		'00, '04, '10, '20, '30	MIN NOM MAX	'H00, 'H04, 'H10, 'H20, 'H30	MIN NOM MAX	'L00, 'L04, 'L10, 'L20, 'L30	MIN NOM MAX	'S00, 'S04, 'S10, 'S20, 'S30, 'S133	MIN NOM MAX	MIN NOM MAX	MIN NOM MAX	V
		4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	4.5 5 5.5	V
High-level output current, I _{OH}		4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	4.75 5 5.25	mA
Low-level output current, I _{OL}		-400	-400	-600	-600	-1000	-1000	-1000	-1000	-1000	-1000	mA
Operating free-air temperature, T _A		0 70	0 70	0 70	0 70	0 70	0 70	0 70	0 70	0 70	0 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS ¹		SERIES 64		SERIES 64H		SERIES 64L		SERIES 64S		UNIT
		SERIES 64	SERIES 74	SERIES 64H	SERIES 74H	SERIES 64L	SERIES 74L	SERIES 64S	SERIES 74S	SERIES 64S	SERIES 74S	
V _{IH} High-level input voltage	1, 2	2	2	0.8	0.8	0.7	0.7	0.7	0.7	0.7	0.7	V
V _{IL} Low-level input voltage	1, 2	0.8	0.8	0.8	0.8	0.7	0.7	0.7	0.7	0.8	0.8	V
V _{IK} Input clamp voltage	3	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.2	V
V _{OH} High-level output voltage	1	2.4 3.4	2.4 3.5	2.4 3.5	2.4 3.5	2.4 3.3	2.4 3.2	2.5 3.4	2.5 3.4	2.5 3.4	2.5 3.4	V
V _{OL} Low-level output voltage	2	0.2 0.4	0.2 0.4	0.2 0.4	0.2 0.4	0.15 0.3	0.2 0.4	0.25 0.4	0.25 0.4	0.25 0.5	0.5	V
I _I Input current at maximum input voltage	4	1	1	1	1	0.1	0.1	0.1	0.1	0.1	1	mA
I _{IH} High-level input current	4	40	40	50	50	10	10	10	10	20	50	μA
I _{IL} Low-level input current	5	-1.5	-1.5	-2	-2	-0.18	-0.18	-0.4	-0.4	-0.4	-2	mA
I _{OS} Short-circuit output current*	6	-20 -55	-40 -100	-3 -15	-20 -100	-3 -15	-20 -100	-40 -100	-40 -100	-40 -100	-40 -100	mA
I _{CC} Supply current	7	-18 -55	-40 -100	-3 -15	-20 -100	-3 -15	-20 -100	-40 -100	-40 -100	-40 -100	-40 -100	mA

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

² All typical values are at V_{CC} = 5 V, T_A = 25°C.

³ I_I = -12 mA for SN64/SN74*, -8 mA for SN64H/SN74H*, and -18 mA for SN64LS/SN74LS* and SN64S/SN74S*.

Not more than one output should be shorted at a time, and for SN64H/SN74H, SN64LS/SN74LS*, and SN64S/SN74S*, duration of short-circuit should not exceed 1 second.

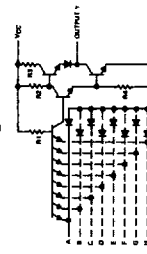
See table on next page

POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

supply current†

TYPE	I _{CCH} (mA) Total with outputs high		I _{CCL} (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	MAX
'00	4	8	12	22	2	2
'04	6	12	18	33	2	2
'10	3	6	9	16.5	2	2
'20	2	4	6	11	2	2
'30	1	2	3	6	2	2
'H00	10	16.8	26	40	4.5	4.5
'H04	16	26	40	58	4.5	4.5
'H10	7.5	12.6	19.5	30	4.5	4.5
'H20	5	8.4	13	20	4.5	4.5
'H30	2.5	4.2	6.5	10	4.5	4.5
'L00	0.44	0.8	1.16	2.04	0.20	0.20
'L04	0.66	1.2	1.74	3.06	0.20	0.20
'L10	0.33	0.6	0.87	1.53	0.20	0.20
'L20	0.22	0.4	0.66	1.02	0.20	0.20
SN54L30	0.11	0.33	0.29	0.51	0.20	0.20
SN74L30	0.11	0.2	0.29	0.51	0.20	0.20
'LS00	0.8	1.6	2.4	4.4	0.4	0.4
'LS04	1.2	2.4	3.6	6.6	0.4	0.4
'LS10	0.6	1.2	1.8	3.3	0.4	0.4
'LS20	0.4	0.8	1.2	2.2	0.4	0.4
'LS30	0.35	0.5	0.6	1.1	0.48	0.48
'S00	10	16	20	36	3.75	3.75
'S04	15	24	30	54	3.75	3.75
'S10	7.5	12	15	27	3.75	3.75
'S20	5	8	10	18	3.75	3.75
'S30	3	6	5.5	10	4.25	4.25
'S133	3	5	5.5	10	4.25	4.25

† Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.



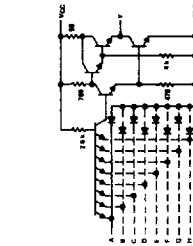
CIRCUIT	R1	R2	R3	R4
'00, '04, '10, '20, '30	4 k	1.6 k	130	1 k
'L00, 'L04, 'L10, 'L20, 'L30	40 k	20 k	500	12 k

'L00, 'L04, 'L10, 'L20, 'L30, CIRCUITS

Input clamp diodes not on SN54L/SN74L* circuits.

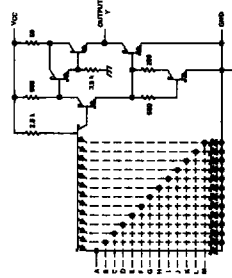
'H00, 'H04, 'H10, 'H20, 'H30, CIRCUITS

*The 12-kΩ resistor is not on 'LS30.



'LS00, 'LS04, 'LS10, 'LS20, 'LS30, CIRCUITS

*The 12-kΩ resistor is not on 'LS30.

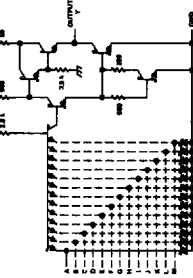
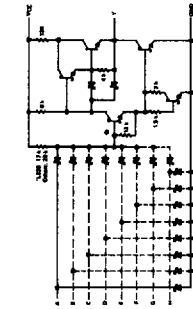
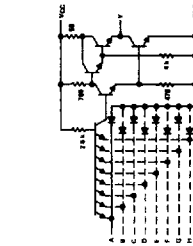


'S00, 'S04, 'S10, 'S20, 'S30, 'S133, CIRCUITS

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t _{PLH} (ns) Propagation delay time, low-to-high-level output			t _{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'00, '10	C _L = 15 pF, R _L = 400 Ω	11	22	7	15		
'04, '20		12	22	8	15		
'30		13	22	8	15		
'H00	C _L = 25 pF, R _L = 280 Ω	5.9	10	6.2	10		
'H04		6	10	6.5	10		
'H10		5.9	10	6.3	10		
'H20	C _L = 50 pF, R _L = 4 kΩ	6	10	7	10		
'H30		6.8	10	8.9	12		
'L00, 'L04, 'L10, 'L20		35	60	31	60		
'L30	C _L = 15 pF, R _L = 2 kΩ	35	60	70	100		
'LS00, 'LS04		9	15	10	15		
'LS10, 'LS20, 'LS30		8	15	13	20		
'S00, 'S04	C _L = 15 pF, R _L = 280 Ω	3	4.5	3	5		
'S10, 'S20		4.5	5	5	5		
'S30, 'S133		4	6	4.5	7		
'S30, 'S133	C _L = 50 pF, R _L = 280 Ω	5.5	6.5	6.5	6.5		
'S30, 'S133		5.5	6.5	6.5	6.5		

Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.



POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	84 FAMILY 74 FAMILY	SERIES 84 SERIES 74		SERIES 84H SERIES 74H		SERIES 84L SERIES 74L		SERIES 84LS SERIES 74LS		SERIES 84S SERIES 74S		UNIT
		'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	
Supply voltage, V _{CC}	54 Family 74 Family	4.5 4.75	5 5.25	4.5 4.75	5 5.25	4.5 4.75	5 5.25	4.5 4.75	5 5.25	4.5 4.75	5 5.25	V
High-level output voltage, V _{OH}	54 Family	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	V
Low-level output current, I _{OL}	54 Family 74 Family	16 16	20 20	20 20	20 20	20 20	20 20	20 20	20 20	20 20	20 20	mA
Operating free-air temperature, T _A	54 Family 74 Family	-55 0	125 70	-55 0	125 70	-55 0	125 70	-55 0	125 70	-55 0	125 70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	SERIES 84 SERIES 74		SERIES 84H SERIES 74H		SERIES 84L SERIES 74L		SERIES 84LS SERIES 74LS		SERIES 84S SERIES 74S		UNIT
			'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	'01, '03, '06, '12, '22	
V _{IH} High-level input voltage	1, 2		2	0.8	0.8	0.8	0.8	0.8	0.7	0.8	0.8	V	
V _{IL} Low-level input voltage	1, 2			0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	V	
V _{IK} Input clamp voltage	3	V _{CC} - MIN, I _I = 5		-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.2	V	
I _{OH} High-level output current	1	V _{CC} = MIN, V _{IL} = V _{IL} max, V _{OH} = 5.5 V	250	250	250	250	250	250	100	250	250	μA	
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _{IH} = 2 V	0.2	0.4	0.2	0.4	0.2	0.4	0.15	0.3	0.4	0.5	
I _I Input current at maximum input voltage	4	V _{CC} = MAX, V _I = 5.5 V	1	1	1	1	1	0.1	0.1	1	1	mA	
I _{IH} High-level input current	4	V _{CC} = MAX, V _{IH} = 2.4 V	40	50	50	50	10	10	10	50	50	μA	
I _{IL} Low-level input current	5	V _{CC} = MAX, V _{IL} = 0.3 V	-1.6	-2	-2	-2	-0.18	-0.18	-0.18	-2	-2	mA	
I _{CC} Supply current	7	V _{CC} = MAX, V _I = 0.5 V										mA	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] I_I = -1.2 mA for SN54/SN74[†], -8 mA for SN54H/SN74H[†], and -18 mA for SN54LS/SN74LS[†] and SN54S/SN74S[†].

See table on next page

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

supply current†

TYPE	I _{CC} H (mA) Total with outputs high		I _{CC} L (mA) Total with outputs low		I _{CC} (mA) Average per Gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	MAX
'01	4	8	12	22	2	2
'03	4	8	12	22	2	2
'05	6	12	18	33	2	2
'12	3	6	9	16.5	2	2
'22	2	4	6	11	2	2
'H01	6.8	10	26	40	4.1	4.1
'H05	16	26	40	58	4.87	4.87
'H22	3.4	5	13	20	4.1	4.1
'L01	0.44	0.8	1.16	2.04	0.20	0.20
'L03	0.44	0.8	1.16	2.04	0.20	0.20
'LS01	0.8	1.6	2.4	4.4	0.4	0.4
'LS03	0.8	1.6	2.4	4.4	0.4	0.4
'LS05	1.2	2.4	3.6	6.6	0.4	0.4
'LS12	0.7	1.4	1.8	3.3	0.42	0.42
'LS22	0.4	0.8	1.2	2.2	0.4	0.4
'S03	6	13.2	20	36	3.25	3.25
'S05	9	19.8	30	54	3.25	3.25
'S22	3	6.6	10	18	3.25	3.25

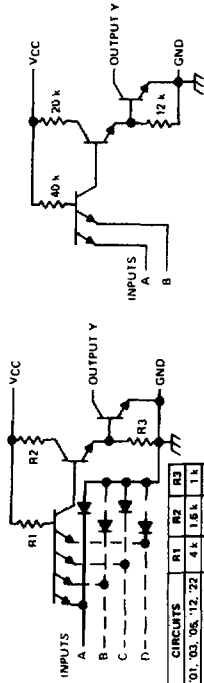
† Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

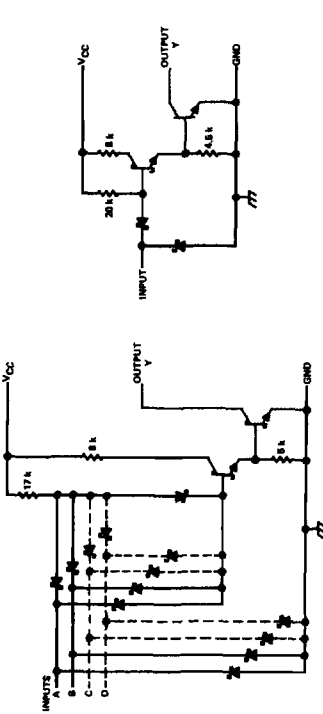
TYPE	TEST CONDITIONS#	τ _{PLH} (ns) Propagation delay time, low-to-high-level output		τ _{PHL} (ns) Propagation delay time, high-to-low-level output	
		MIN	TYP	MAX	TYP
'01, '03	C _L = 15 pF, R _L = 4 kΩ for τ _{PLH} , 400 Ω for τ _{PHL}	35	45	8	15
'05		40	55	8	15
'12, '22	C _L = 25 pF, R _L = 280 Ω	35	45	8	15
'H01, 'H05, 'H22		10	15	7.5	12
'L01, 'L03	C _L = 50 pF, R _L = 4 kΩ	60	90	33	60
'LS01, 'LS03,	C _L = 15 pF, R _L = 2 kΩ	17	32	15	28
'LS05, 'LS12, 'LS22		2	5	7.5	2
'S03, 'S05, 'S22	C _L = 15 pF, R _L = 280 Ω	2	5	7.5	2
	C _L = 50 pF, R _L = 280 Ω	7.5	7	4.5	7

Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

schematics (each gate)



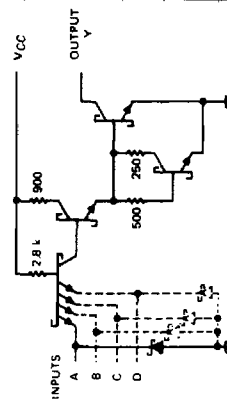
'01, '03, '05, '12, '22, 'H01, 'H05, 'H22 CIRCUITS



'L01, 'L03 CIRCUITS

'LS01, 'LS03, 'LS12, 'LS22 CIRCUITS

'LS05 CIRCUITS



'S03, 'S05, 'S22 CIRCUITS

Resistor values shown are nominal and in ohms.

OPEN-COLLECTOR OUTPUT APPLICATION DATA

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine standard loads of its own series. When no other open-collector gates are paralleled, this gate may be used to drive ten loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if only one of the paralleled outputs is sinking all the currents.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH \text{ min}}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH \text{ to TTL loads}}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(\text{max})} = \frac{V_{CC} - V_{OH \text{ min}}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of standard loads.

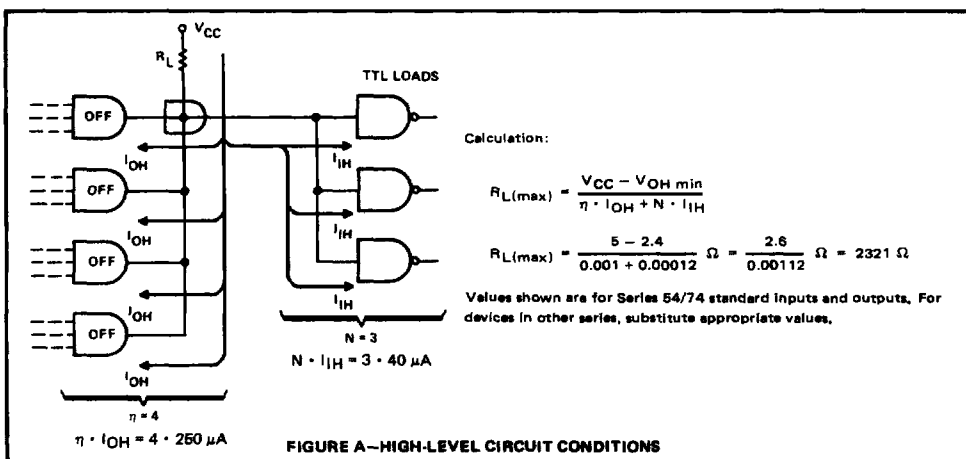


FIGURE A—HIGH-LEVEL CIRCUIT CONDITIONS

OPEN-COLLECTOR OUTPUT APPLICATION DATA

APPLICATION DATA

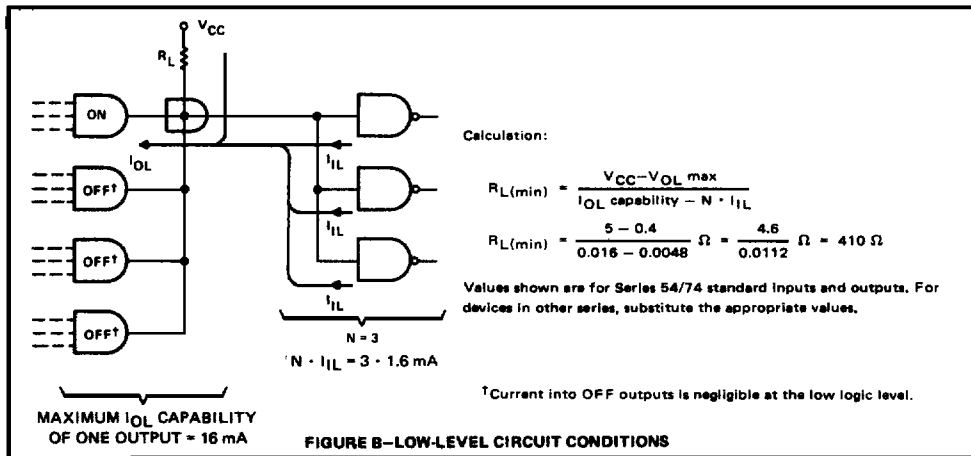
low-level (on-state) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to the recommended maximum I_{OL} , the maximum current which will ensure that the low-level output voltage, V_{OL} , will be below $V_{OL\ max}$.

Also, fan-out must be considered. Part of I_{OL} will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L .

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(\min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

PARAMETER	74 FAMILY		SERIES 54 SERIES 74		SERIES 54L SERIES 74L		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V _{CC}	4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
High-level output current, I _{OH}	4.75	5.25	4.75	5.25	4.75	5.25	4.75	5.25	4.75	5.25	mA
Low-level output current, I _{OL}	-4.00	-4.00	-4.00	-4.00	-4.00	-4.00	-4.00	-4.00	-4.00	-4.00	mA
Operating free-air temperature, T _A	0	70	0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74		SERIES 54L SERIES 74L		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{IH} High-level input voltage	1, 2	54 Family 74 Family	0.8	0.8	0.7	0.7	0.7	0.7	0.7	0.8	V
V _{IL} Low-level input voltage	1, 2	54 Family 74 Family	0.8	0.8	0.7	0.7	0.8	0.8	0.8	0.8	V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = 3	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.2	V
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4	3.4	2.4	3.3	2.5	3.4	2.5	3.4	V
V _{OL} Low-level output voltage	2	V _{CC} = MIN, I _{OL} = MAX V _{IH} = 2 V	0.2	0.4	0.15	0.3	0.25	0.4	0.25	0.4	V
I _I Input current at maximum input voltage	4	V _I = 5.5 V V _I > 7 V	1	1	0.1	0.1	0.1	0.1	0.1	0.1	mA
I _{IH} High-level input current	4	V _{CC} = MAX	40	40	10	10	20	20	20	20	μA
I _{IL} Low-level input current	5	V _{CC} = MAX	-1.6	-1.6	-0.18	-0.18	-0.4	-0.4	-0.4	-0.4	mA
I _{OS} Short-circuit output current‡	6	V _{CC} = MAX	-55	-3	-15	-20	-100	-40	-100	-40	mA
I _{CC} Supply current§	7	V _{CC} = MAX	-18	-55	-3	-15	-20	-100	-40	-100	mA

See table on next page

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN54/SN74* and -18 mA for SN54LS/SN74LS* and SN64S/SN74S*.

¶ Not more than one output should be shorted at a time, and for SN54LS/SN74LS* and SN64S/SN74S*, duration of output short-circuit should not exceed one second.

POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS

supply current†

TYPE	I _{CC} (mA)		I _{CL} (mA)		I _{CC} (mA)	
	Total with outputs high		Total with outputs low		Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	MAX
'02	8	16	14	27	2.75	2.75
'25	8	16	10	19	2.25	2.25
'27	10	16	16	26	4.34	4.34
'L02	0.8	1.6	1.4	2.6	0.275	0.275
'LS02	1.6	3.2	2.8	5.4	0.55	0.55
'LS27	2.0	4	3.4	6.8	0.9	0.9
'S02	17	29	26	45	5.38	5.38
'S260	17	29	26	45	10.75	10.75

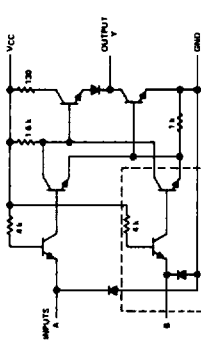
† Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t _{PLH} (ns)		Propagation delay time, low-to-high-level output		Propagation delay time, high-to-low-level output	
		MIN	TYP	MAX	MIN	TYP	MAX
'02	C _L = 15 pF, R _L = 400 Ω	12	15	8	15	8	15
'25		13	22	8	15	8	15
'27		10	15	7	11	7	11
'L02	C _L = 50 pF, R _L = 4 kΩ	31	60	35	60	35	60
'LS02, 'LS27		10	15	10	15	10	15
'S02		3.5	5.5	3.5	5.5	3.5	5.5
'S260	C _L = 15 pF, R _L = 280 Ω	5	5	5	5	5	5
		4	5.5	4	6	4	6

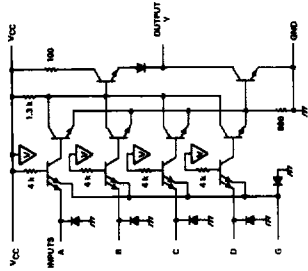
Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

schematics (each gate)



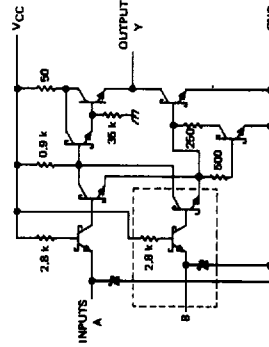
The portion of the schematic within the dashed lines is repeated for the C input of the '27.

'02, '27 CIRCUITS



'25 CIRCUITS

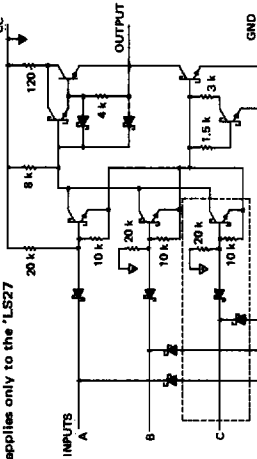
Resistor values are nominal and in ohms.



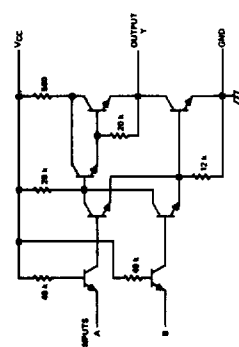
The portion of the schematic within the dashed lines is repeated for each additional input of the 'S260, and the 0.9-kΩ resistor is changed to 0.6 kΩ.

'S02, 'S260 CIRCUITS

The portion of the schematic within the dashed lines applies only to the 'LS27



'LS02, 'LS27 CIRCUITS



'L02 CIRCUITS

POSITIVE-AND GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	SERIES 54		SERIES 54H		SERIES 54S		SERIES 54S		UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM		MAX
Supply Voltage, V _{CC}			4.5	5	4.5	5	4.5	5	4.5	5	V	
High-level output current, I _{OH}			74 Family	4.75	5	4.75	5	4.75	5	4.75	5	μA
			54 Family	-800								
Low-level output current, I _{OL}			74 Family	16								mA
			54 Family	16								mA
Operating free-air temperature, T _A			54 Family	-55	125	-55	125	-55	125	-55	125	°C
			74 Family	0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	SERIES 54		SERIES 54H		SERIES 54S		SERIES 54S		UNIT	
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†		MAX
V _{IH} High-level input voltage	1, 2		2		2		2		2		V	
V _{IL} Low-level input voltage	1, 2		0.8		0.8		0.8		0.8		V	
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = 8	0.8		0.8		0.8		0.8		V	
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = MAX	54 Family	2.4	3.4	2.4	3.4	2.5	3.4	2.5	3.4	V
			74 Family	2.4	3.4	2.4	3.4	2.7	3.4	2.7	3.4	V
V _{OL} Low-level output voltage	2	V _{CC} = MIN, I _{OL} = MAX	54 Family	0.2	0.4	0.15	0.3	0.25	0.4	0.25	0.4	V
			74 Family	0.2	0.4	0.2	0.4	0.35	0.5	0.35	0.5	V
I _I Input current at maximum input voltage	4	V _{CC} = MAX	Series 74LS					0.25	0.4			mA
			54 Family	1		1		0.1		1		mA
I _{IH} High-level input current	4	V _{CC} = MAX	74 Family	40		50		0.1				μA
			54 Family	40		50		0.1				μA
I _{IL} Low-level input current	5	V _{CC} = MAX	74 Family	-1.6		-2		-0.4				μA
			54 Family	-1.6		-2		-0.4				μA
I _{OS} Short circuit output current [‡]	6	V _{CC} = MAX	-20	-55	-40	-100	-20	-100	-40	-100	mA	
I _{CC} Supply current	7	V _{CC} = MAX	-18	-55	-40	-100	-20	-100	-40	-100	mA	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 2.5 V.

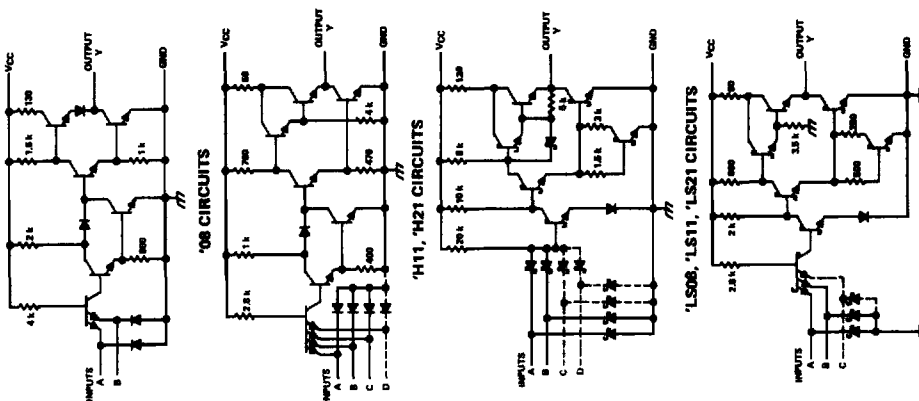
[§]I_I = -12 mA for SN54/SN74*, -8 mA for SN54H/SN74H*, and -18 mA for SN54LS/SN74LS* and SN54S/SN74S*.

Not more than one output should be shorted at a time, and for SN54H/SN74H, SN54LS/SN74LS* and SN54S/SN74S*, duration of output short circuit should not exceed one second.

See table on next page

POSITIVE-AND GATES WITH TOTEM-POLE OUTPUTS

schematics (each gate)



Resistor values shown are nominal and in ohms.

supply current[†]

TYPE	I _{CC} (mA)		I _{CL} (mA)		I _{CC} (mA)	
	Total with outputs high		Total with outputs low		Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	MAX
'08	11	21	20	33	3.88	
'H11	18	30	30	48	8	
'H21	12	20	20	32	8	
'LS08	2.4	4.8	4.4	8.8	0.85	
'LS11	1.8	3.6	3.3	6.6	0.85	
'LS21	1.2	2.4	2.2	4.4	0.85	
'S08	18	32	32	57	6.25	
'S11	13.5	24	24	42	6.25	

[†]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25° C.

switching characteristics at V_{CC} = 5 V, T_A = 25° C

TYPE	TEST CONDITIONS#	t _{pLH} (ns)		t _{pHL} (ns)			
		Propagation delay time, low-to-high-level output		Propagation delay time, high-to-low-level output			
		MIN	TYP	MAX	MIN	TYP	MAX
'08	C _L = 15 pF, R _L = 400 Ω		17.5	27	12	19	
'H11, 'H21	C _L = 25 pF, R _L = 280 Ω		7.6	12	8.8	12	
'LS08, 'LS11	C _L = 15 pF, R _L = 2 kΩ		8	15	10	20	
'LS21	C _L = 15 pF, R _L = 280 Ω		4.5	7	5	7.5	
'S08, 'S11	C _L = 50 pF, R _L = 280 Ω		6		7.5		

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	54 FAMILY		SERIES 64		SERIES 64H		SERIES 64LS		SERIES 64S		UNIT	
	74 FAMILY		SERIES 74		SERIES 74H		SERIES 74LS		SERIES 74S			
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5
High-level output voltage, V_{OH}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25
Low-level output current, I_{OL}	54 Family		16	74 Family		20	54 Family		4	74 Family		20
Operating free-air temperature, T_A	54 Family		16	74 Family		20	54 Family		4	74 Family		20
	54 Family		16	74 Family		20	54 Family		4	74 Family		20
	54 Family		-55	74 Family		-55	54 Family		-55	74 Family		-55
	54 Family		0	74 Family		0	54 Family		0	74 Family		0

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 64		SERIES 64H		SERIES 64LS		SERIES 64S		UNIT
			SERIES 74		SERIES 74H		SERIES 74LS		SERIES 74S		
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX
V_{IH} High-level input voltage	1, 2		2		2	2		2	2		V
V_{IL} Low-level input voltage	1, 2		0.8		0.8	0.8		0.7	0.8		V
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}, I_1 = \text{§}$	0.8		0.8	-1.5		-1.5	-1.2		V
I_{OH} High-level output current	1	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{OH} = 5.5 \text{ V}$	250		250	250		100	250		μA
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$	0.2	0.4	0.15	0.3	0.25	0.4	0.5		V
I_1 Input current at maximum input voltage	4	$V_{CC} = \text{MAX}, I_{OL} = 4 \text{ mA}$	1		1	0.1		0.1	1		mA
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}$	40		50	50		20	50		μA
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}$	-1.6		-2	-2		-0.4	-2		mA
I_{CC} Supply current	7	$V_{CC} = \text{MAX}$									mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ $I_1 = -12 \text{ mA}$ for SN64/SN74, -8 mA for SN64H/SN74H, and -18 mA for SN64LS/SN74LS.

See table on next page

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

supply current[†]

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	MAX
'09	11	21	20	33	3.88	
'H15	15	25	30	48	7.5	
'LS09	2.4	4.8	4.4	8.8	0.85	
'LS15	1.8	3.6	3.3	6.6	0.85	
'S09	18	32	32	57	6.25	
'S15	10.5	19.5	24	42	5.75	

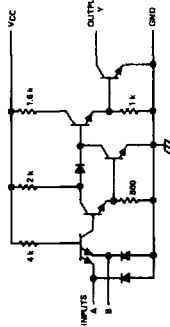
[†]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A . Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

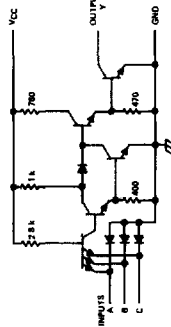
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output		t_{PHL} (ns) Propagation delay time, high-to-low-level output			
		MIN	TYP	MAX	MIN	TYP	MAX
'09	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$		21	32	16	24	
'H15	$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$		12	18	9	13	
'LS09, 'LS15	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$		20	35	17	35	
'S09	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$		6.5	10	6.5	10	
	$C_L = 50\text{ pF}$, $R_L = 280\ \Omega$		9		9		
'S15	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$		5.5	8.5	6	9	
	$C_L = 50\text{ pF}$, $R_L = 280\ \Omega$		8.5		8		

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

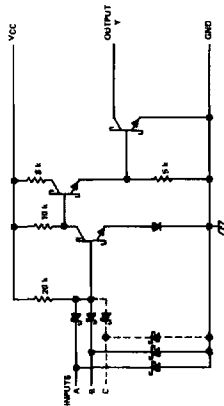
schematics (each gate)



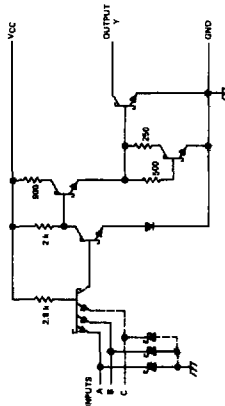
'09 CIRCUITS



'H15 CIRCUITS



'LS09, 'LS15 CIRCUITS



'S09, 'S15 CIRCUITS

Resistor values shown are nominal and in ohms.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

PARAMETER	54 FAMILY		SERIES 54				SERIES 54LS				SERIES 74LS				UNIT	
	74 FAMILY		SERIES 74				SERIES 74LS				SERIES 74LS					
	MIN	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Supply voltage, V _{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level output current, I _{OH}	-800		-800			-800			-800			-800			-1000	μA
Low-level output current, I _{OL}	18		18			18			18			18			20	mA
Operating free-air temperature, T _A	-55		125			-55			125			-55			125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]				SERIES 54				SERIES 54LS				SERIES 74LS				UNIT
						SERIES 54				SERIES 54LS				SERIES 74LS				
		MIN	TYP	MAX	MAX	MIN	TYP	MAX	MAX	MIN	TYP	MAX	MAX	MIN	TYP	MAX	MAX	
V _{T+} Positive-going threshold voltage	8	V _{CC} = 5 V				1.5	1.7	2	1.5	1.7	2	1.4	1.6	1.9	1.6	1.77	1.9	V
V _{T-} Negative-going threshold voltage	9	V _{CC} = 5 V				0.8	0.9	1.1	0.6	0.9	1.1	0.5	0.8	1	1.1	1.22	1.4	V
V _{IH} Input clamp voltage	8, 9	V _{CC} = 5 V				0.4	0.8	0.4	0.8	0.4	0.8	0.4	0.8	0.4	0.8	0.2	0.85	V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = 8				-1.5			-1.5			-1.5			1.5		-1.2	V
V _{OH} High-level output voltage	9	V _{CC} = MAX, V _I = V _{T-} , min				2.4	3.4		2.4	3.4		2.5	3.4		2.5	3.4		V
V _{OL} Low-level output voltage	8	V _{CC} = MIN, I _{OL} = MAX				0.2	0.4	0.2	0.4	0.2	0.4	0.25	0.4	0.25	0.4	0.5		V
I _{T+} Input current at positive-going threshold	8	V _{CC} = 5 V, V _I = V _{T+}				-0.65			-0.43			-0.14			-0.9			mA
I _{T-} Input current at negative-going threshold	9	V _{CC} = 5 V, V _I = V _{T-}				-0.85			-0.56			-0.18			-1.1			mA
I _I Input current at maximum input voltage	4	V _{CC} = MAX				1			1			0.1						mA
I _{IH} High-level input current	4	V _{CC} = MAX				40			40			20			50			μA
I _{IL} Low-level input current	5	V _{CC} = MAX				-1			-0.8			-0.4			-2			mA
I _{OB} Short-circuit output current [‡]	6	V _{CC} = MAX				-18			-55			-20			-40			mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] I_I = -12 mA for SN54/SN74[†] and -18 mA for 'LS13, 'LS14, 'LS132, and 'S132.

[¶] Not more than one output should be shorted at a time, and for SN54LS/SN74LS[†] and 'S132, duration of output short-circuit should not exceed one second.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

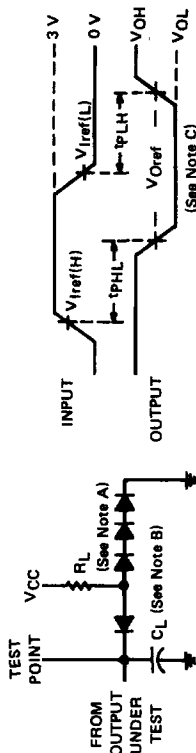
TYPE	TEST CONDITIONS	t_{PLH} (ns)		t_{PHL} (ns)		
		MIN	TYP	MAX	MIN	TYP
'13	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$	18	27	15	22	
'14, '132		15	22	15	22	
'LS13		15	22	18	27	
'LS14	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	15	22	15	22	
'LS132		15	22	15	22	
'S132	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$	7	10.5	8.5	13	

supply current¹

TYPE	I_{OCH} (mA)		I_{OCL} (mA)		I_{CC} (mA)	
	TYP	MAX	TYP	MAX	Average per gate outputs low (50% duty cycle)	
'13	14	23	20	32	8.5	
'14	22	36	39	60	5.1	
'132	15	24	28	40	5.1	
'LS13	2.9	6	4.1	7	1.75	
'LS14	8.6	16	12	21	1.72	
'LS132	5.9	11	8.2	14	1.76	
'S132	28	44	44	68	9	

¹ Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A . Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

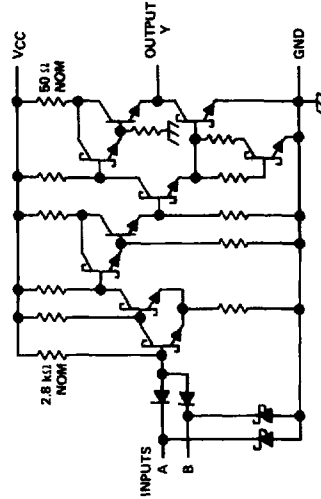
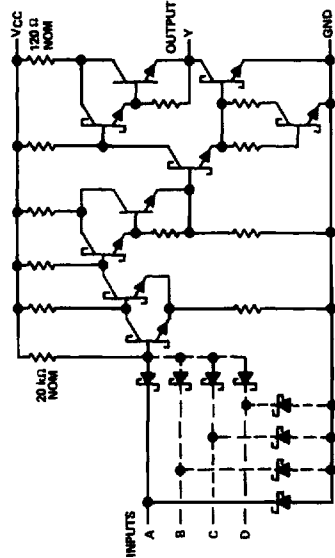
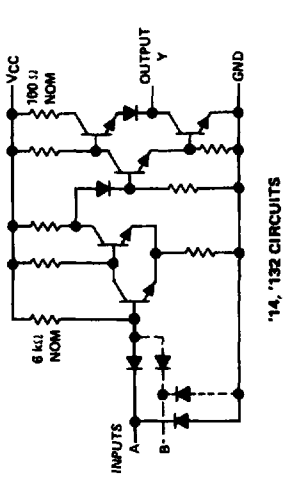
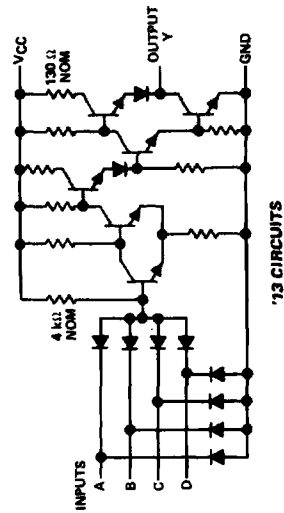
VOLTAGE WAVEFORMS

- NOTES: A. All diodes are 1N916 or 1N3064.
 B. C_L includes probe and jig capacitance.
 C. Generator characteristics and reference voltages are:

Generator Characteristics			Reference Voltages		
Z_{out}	PRR	t_r	$V_{I\text{ref}}(H)$	$V_{I\text{ref}}(L)$	$V_{O\text{ref}}$
50 Ω	1 MHz	10 ns	1.7 V	0.8 V	1.5 V
50 Ω	1 MHz	15 ns	1.8 V	0.8 V	1.3 V
50 Ω	1 MHz	2.5 ns	1.8 V	1.2 V	1.5 V

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

schematics (each gate)



Resistor values shown are nominal.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

TYPICAL CHARACTERISTICS OF '13, '14, AND '132 CIRCUITS†

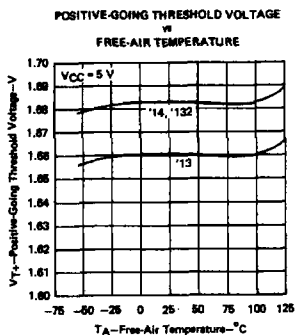


FIGURE 1

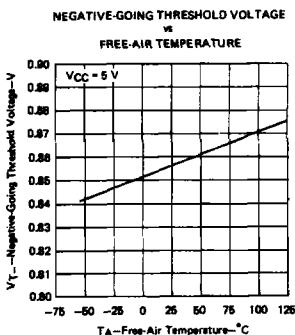


FIGURE 2

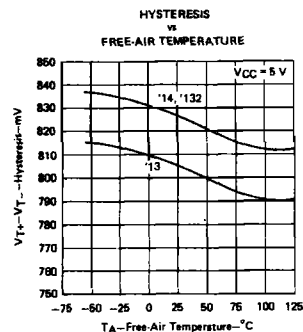


FIGURE 3

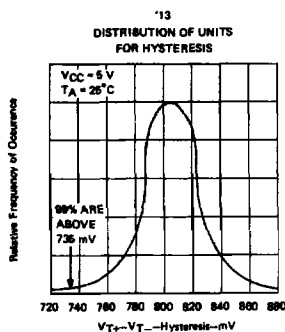


FIGURE 4

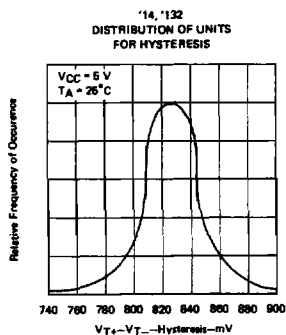


FIGURE 5

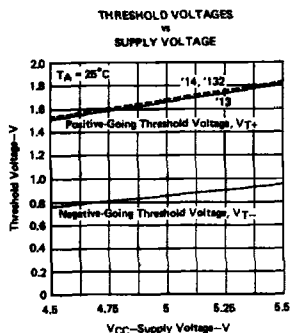


FIGURE 6

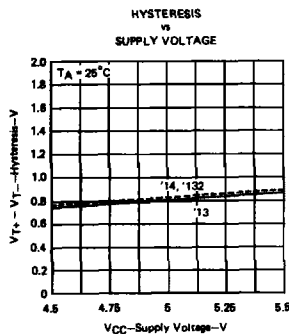


FIGURE 7

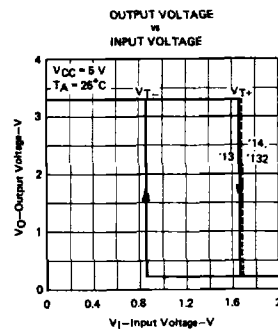
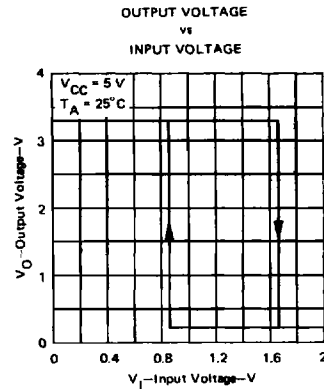
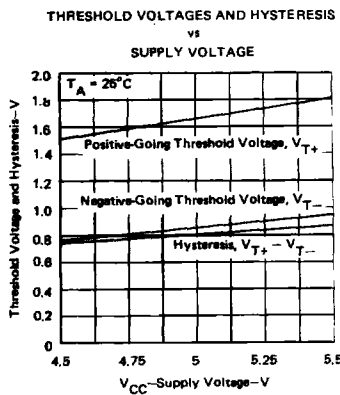
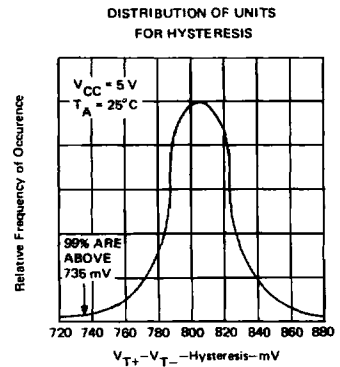
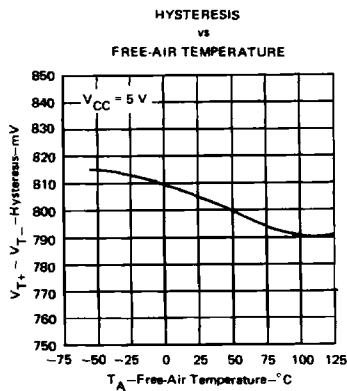
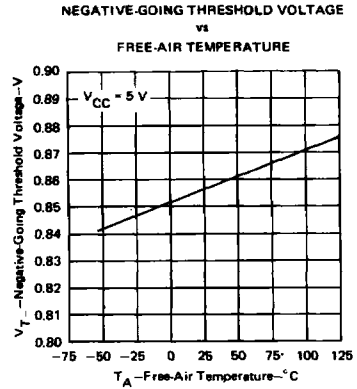
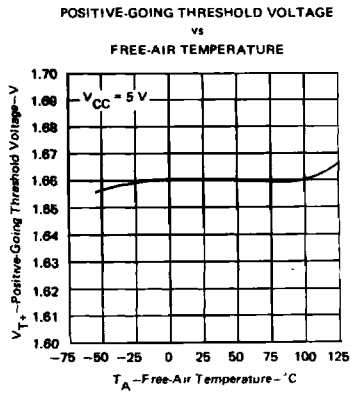


FIGURE 8

†Data for temperatures below 0°C and 70°C and supply voltages below 4.75V and above 5.25 V are applicable for SN5413, SN5414, and SN54132 only.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

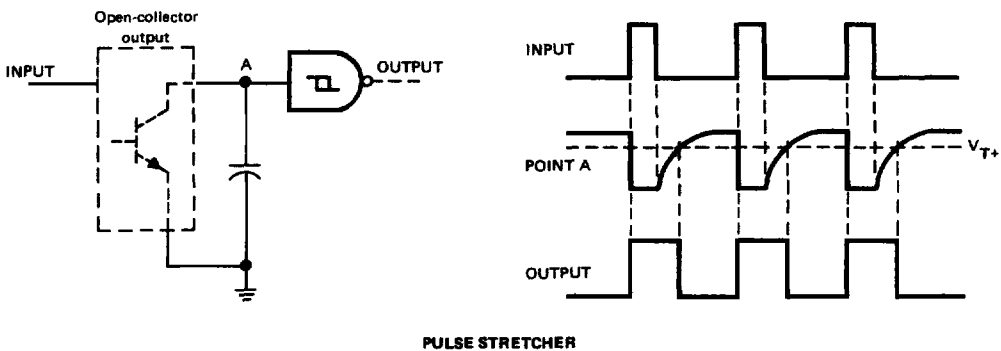
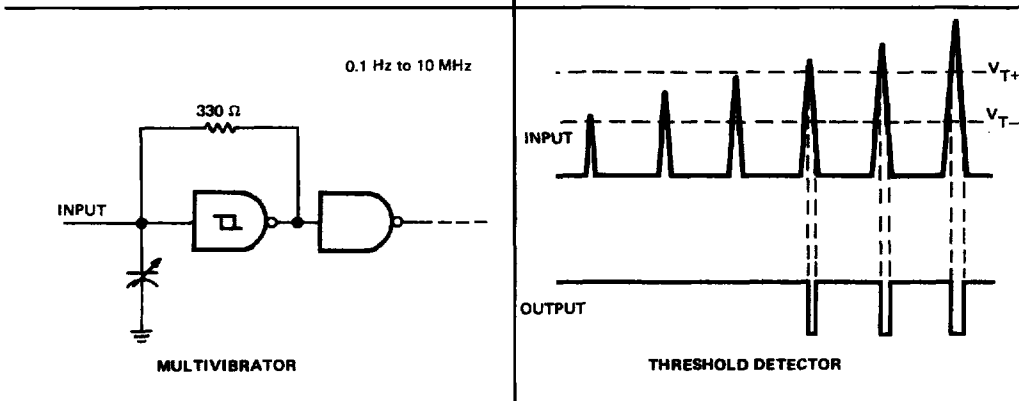
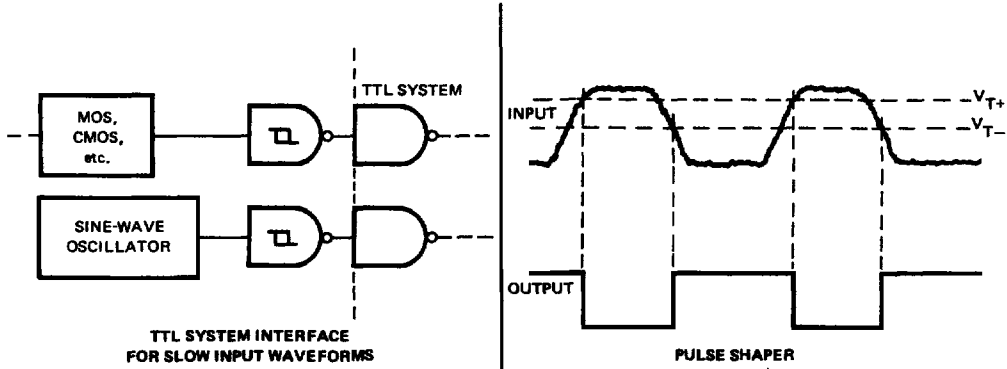
TYPICAL CHARACTERISTICS OF 'LS13, 'LS14, AND 'LS132 CIRCUITS†



† Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 are applicable for SN54LS13, SN54LS14, and SN54LS132 only.

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

TYPICAL APPLICATION DATA



BUFFERS/CLOCK DRIVERS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

PARAMETER	TEST CONDITIONS†	SERIES 54		SERIES 54H		SERIES 54LS		SERIES 54S		UNIT
		MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
Supply voltage, V _{CC}		4.5	5	4.5	5	4.5	5	4.5	5	V
High-level output current, I _{OH}		4.75	5	4.75	5	4.75	5	4.75	5	mA
Low-level output current, I _{OL}		-2.4	-1.2	-2.4	-1.2	-2.4	-1.2	-2.4	-1.2	mA
Operating free-air temperature, T _A		0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	SERIES 54		SERIES 54H		SERIES 54LS		SERIES 54S		UNIT
		MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
V _{IH} High-level input voltage	1, 2	0.8	0.8	0.8	0.8	0.7	0.7	0.8	0.8	V
V _{IL} Low-level input voltage	1, 2	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	V
V _{IK} Input clamp voltage	3	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.2	V
V _{OH} High-level output voltage	1	2.4	3.4	2.4	3.4	2.5	3.4	2.5	3.4	V
V _{OL} Low-level output voltage	2	0.2	0.4	0.2	0.4	0.15	0.3	0.25	0.4	V
I _I Input current at maximum input voltage	4	0.2	0.4	0.2	0.4	0.2	0.4	0.35	0.5	mA
I _{IH} High-level input current	4	0.2	0.4	0.2	0.4	0.25	0.4	0.25	0.4	mA
I _{IL} Low-level input current	5	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	mA
I _{OS} Short-circuit output current*	6	-70	-180	-70	-125	-30	-130	-50	-225	mA
I _{CC} Supply current	7	-70	-180	-70	-125	-30	-130	-50	-225	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

§ I_I = -12 mA for SN54/SN74, -8 mA for SN54H/SN74H, and -18 mA for SN54LS/SN74LS and SN54S/SN74S.

◆ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second for all of these circuits except 'S37 and 'S40, or 100 milliseconds for 'S37 and 'S40.

See table on next page

BUFFERS/CLOCK DRIVERS WITH TOTEM-POLE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t_{PLH} (ns)			t_{PHL} (ns)		
		MIN	TYP	MAX	MIN	TYP	MAX
'28	$C_L = 50\text{ pF}$, $R_L = 133\ \Omega$	Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low output		
		6	9	12	8	12	18
'37	$C_L = 150\text{ pF}$, $R_L = 133\ \Omega$	Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low output		
		10	15	22	8	15	24
'40	$C_L = 45\text{ pF}$, $R_L = 133\ \Omega$	Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low output		
		13	22	33	8	15	24
'H40	$C_L = 15\text{ pF}$, $R_L = 133\ \Omega$	Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low output		
		8.5	12	18	6.5	12	18
'LS28	$C_L = 25\text{ pF}$, $R_L = 93\ \Omega$	Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low output		
		12	24	36	12	24	36
'LS37	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$	Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low output		
		12	24	36	12	24	36
'LS40	$C_L = 50\text{ pF}$, $R_L = 93\ \Omega$	Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low output		
		12	24	36	12	24	36
'S37	$C_L = 150\text{ pF}$, $R_L = 93\ \Omega$	Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low output		
		6	6.5	12	4	4	6.5
'S40	$C_L = 150\text{ pF}$, $R_L = 93\ \Omega$	Propagation delay time, low-to-high-level output			Propagation delay time, high-to-low output		
		6	6.5	12	4	4	6.5

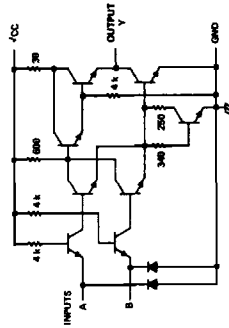
Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

supply current[†]

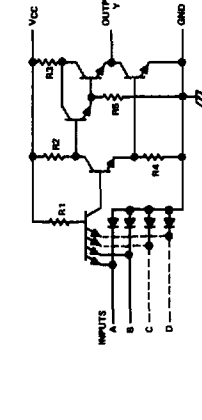
TYPE	I_{CCH} (mA)		I_{CCL} (mA)		I_{CC} (mA)	
	TYP	MAX	TYP	MAX	Average per gate (50% duty cycle)	TYP
'28	12	21	33	57	5.63	5.63
	9	15.5	34	54	5.38	5.38
'40	4	8	17	27	5.25	5.25
	10.4	16	25	40	8.05	8.05
'LS28	1.8	3.6	6.9	13.8	1.09	1.09
	0.9	2	6	12	0.86	0.86
'LS40	0.45	1	3	6	0.86	0.86
	20	36	46	80	8.25	8.25
'S40	10	18	25	44	8.75	8.75

† Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

schematics (each gate)

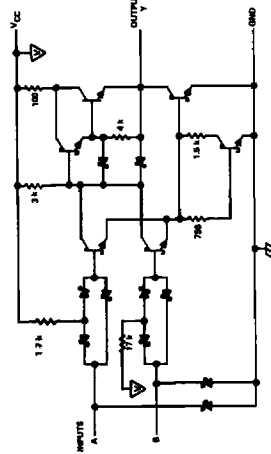


'28 CIRCuits



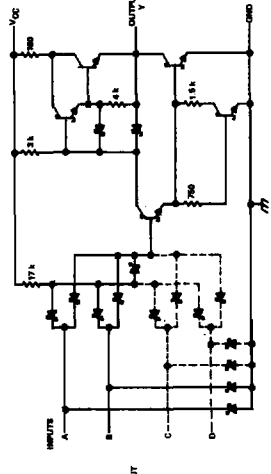
'37, '40, 'H40 CIRCuits

'37	'40	'H40
R1 4 k	4 k	1.4 k
R2 600	600	300
R3 100	100	45
R4 400	400	250
R5 4 k	4 k	2 k

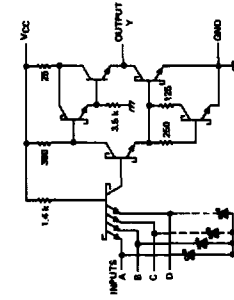


'LS28 CIRCuits

Resistor values shown are nominal and in ohms.



'LS37, 'LS40 CIRCuits



'S37, 'S40 CIRCuits

50-OHM/75-OHM LINE DRIVERS

recommended operating conditions

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54		SERIES 54S		SERIES 74S		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, VCC			4.5	5.5	4.5	5.5	4.5	5.5	V
High-level output current, IOH			4.75	5	4.75	5	4.75	5	mA
Low-level output current, IOL					-29	-40			mA
Operating free-air temperature, TA			-55	125	-55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54		SERIES 54S		SERIES 74S		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{IH} High-level input voltage	1, 2		2	0.8	2	0.8	2	0.8	V
V _{IL} Low-level input voltage	1, 2								V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §							V
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -2.4 mA	54 Family	2.4	3.4				
		V _{CC} = MIN, V _{IL} = 0.4 V, I _{OH} = -13.2 mA	74 Family	2.4	3.4				
		V _{CC} = MIN, V _{IL} = 0.4 V, I _{OH} = MAX		2					
		V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -3 mA	54 Family			2.5	3.4		
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 50 Ω to GND	74 Family			2.7	3.4		
		V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = MAX		0.26	0.4				
I _I Input current at maximum input voltage	4	V _{CC} = MAX, V _I = 5.5 V			1				mA
I _{IH} High-level input current	4	V _{CC} = MAX			40				μA
		V _{IH} = 2.7 V			100				
I _{IL} Low-level input current	5	V _{CC} = MAX			-1.6				mA
		V _{IL} = 0.5 V			-4				
I _{OS} Short-circuit output current‡	6	V _{CC} = MAX			-70	-180	-50	-225	mA
		Total, outputs high			12	21	10	18	
		Total, outputs low			33	57	25	44	
I _{CC} Supply current	7	V _{CC} = 5 V, 50% duty cycle			5.63				mA
		Average per gate					8.75		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, TA = 25 °C.

§ I_I = -12 mA for '128 and -18 mA for 'S140.

¶ Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second for '128 or 100 milliseconds for 'S140.

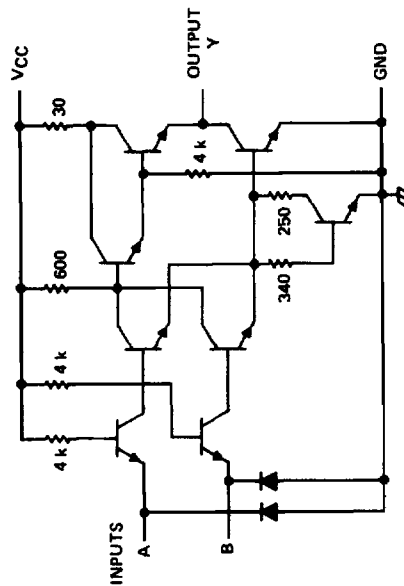
50-OHM/75-OHM LINE DRIVERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t_{PLH} (ns)		Propagation delay time, high-to-low-level output	
		MIN	TYP	MAX	TYP
'128	$C_L = 50\text{ pF}$, $R_L = 133\ \Omega$	6	9	8	12
	$C_L = 150\text{ pF}$, $R_L = 133\ \Omega$	10	15	12	18
'S140	$C_L = 50\text{ pF}$, $R_L = 93\ \Omega$	4	6.5	4	6.5
	$C_L = 150\text{ pF}$, $R_L = 93\ \Omega$	6	6	6	6

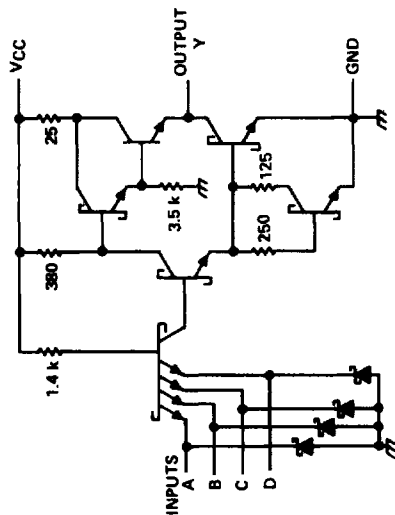
#Load circuit and voltage waveforms are shown on page 3-10.

schematics (each driver)



'128 CIRCUITS

Resistor values shown are nominal and in ohms.



'S140 CIRCUITS

SERIES 54/74

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54' SERIES 74'												UNIT
		'06, '07			'16, '17			'26			'33, '38			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
High-level output voltage, V_{OH}		4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Low-level output current, I_{OL}				30			30			30			16	48
Operating free-air temperature, T_A		-55		125	-55		125	-55		125	-55		125	°C
		0		70	0		70	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54' SERIES 74'												UNIT
			'06, '07			'16, '17			'26			'33, '38			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH} High-level input voltage	1, 2		2		2		2		2		2		2	V	
V_{IL} Low-level input voltage	1, 2				0.8		0.8		0.8		0.8		0.8	V	
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5		-1.5		-1.5		-1.5		-1.5	V	
I_{OH} High-level output current	1	$V_{CC} = \text{MIN}, V_I = A$			250		250		250		250		250	µA	
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_I = A$			0.4		0.4		0.4		0.4		0.4	V	
I_I Input current at maximum input voltage	4	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1		1		1		1		1	mA	
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}, V_{IH} = 2.4 \text{ V}$			40		40		40		40		40	µA	
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$			-1.8		-1.8		-1.8		-1.8		-1.8	mA	
I_{CC} Supply current	7	$V_{CC} = \text{MAX}$												mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ The input voltage is $V_{IH} = 2 \text{ V}$ or $V_{IL} = V_{IL \text{ max}}$, as appropriate. See tables with test figures 1 and 2.

See table on next page

SERIES 54/74 BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t_{PLH} (ns)		t_{PHL} (ns)	
		TYP	MAX	TYP	MAX
'06, '16	$C_L = 15\text{ pF}$, $R_L = 110\ \Omega$	10	15	15	23
'07, '17		6	10	20	30
'26	$C_L = 15\text{ pF}$, $R_L = 1\text{ k}\Omega$	16	24	11	17
'33	$C_L = 50\text{ pF}$, $R_L = 133\ \Omega$	10	15	12	18
'38	$C_L = 150\text{ pF}$, $R_L = 133\ \Omega$	15	22	16	24
	$C_L = 45\text{ pF}$, $R_L = 133\ \Omega$	14	22	11	18

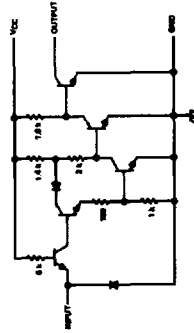
#Load circuit and voltage waveforms are shown on page 3-10.

supply current[†]

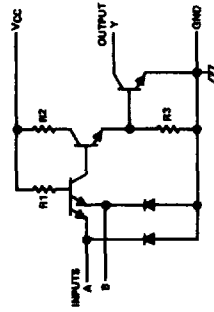
TYPE	I_{CCH} (mA)		I_{CCL} (mA)		I_{CC} (mA)	
	TYP	MAX	TYP	MAX	Average per gate (50% duty cycle)	
'06, '16	30	48	32	51	5.17	
'07, '17	29	41	21	30	4.17	
'26	4	8	12	22	2.00	
'33	12	21	33	57	5.63	
'38	5	8.5	34	54	4.88	

†Maximum values of I_{CC} shown are over the recommended operating range of V_{CC} and T_A ; typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

schematics (each gate)

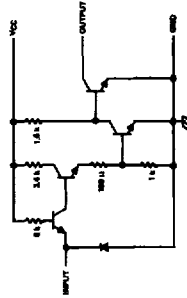


'06, '16 CIRCUITS

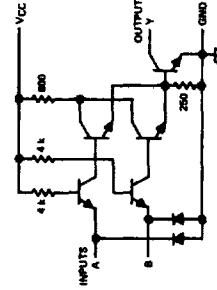


'26, '38 CIRCUITS

CIRCUITS	R1	R2	R3
'26	4 k Ω	1.5 k Ω	1 k Ω
'38	4 k Ω	600 Ω	400 Ω



'07, '17 CIRCUITS



'33 CIRCUITS

SERIES 54LS/74LS AND SERIES 54S/74S BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54LS [†] SERIES 74LS [†]						SERIES 54S [‡] SERIES 74S [‡]		UNIT				
		'LS26		'LS33		'LS38		'S38						
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM		MAX			
Supply voltage, V _{CC}		4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	5	5.5	V	
High-level output voltage, V _{OH}		4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Low-level output current, I _{OL}				15			5.5			5.5			5.5	V
Operating free-air temperature, T _A				4			12			12			80	mA
				8			24			24			60	mA
				-65			125			-55			125	°C
				0			70			0			70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	SERIES 54LS [†] SERIES 74LS [†]						SERIES 54S [‡] SERIES 74S [‡]		UNIT			
			'LS26		'LS33		'LS38		'S38					
			MIN	TYP [§]	MAX	MIN	TYP [§]	MAX	MIN	TYP [§]		MAX		
V _{IH} High-level input voltage	1, 2		2		2		2		2		2		V	
V _{IL} Low-level input voltage	1, 2			0.7		0.7		0.7		0.7		0.8	V	
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = 8			0.8		0.8		0.8		0.8		0.8	V
I _{OH} High-level output current	1	V _{CC} = MIN, I _I = 8 V _I = Δ			-1.5		-1.5		-1.5		-1.5		-1.2	V
					50								μA	
					1000								250	μA
V _{OL} Low-level output voltage	2	V _{CC} = MIN, I _{OL} = MAX V _I = Δ			0.25		0.4		0.25		0.4		0.5	V
					0.35		0.5		0.35		0.5		0.5	V
					0.25		0.4		0.25		0.4		0.4	V
I _I Input current at maximum input voltage	4	V _{CC} = MAX V _I = 7 V			0.1		0.1		0.1		0.1		1	mA
I _{IH} High-level input current	4	V _{CC} = MAX V _{IH} = 2.7 V			20		20		20		20		100	μA
I _{IL} Low-level input current	5	V _{CC} = MAX V _{IL} = 0.4 V			-0.4		-0.4		-0.4		-0.4		-4	mA
I _{CC} Supply current	7	V _{CC} = MAX												mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] I_I = -18 mA for SN54LS/SN74LS[†] and -12 mA for SN54S/SN74S[‡].

^Δ The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.

See table on next page

SERIES 54LS/74LS AND SERIES 54S/74S BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	Φ_{LH} (ns)		Propagation delay time, high-to-low-level output	
		TYP	MAX	TYP	MAX
'LS26	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	17	32	15	28
'LS33	$C_L = 45\text{ pF}$, $R_L = 687\ \Omega$	20	32	18	28
'LS38	$C_L = 50\text{ pF}$, $R_L = 93\ \Omega$	6.5	10	6.5	10
'S38	$C_L = 150\text{ pF}$	9		8.5	

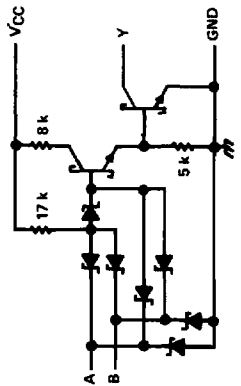
Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

supply current†

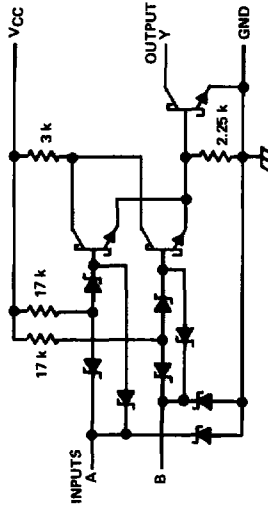
TYPE	I_{CCH} (mA)		I_{CCL} (mA)		I_{CC} (mA)	
	TYP	MAX	TYP	MAX	Average per gate (50% duty cycle)	
'LS26	0.8	1.6	2.4	4.4	0.4	
'LS33	1.8	3.6	6.9	13.8	1.09	
'LS38	0.9	2	6	12	0.88	
'S38	20	36	46	80	8.25	

† Maximum values of I_{CC} shown are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

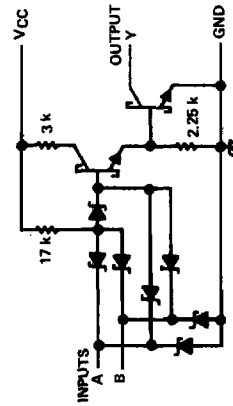
schematics (each gate)



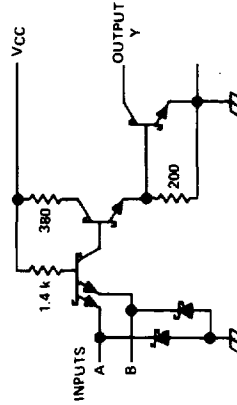
'LS26 CIRCUITS



'LS33 CIRCUITS



'LS38 CIRCUITS



'S38 CIRCUITS

POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

PARAMETER	TEST FIGURE	TEST CONDITIONS ¹	SERIES 54 SERIES 74		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN		TYP
Supply voltage, V _{CC}			4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.25
High-level output current, I _{OH}			4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25
Low-level output current, I _{OL}					-800			-400			-1000			μA
Operating free-air temperature, T _A					16			4			20			mA
					16			8			20			mA
					125			125			125			125
					0			0			0			0
					70			70			70			70

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS ¹	SERIES 54 SERIES 74		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		SERIES 54LS SERIES 74LS		SERIES 54S SERIES 74S		UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	
V _{IH} High-level input voltage	1, 2		2		0.8			0.7					0.8
V _{IL} Low-level input voltage	1, 2				0.8			0.8					0.8
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = 5			-1.5			-1.5					-1.2
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = MAX	2.4	3.4		2.5	3.4		2.5	3.4		2.5	3.4
V _{OL} Low-level output voltage	2	V _{CC} = MIN, I _{OL} = MAX, V _{IL} = V _{IL max}	0.2	0.4		0.25	0.4		0.25	0.4		0.25	0.4
I _I Input current at maximum input voltage	4	V _{CC} = MAX			1			0.1					1
I _{IH} High-level input current	4	V _{IH} = 2.4 V			40			20					50
I _{IL} Low-level input current	5	V _{IL} = 0.4 V			-1.6			-0.4					-2
I _{OS} Short-circuit output current [‡]	6	V _{CC} = MAX	-20	-55	-20	-55	-20	-100	-40	-100	-40	-100	-100
I _{CC} Supply current	Total, output high		15	22	15	22	3.1	6.2	18	32	18	32	32
	Total, output low		23	38	23	38	4.9	9.8	38	68	38	68	68
Average per gate			4.75				1.0						7

¹For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡]I_{OL} = -12 mA for SN64/SN74[†] and -18 mA for SN64LS/SN74LS[†] and SN64S/SN74S[†].

[†]Not more than one output should be shorted at a time, and for SN64LS/SN74LS[†] and SN64S/SN74S[†], duration of the short-circuit should be less than one second.

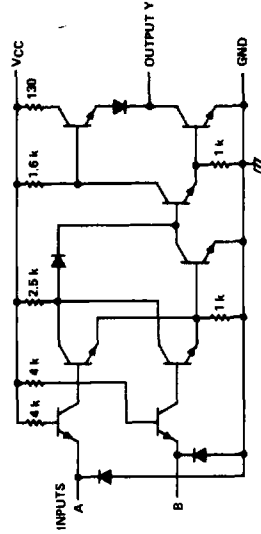
POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS

schematics (each gate)

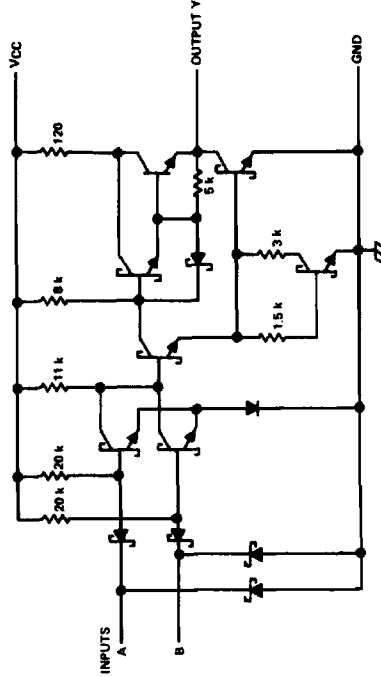
switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t_{PLH} (ns)		Propagation delay time, low-to-high-level output		t_{PHL} (ns)	
		MIN	TYP	MAX	MIN	TYP	MAX
'32	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$	10	15	14	14	22	22
'LS32	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	14	22	14	14	22	22
'S32	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$	4	7	4	4	7	7
	$C_L = 50\text{ pF}$, $R_L = 280\ \Omega$	5		5		5	

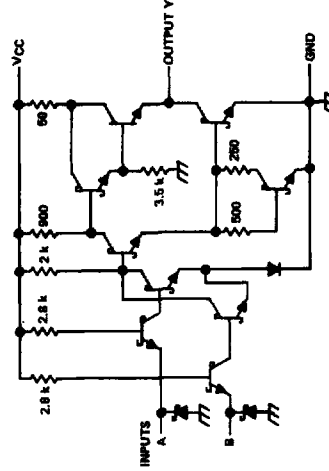
#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.



'32 CIRCUITS



'LS32 CIRCUITS



'S32 CIRCUITS

Resistor values shown are nominal and in ohms.



AND-OR-INVERT GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

PARAMETER	TEST FIGURE	TEST CONDITIONS ¹	SERIES 54		SERIES 54H		SERIES 54L		SERIES 54LS		SERIES 54S		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V _{CC}	1, 2		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
High-level output current, I _{OH}	3		4.75	5	4.75	5	4.75	5	4.75	5	4.75	5	mA
Low-level output current, I _{OL}	4		-400	-400	-500	-500	-200	-400	-400	-400	-1000	-1000	mA
Operating free-air temperature, T _A	7		0	70	0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS ¹	SERIES 54		SERIES 54H		SERIES 54L		SERIES 54LS		SERIES 54S		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{IH}	1, 2		2	2	2	2	2	2	2	2	2	V	
V _{IL}	1, 2		0.8	0.8	0.8	0.8	0.7	0.7	0.7	0.7	0.8	V	
V _{IK}	3	V _{CC} = MIN, I ₁ = 8	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.2	V	
V _{OH}	1	V _{CC} = MIN, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4	3.4	2.4	3.4	2.4	3.3	2.5	3.4	2.5	3.4	V
V _{OL}	2	V _{CC} = MIN, V _{IH} = 2 V	0.2	0.4	0.2	0.4	0.15	0.3	0.25	0.4	0.25	0.4	V
I ₁	4	V _{CC} = MAX, I ₁ = 7 V	1	1	1	1	0.1	0.1	0.1	0.1	0.1	0.1	mA
I _{IH}	4	V _{CC} = MAX, V _{IH} = 2.4 V	40	50	50	50	10	10	20	20	50	50	μA
I _{IL}	5	V _{CC} = MAX, V _{IL} = 0.4 V	-1.8	-2	-2	-2	-0.18	-0.18	-0.4	-0.4	-0.4	-0.4	mA
I _{OS}	6	V _{CC} = MAX	-20	-55	-40	-100	-3	-15	-20	-100	-40	-100	mA
I _{CC}	7	V _{CC} = MAX	-18	-85	-40	-100	-3	-15	-20	-100	-40	-100	mA

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

² All typical values are at V_{CC} = 5 V, T_A = 25°C.

³ I₁ = -12 mA for SN54/SN74*, -8 mA for SN54H/SN74H*, and -18 mA for SN54LS/SN74LS* and SN54S/SN74S*.

Not more than one output should be shorted at a time, and for SN54LS/SN74LS, SN54H/SN74H*, and SN54S/SN74S*, duration of the short-circuit should not exceed one second.

See table on next page

AND-OR-INVERT GATES WITH TOTEM-POLE OUTPUTS

switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

TYPE	TEST CONDITIONS#	t_{PLH} (ns)		Propagation delay time, low-to-high-level output		t_{PHL} (ns)	
		MIN	TYP	MAX	MIN	TYP	MAX
'51, '54	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$	13	22	8	15	8	15
'H51	$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$	6.8	11	6.2	11	6.2	11
'H54	$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$	7	11	6.2	11	6.2	11
'L51, 'L54, 'L55	$C_L = 50\text{ pF}$, $R_L = 4\text{ k}\Omega$	50	90	35	60	35	60
'LS51, 'LS55	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	12	20	12.5	20	12.5	20
'LS54	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	12	20	12.5	20	12.5	20
'S51, 'S64	$C_L = 15\text{ pF}$, $R_L = 280\ \Omega$	3.5	5.5	3.5	5.5	3.5	5.5
	$C_L = 50\text{ pF}$, $R_L = 280\ \Omega$	5	5	5	5	5	5

Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

supply current†

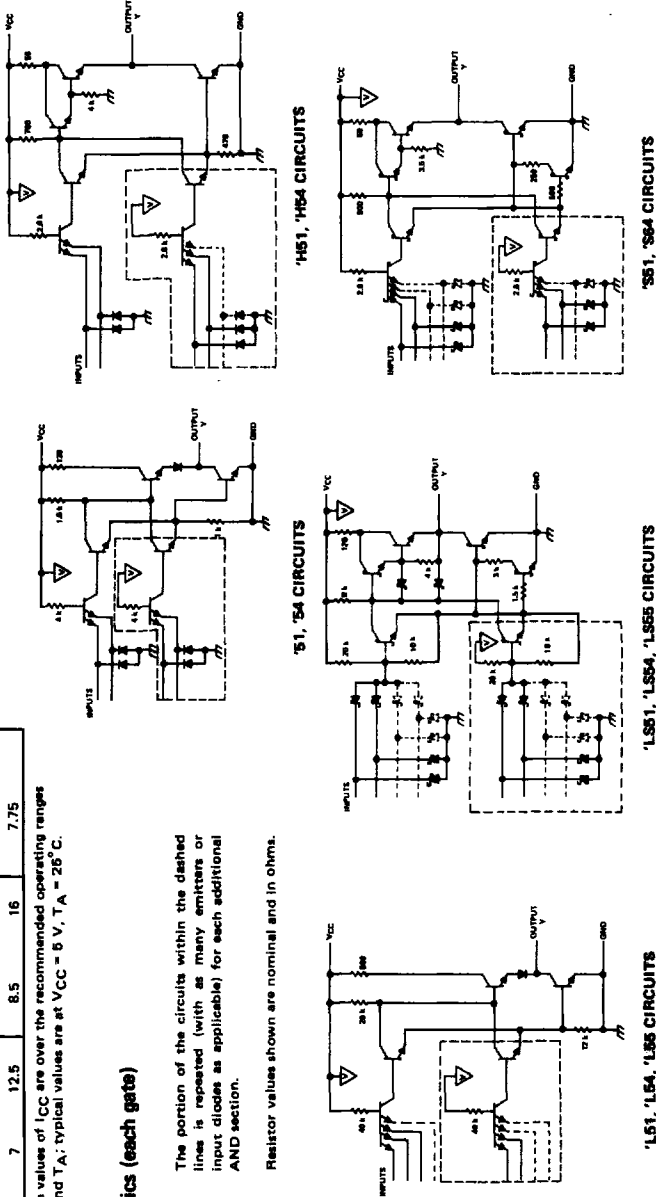
TYPE	I_{CCH} (mA)		I_{CCL} (mA)		I_{CC} (mA)	
	TYP	MAX	TYP	MAX	Average per AOI gate (50% duty cycle)	TYP
'51	4	8	7.4	14	2.85	2.85
'54	4	8	5.1	9.5	4.55	4.55
'H51	8.2	12.8	15.2	24	5.85	5.85
'H54	7.1	11	9.4	14	8.25	8.25
'L51	0.44	0.8	0.76	1.3	0.30	0.30
'L54	0.39	0.8	0.60	0.99	0.50	0.50
'L55	0.22	0.4	0.38	0.65	0.30	0.30
'LS51	0.8	1.6	1.4	2.8	0.55	0.55
'LS54	0.8	1.6	1.0	2	0.9	0.9
'LS55	0.4	0.8	0.7	1.3	0.55	0.55
'S51	5.2	17.8	13.6	22	5.45	5.45
'S64	7	12.5	8.5	16	7.75	7.75

† Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

schematics (each gate)

The portion of the circuits within the dashed lines is repeated (with as many emitters or input diodes as applicable) for each additional AND section.

Resistor values shown are nominal and in ohms.



AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

	'S65			'S74S65			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	'S65			LIMIT	
			MIN	TYP‡	MAX		
V_{IH} High-level input voltage	1, 2		2			V	
V_{IL} Low-level input voltage	1, 2				0.8	V	
V_{IK} Input clamp voltage	3	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V	
I_{OH} High-level output current	1	$V_{CC} = \text{MIN}, V_{IH} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$			250	μ A	
V_{OL} Low-level output voltage	2	$V_{CC} = \text{MIN}, V_{IL} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V	
I_I Input current at maximum input voltage	4	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA	
I_{IH} High-level input current	4	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	μ A	
I_{IL} Low-level input current	5	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA	
I_{CCH} Supply current, output high	7	$V_{CC} = \text{MAX}$			6	11	mA
I_{CCL} Supply current, output low	7	$V_{CC} = \text{MAX}$			8.5	16	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

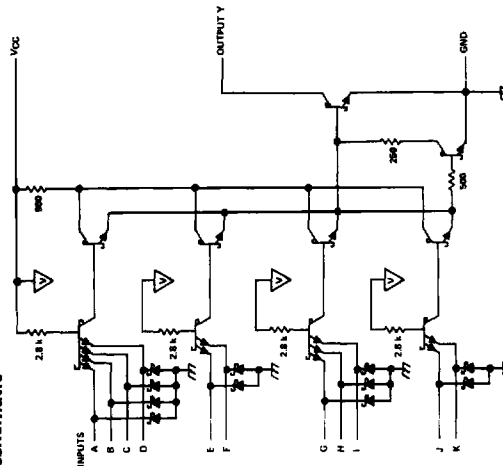
‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS#	'S65			UNIT
		MIN	TYP	MAX	
Propagation delay time, t_{pLH} low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 280 \Omega$	2	5	7.5	ns
Propagation delay time, t_{pHL} high-to-low-level output	$C_L = 50 \text{ pF}, R_L = 280 \Omega$	2	8	8	ns
	$C_L = 15 \text{ pF}, R_L = 280 \Omega$	2	5.5	8.5	ns
	$C_L = 50 \text{ pF}, R_L = 280 \Omega$		6.5		ns

Load circuit and voltage waveforms are shown on page 3-10.

schematic



Resistor values shown are nominal and in ohms.

GATES WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 64		SERIES 64LS		SERIES 64S		SERIES 74S		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V _{CC}	1, 2	54 Family 74 Family	'126, '126A, '426, '426A		'126, '126A, '426, '426A		'126, '126A, '426, '426A		'126, '126A, '426, '426A		V
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
High-level output current, I _{OH}	1	54 Family 74 Family	4.5, 5, 5.5, 6, 6.5, 7.5		4.5, 5, 5.5, 6, 6.5, 7.5		4.5, 5, 5.5, 6, 6.5, 7.5		4.5, 5, 5.5, 6, 6.5, 7.5		mA
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Low-level output current, I _{OL}	2	54 Family 74 Family	-5.2		-5.2		-5.2		-5.2		mA
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Operating free-air temperature, T _A	7	54 Family 74 Family	0, 70		0, 70		0, 70		0, 70		°C
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 64		SERIES 64LS		SERIES 64S		SERIES 74S		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{IH} High-level input voltage	1, 2	54 Family	0.8		0.7		0.8		0.8		V
V _{IL} Low-level input voltage	1, 2	74 Family	0.8		0.8		0.8		0.8		V
V _{IK} Input clamp voltage	3	I _I = §	-1.5		1.5		2.4, 3.2		-1.2		V
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4, 3.1		2.4		2.4, 3.2		2.4, 3.2		V
V _{OL} Low-level output voltage	2	V _{CC} = MIN, I _{OL} = MAX	0.4		0.25, 0.4		0.25, 0.4		0.5		V
		V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 12 mA	0.4		0.35, 0.6		0.25, 0.4		0.5		
I _{OZ} Off-state (high-impedance state) output current	19	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{IL} max	-40		-20		-20		-90		µA
		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	-40		-20		-20		-90		
I _I Input current at maximum input voltage	4	V _I = 5.5 V, V _I = 7 V	1		0.1		1		1		mA
I _{IH} High-level input current	4	V _{CC} = MAX, V _{IH} = 2.4 V, V _{IL} = 0.4 V	40		20		40		80		µA
I _{IL} Low-level input current	5	V _{CC} = MAX, V _{IH} = 2.4 V, V _{IL} = 0.4 V	-1.6		0.4		-1.6		-2		mA
I _{OS} Short-circuit output current [¶]	6	V _{CC} = MAX	-30		-40		-225		-40		mA
I _{CC} Supply current	7	V _{CC} = MAX	-70		-40		-225		-40		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25° C.

§ I_I = -12 mA for SN54/SN74* and -18 mA for SN64LS/SN74LS* and SN54S/SN74S*.

¶ Not more than one output should be shorted at a time, and for SN64LS/SN74LS* and SN54S/SN74S*, duration of the short circuit should not exceed one second.

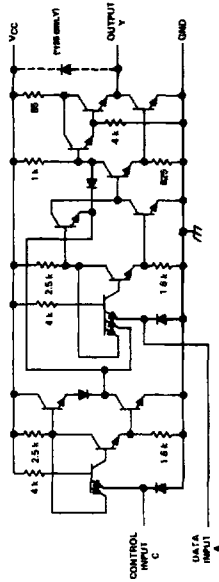
GATES WITH 3-STATE OUTPUTS

supply current[†]

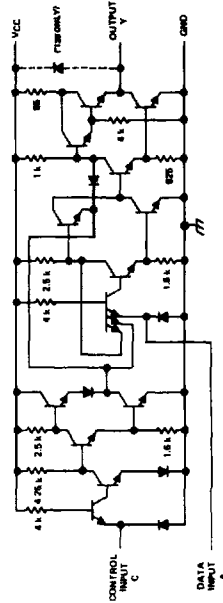
TYPE	TEST CONDITIONS		I _{CC} (mA)	
	DATA INPUTS	OUTPUT CONTROLS	MIN	MAX
'125, '425	0 V	4.5 V	32	54
'126, '426	0 V	0 V	36	62
'LS125A	0 V	4.5 V	11	20
'LS126A	0 V	0 V	12	22
'S134	0 V	0 V	7	13
	5 V	0 V	9	16
	5 V	5 V	14	25

[†] Maximum value of I_{CC} are over the recommended operating range of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)



'125A, '425 CIRCUITS



'126A, '426 CIRCUITS

Resistor values shown are nominal and in ohms.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	SERIES 64/74			SERIES 64LS/74LS			SERIES 54S/74S			UNIT		
	TEST CONDITIONS#	'125, '425 TYP	'426 TYP	TEST CONDITIONS#	'LS125A TYP	'LS126A TYP	TEST CONDITIONS#	'S134 TYP	'S134 TYP			
t _{PLH} Propagation delay time, low-to-high-level output	C _L = 50 pF, R _L = 400 Ω	8	13	8	13	9	15	9	15	C _L = 15 pF, R _L = 280 Ω	4	6
		12	18	12	18	7	18	8	18	7	C _L = 60 pF, R _L = 280 Ω	5
t _{PHL} Propagation delay time, high-to-low-level output	C _L = 50 pF, R _L = 400 Ω	11	17	11	18	12	20	16	25	C _L = 15 pF, R _L = 280 Ω	5	7.5
		18	25	16	25	15	25	21	35	20	C _L = 60 pF, R _L = 280 Ω	7
t _{PZH} Output enable time to high level	C _L = 5 pF, R _L = 400 Ω	5	8	10	16	20	20	20	20	C _L = 50 pF, R _L = 280 Ω	13	19.5
t _{PZL} Output enable time to low level		7	12	12	18	18	18	18	18	18	C _L = 50 pF, R _L = 280 Ω	14
t _{PZH} Output disable time from high level	C _L = 5 pF, R _L = 400 Ω	5	8	10	16	20	20	20	20	C _L = 5 pF, R _L = 280 Ω	5.5	8.5
t _{PZL} Output disable time from low level		7	12	12	18	18	18	18	18	18	C _L = 5 pF, R _L = 280 Ω	9

Load circuit and voltage waveforms are shown on page 3-10 and 3-11.

HEX BUS DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	TEXT FIGURE	TEST CONDITIONS ¹	SERIES 64		SERIES 74		SERIES 84		SERIES 74LS		SERIES 74ALS		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, VCC			4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V	
High-level output current, I _{OH}			4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	mA	
Low-level output current, I _{OL}					-5.2			-2.6			-2.6	mA	
Operating free-air temperature, T _A			-55	125	-55	125	-55	125	-55	125	125	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEXT FIGURE	TEST CONDITIONS ¹	SERIES 64		SERIES 74		SERIES 84		SERIES 74LS		SERIES 74ALS		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{IH} High-level input voltage	1, 2				0.8							0.7	V
V _{IL} Low-level input voltage	1, 2				0.8							0.8	V
V _{IK} Input clamp voltage	3	VCC = MIN, I _I = 8			-1.5							-1.5	V
V _{OH} High-level output voltage	1	VCC = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4	3.3	2.4	3.3	2.4	3.3	2.4	3.3	2.4	3.3	V
V _{OL} Low-level output voltage	2	VCC = MIN, I _{OL} = MAX			0.4				0.25	0.4	0.25	0.4	V
I _{OZ} Off-state (high-impedance state) output current	19	V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OL} = 12 mA			40				0.36	0.6	0.25	0.4	µA
I _I Input current at maximum input voltage	4	V _{IH} = 2 V, V _{IL} = V _{IL} max			-40				1			-20	µA
I _{IH} High-level input current	4	VCC = MAX			40				0.1			0.1	mA
I _{IL} Low-level input current	4	VCC = MAX, V _I = 0.5 V, Either G input at 2 V			-40				20			20	µA
I _{IS} Short-circuit output current ²	6	VCC = MAX, V _I = 0.4 V, Both G inputs at 0.4 V			-1.6				-0.4			-0.4	mA
I _{CC} Supply current	7	VCC = MAX			-40				-130			-40	mA

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

² All typical values are at VCC = 5 V, T_A = 25°C.

³ I_I = -12 mA for SN64/SN74 and -18 mA for SN84LS/SN74LS and SN84/SN74S.

⁴ Not more than one output should be shorted at a time, and for SN84LS/SN74LS and SN84/SN74S, duration of output short-circuit should not exceed one second.

HEX BUS DRIVERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$, see note 1

supply current[†]

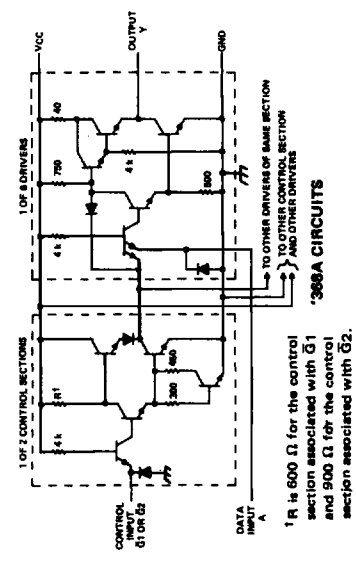
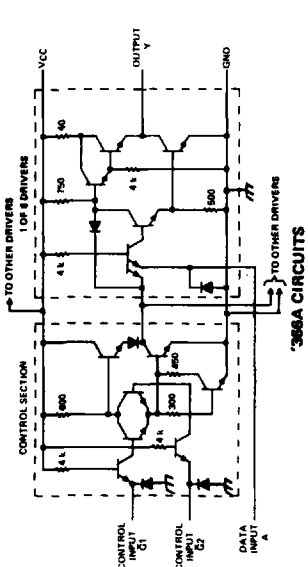
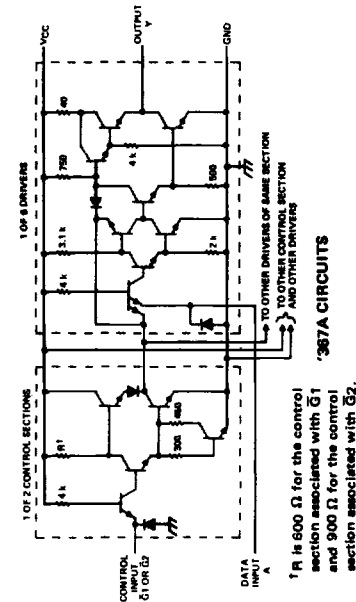
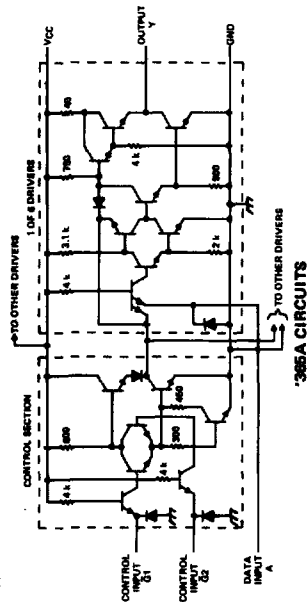
TYPE	DATA INPUTS	OUTPUT CONTROLS	I_{CC} (mA)	
			TYP	MAX
'386A, '387A	0 V	4.5 V	66	85
'386A, '388A	0 V	4.5 V	58	77
'LS386A, 'LS387A	0 V	4.5 V	14	24
'LS386A, 'LS388A	0 V	4.5 V	12	21

† Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

PARAMETER*	TEST CONDITIONS		SERIES 94L874LS		SERIES 94L874LS	
	TYP	MAX	'386A, '387A TYP	'386A, '388A TYP	'LS386A, 'LS387A TYP	'LS386A, 'LS388A TYP
t_{PLH}	18	17	10	16	7	15
t_{PHL}	22	18	9	22	12	18
t_{PZH}	35	35	19	35	18	35
t_{PZL}	37	37	24	40	28	45
t_{PHZ}	11	11	30	30	30	32
t_{PLZ}	27	27	35	35	35	35

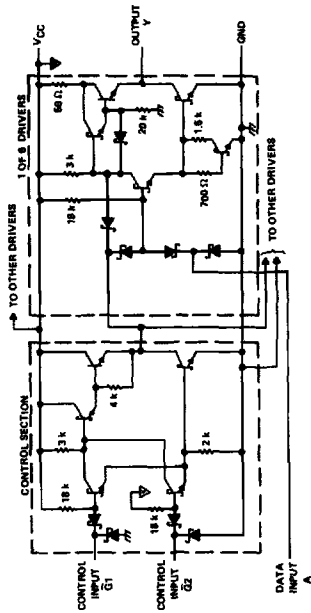
* t_{PLH} = Propagation delay time, low-to-high-level output
 t_{PHL} = Propagation delay time, high-to-low-level output
 t_{PZH} = Output enable time to high level
 t_{PZL} = Output disable time to low level
 t_{PHZ} = Propagation delay time, low-to-high-level output
 t_{PLZ} = Output disable time from high level
 t_{PLZ} = Output disable time from low level
 NOTE 1: Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

schematics

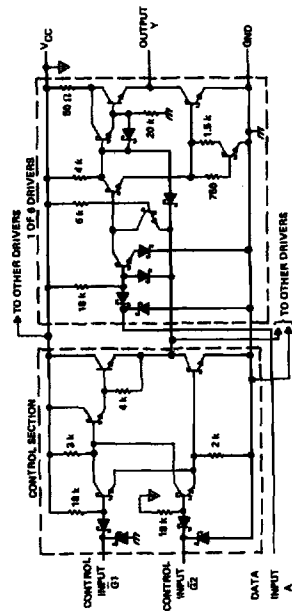


Resistor values shown are nominal and in ohms.

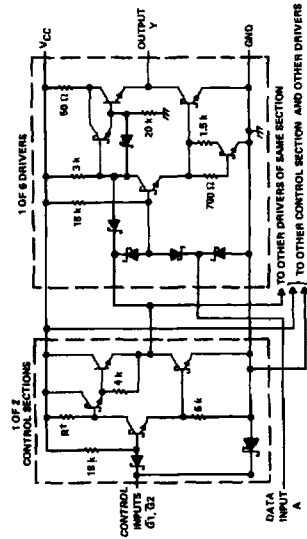
HEX BUS DRIVERS WITH 3-STATE OUTPUTS



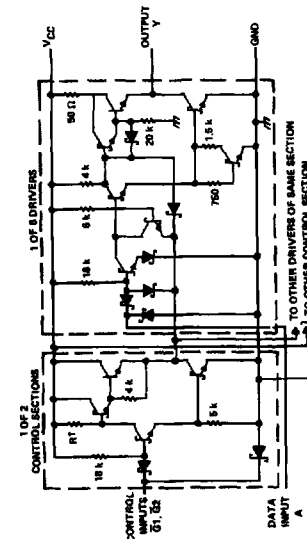
'LS366A CIRCUITS



'LS366A CIRCUITS



'LS368A CIRCUITS



'LS367A CIRCUITS

† R is 5 kΩ for the control section associated with G1 and 8 kΩ for the control section associated with G2.

† R is 5 kΩ for the control section associated with G1 and 8 kΩ for the control section associated with G2.

Resistor values shown are nominal and in ohms

recommended operating conditions

PARAMETER	TEST FIGURE	SERIES 54 SERIES 74						SERIES 64H SERIES 74H			UNIT
		'23		'50, '53		'H50, 'H52, 'H53, 'H55		MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
High-level output current, I _{OH}		4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	μA
Low-level output current, I _{OL}				-800			-400			-500	μA
Operating free-air temperature range, T _A	54 Family			16			16			20	°C
	74 Family			16			16			20	°C
Operating free-air temperature range, T _A	54 Family	-55	125	-55	125	-55	125	-55	125	-55	°C
	74 Family	0	70	0	70	0	70	0	70	0	°C

The '23, '50, and '53 are designed for use with up to four '60 expanders.
 The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.
 The 'H52 is designed for use with up to six 'H61 expanders.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54 SERIES 74			SERIES 64H SERIES 74H			UNIT
			'23	'50, '53	'H50, 'H52, 'H53, 'H55	MIN	TYP‡	MAX	
V _{IH} High-level input voltage	1, 2		2	2	2	0.8	0.8	0.8	V
V _{IL} Low-level input voltage	1, 2					-1.5	-1.5	-1.5	V
V _{IK} Input clamp voltage	3	V _{CC} = MIN, I _I = §							V
V _{OH} High-level output voltage	1	V _{CC} = MIN, V _I = Δ, I _{OH} = MAX	2.4	3.4	2.4	3.4	2.4	3.4	V
V _{OL} Low-level output voltage	2	V _{CC} = MIN, V _I = Δ, I _{OL} = MAX	0.2	0.4	0.2	0.4	0.2	0.4	V
I _I Input current at maximum input voltage	4	V _{CC} = MAX, V _I = 5.5 V		1		1		1	mA
I _{IH} High-level input current	Data input	V _{CC} = MAX, V _{IH} = 2.4 V		40		40		50	μA
	Strobe of '23			160		160			μA
I _{IL} Low-level input current	Data input	V _{CC} = MAX, V _{IL} = 0.4 V		-1.6		-1.6		-2	mA
	Strobe of '23			-6.4		-6.4			mA
I _{OS} Short-circuit output current*	54 Family	V _{CC} = MAX	-20	-55	-20	-55	-40	-100	mA
	74 Family	V _{CC} = MAX	-18	-55	-18	-55	-40	-100	mA
I _{CC} Supply current	7	V _{CC} = MAX							mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN54/SN74* and -8 mA for SN54H/SN74H*.

* The input voltage is V_{IH} = 2 V or V_{IL} = V_{IH} max, as appropriate. See tables with test figures 1 and 2.

† Not more than one output should be shorted at a time, and for the SN54H/SN74H*, duration of short-circuit should not exceed one second.

See table on next page

EXPANDABLE GATES

electrical characteristics using expander inputs, $V_{CC} = \text{MIN}$, $T_A = \text{MIN}$ (unless otherwise noted)

TYPE	$I_{X'} \text{ (mA)}$ (I_X for 'H62) Expander current		$V_{BE(Q)} \text{ (V)}$ Base-emitter voltage of output transistor Q		$V_{OH} \text{ (V)}$ High-level output voltage		$V_{OL} \text{ (V)}$ Low-level output voltage		
	TEST CONDITIONS	MIN TYP [‡] MAX	TEST CONDITIONS	MIN TYP [‡] MAX	TEST CONDITIONS	MIN TYP [‡] MAX	TEST CONDITIONS	MIN TYP [‡] MAX	
SN5423	$V_{XX} = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$, See Figure 10	-3.5 -2.9 -2.9	$I_X + I_{X'} = 410 \mu\text{A}$, $R_{XX} = 0$, $I_{OL} = 16 \text{ mA}$, See Figure 11	1:1	$I_X = 150 \mu\text{A}$, $I_{X'} = -150 \mu\text{A}$, $I_{OH} = -400 \mu\text{A}$, See Figure 12	2.4	$I_X + I_{X'} = 300 \mu\text{A}$, $R_{XX} = 114 \Omega^*$, $I_{OL} = 16 \text{ mA}$, See Figure 11	0.2	0.4
SN7423	$V_{XX} = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$, See Figure 10	-3.8 -3.1 -3.1	$I_X + I_{X'} = 620 \mu\text{A}$, $R_{XX} = 0$, $I_{OL} = 16 \text{ mA}$, See Figure 11	1	$I_X = 270 \mu\text{A}$, $I_{X'} = -270 \mu\text{A}$, $I_{OH} = -400 \mu\text{A}$, See Figure 12	2.4	$I_X + I_{X'} = 430 \mu\text{A}$, $R_{XX} = 105 \Omega^*$, $I_{OL} = 16 \text{ mA}$, See Figure 11	0.2	0.4
SN54H50, SN54H53, SN54H55	$V_{X'} = 1.4 \text{ V}$, $I_X = 0$, $I_{OL} = 0$, See Figure 10	-5.85	$I_X + I_{X'} = 700 \mu\text{A}$, $R_{XX} = 0$, $I_{OL} = 20 \text{ mA}$, See Figure 11	1:1	$I_X = 320 \mu\text{A}$, $I_{X'} = -320 \mu\text{A}$, $I_{OH} = -500 \mu\text{A}$, See Figure 12	2.4	$I_X + I_{X'} = 470 \mu\text{A}$, $R_{XX} = 88 \Omega$, $I_{OL} = 20 \text{ mA}$, See Figure 11	0.2	0.4
SN74H50, SN74H53, SN74H55	$V_{X'} = 1.4 \text{ V}$, $I_X = 0$, $I_{OL} = 0$, See Figure 10	-6.3	$I_X + I_{X'} = 1.1 \text{ mA}$, $R_{XX} = 0$, $I_{OL} = 20 \text{ mA}$, See Figure 11	1	$I_X = 570 \mu\text{A}$, $I_{X'} = -570 \mu\text{A}$, $I_{OH} = -500 \mu\text{A}$, See Figure 12	2.4	$I_X + I_{X'} = 600 \mu\text{A}$, $R_{XX} = 83 \Omega$, $I_{OL} = 20 \text{ mA}$, See Figure 11	0.2	0.4
SN54H62	$V_X = 1 \text{ V}$, $I_{OH} = -500 \mu\text{A}$, See Figure 13	-2.7 -2.9			$V_X = 1 \text{ V}$, $I_{OH} = -500 \mu\text{A}$, See Figure 13	2.4	$I_X = -300 \mu\text{A}$, $I_{OL} = 20 \text{ mA}$, $T_A = \text{MAX}$, See Figure 14	0.2	0.4
SN74H62									

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

* R_{XX} equals 114Ω for SN5423, 138Ω for SN5450 and SN5453, 105Ω for SN7423, and 130Ω for SN7450 and SN7453.

supply current[†]

TYPE	$I_{CCH} \text{ (mA)}$ Total with outputs high		$I_{CCL} \text{ (mA)}$ Total with outputs low		$I_{CC} \text{ (mA)}$ Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	TYP
'23	8	16	10	19	4.5	4.5
'50	4	8	7.4	14	2.85	2.85
'53	4	8	5.1	9.5	4.55	4.55
'H50	8.2	12.8	15.2	24	5.85	5.85
'H62	20	31	15.2	24	17.6	17.6
'H53	7.1	11	9.4	14	8.25	8.25
'H55	4.5	6.4	7.5	12	6.00	6.00

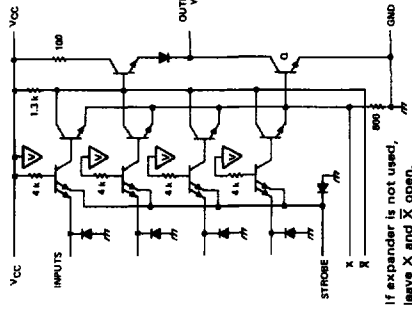
[†]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A ; typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

TYPE	TEST CONDITIONS#	t_{PLH} (ns)		t_{PHL} (ns)	
		TYP	MAX	TYP	MAX
'23, '50, '53	$C_L = 15$ pF, $R_L = 400 \Omega$, Expander pins open	13	22	8	15
'50	$C_L = 15$ pF, $R_L = 400 \Omega$, From input of '60 expander	15	30	10	20
'H60	$C_L = 25$ pF, $R_L = 280 \Omega$, Expander pins open	6.8	11	6.2	11
'H62		10.6	15	9.2	15
'H63		7	11	6.2	11
'H65		7	11	6.5	11
'H60		$C_L = 25$ pF, $R_L = 280 \Omega$, $C = 15$ pF (GND to X of	11	7.4	7.4
'H62	'H50, 'H63, or 'H65; or	11.4	7.4	7.4	7.7
'H65	to X of 'H62)	11.4	7.7	7.7	7.7

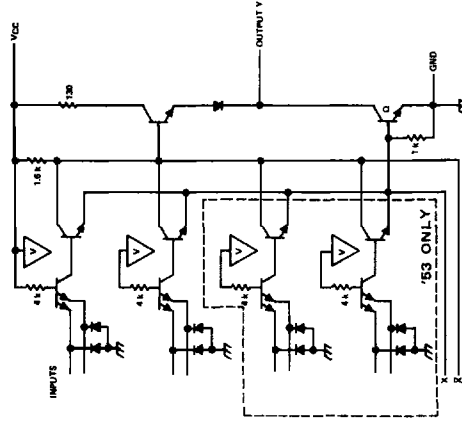
#Load circuit and voltage waveforms are shown on page 3-10.

schematics (each gate)



If expander is not used, leave X and Y open.

'23 CIRCUITS

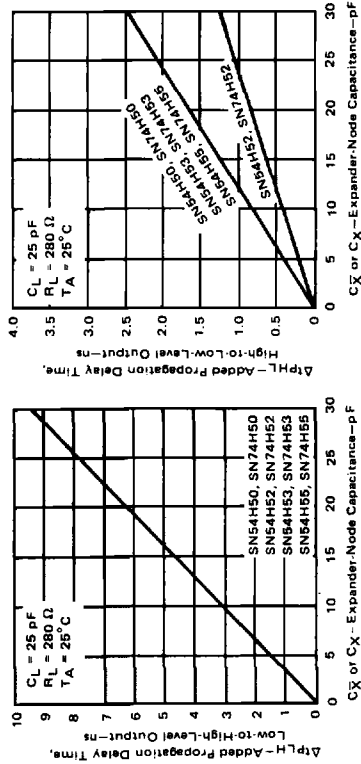


If expander is not used, leave X and Y open.

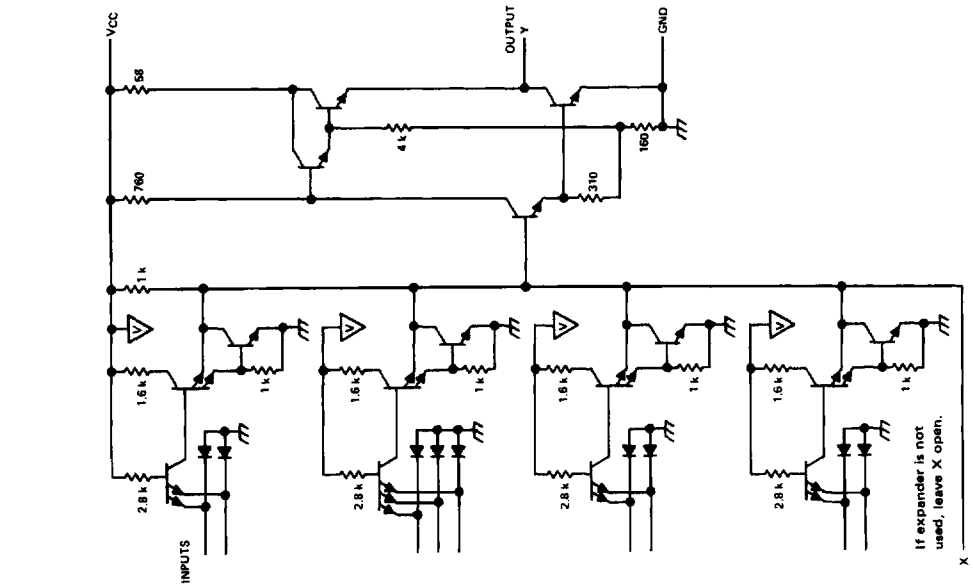
'50, '53 CIRCUITS

Resistor values shown are nominal and in ohms.

TYPICAL ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE

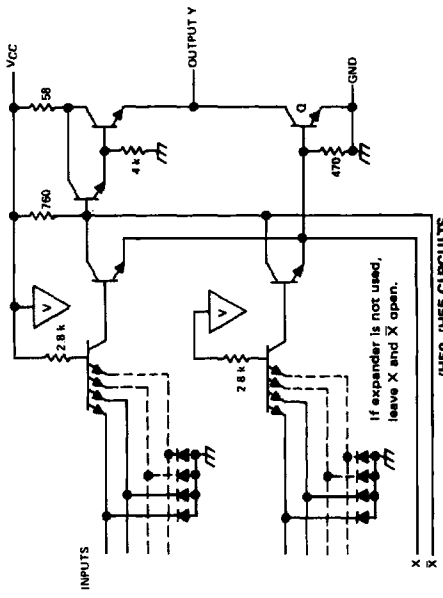


EXPANDABLE GATES

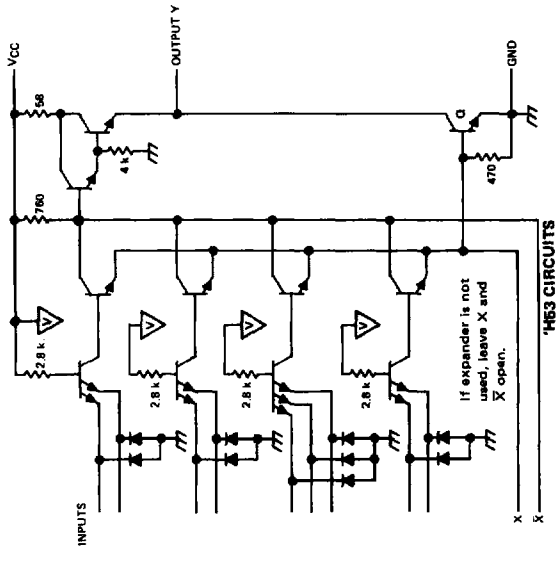


1462 CIRCUITS

Resistor values shown are nominal and in ohms.



1450, 1455 CIRCUITS



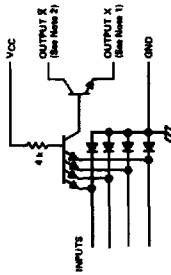
1463 CIRCUITS

recommended operating conditions

	SN5480		SN7480		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	5.5	4.75	5	5.25 V
Operating free-air temperature, T_A	-55	125	0	70	$^{\circ}$ C

The '23, '50, and '53 are designed for use with up to four '80 expanders.

schematic (each gate)



'80 CIRCUITS

- NOTES: 1. Connect to X input of '23, '50, or '53 circuit.
2. Connect to \bar{X} input of '23, '50, or '53 circuit.

Resistor value shown is nominal and in ohms.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	SN5480		SN7480		UNIT	
		TEST CONDITIONS	MIN	TYP†	MAX		TEST CONDITIONS
V_{IH} High-level input voltage	15		2			V	
V_{IL} Low-level input voltage	16		0.8			0.8 V	
$V_{XX(on)}$ On-state voltage between expander outputs	15	$V_{CC} = 4.5$ V, $V_{IH} = 2$ V, $V_X = 1.1$ V, $I_X = 3.5$ mA, $T_A = -55^{\circ}$ C		0.4	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_X = 1$ V, $I_X = 3.8$ mA, $T_A = 0^{\circ}$ C	0.4 V	
$I_X(on)$ On-state expander current	15	$V_{CC} = 4.5$ V, $V_{IH} = 2$ V, $V_X = 1.1$ V, $I_X = 0$, $T_A = -55^{\circ}$ C	-0.3		$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_X = 1$ V, $I_X = 0$, $T_A = 0^{\circ}$ C	-0.43 mA	
$I_X(off)$ Off-state expander current	16	$V_{CC} = 4.5$ V, $V_{IL} = 0.8$ V, $V_X = 4.5$ V, $R_X = 1.2$ k Ω , $T_A = -55^{\circ}$ C		150	$V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V, $V_X = 4.5$ V, $R_X = 1.2$ k Ω , $T_A = 0^{\circ}$ C	270 μ A	
I_I Input current at maximum input voltage	4	$V_{CC} = 5.5$ V, $V_I = 5.5$ V		1	$V_{CC} = 5.25$ V, $V_I = 5.5$ V	1 mA	
I_{IH} High-level input current	4	$V_{CC} = 5.5$ V, $V_I = 2.4$ V		40	$V_{CC} = 5.25$ V, $V_I = 2.4$ V	40 μ A	
I_{IL} Low-level input current	5	$V_{CC} = 5.5$ V, $V_I = 0.4$ V		-1.6	$V_{CC} = 5.25$ V, $V_I = 0.4$ V	-1.6 mA	
$I_{CC(on)}$ Supply current, expander on	7	$V_{CC} = 5.5$ V, $V_I = 4.5$ V, $V_X = 0.85$ V, $I_X = 0$	1.2	2.5	$V_{CC} = 5.25$ V, $V_I = 4.5$ V, $V_X = 0.85$ V, $I_X = 0$	1.2 2.5 mA	
$I_{CC(off)}$ Supply current, expander off	7	$V_{CC} = 5.5$ V, $V_I = 0$, $V_X = 0.85$ V, $I_X = 0$	2	4	$V_{CC} = 5.25$ V, $V_I = 0$, $V_X = 0.85$ V, $I_X = 0$	2 4 mA	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^{\circ}$ C.

EXPANDERS

recommended operating conditions

	SN64H60		SN74H60, SN74H62		UNIT
	MIN	NOM	MAX	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	5.26	V
Operating free-air temperature, T_A	-55		125	0	70 °C

See schematics
next page

The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	SN64H60, SN64H62		SN74H60, SN74H62		UNIT
		MIN	TYP† MAX	MIN	TYP† MAX	
V_{IH} High-level input voltage	15		2			V
V_{IL} Low-level input voltage	16		0.8			V
$V_{XX(on)}$ On-state voltage between expander outputs	15	$V_{CC} = 4.5\text{ V}, V_{IH} = 2\text{ V}, V_X = 1.1\text{ V}, I_X = 5.85\text{ mA}, T_A = -55^\circ\text{C}$		$V_{CC} = 4.75\text{ V}, V_{IH} = 2\text{ V}, V_X = 1\text{ V}, I_X = 6.3\text{ mA}, T_A = 0^\circ\text{C}$		0.4
		$V_{CC} = 5.5\text{ V}, V_{IH} = 2\text{ V}, V_X = 1\text{ V}, I_X = 7.85\text{ mA}, T_A = 125^\circ\text{C}$		$V_{CC} = 5.25\text{ V}, V_{IH} = 2\text{ V}, V_X = 1\text{ V}, I_X = 7.4\text{ mA}, T_A = 70^\circ\text{C}$		0.4
		$V_{CC} = 4.5\text{ V}, V_{IH} = 2\text{ V}, V_X = 1.1\text{ V}, I_X = 0, T_A = -55^\circ\text{C}$		$V_{CC} = 4.75\text{ V}, V_{IH} = 2\text{ V}, V_X = 1\text{ V}, I_X = 0, T_A = 0^\circ\text{C}$		-600
$I_X(off)$ Off-state expander current	16	$V_{CC} = 4.5\text{ V}, V_{IL} = 0.8\text{ V}, V_X = 4.5\text{ V}, R_X = 575\ \Omega, T_A = -55^\circ\text{C}$		$V_{CC} = 4.75\text{ V}, V_{IL} = 0.8\text{ V}, V_X = 4.5\text{ V}, R_X = 575\ \Omega, T_A = 0^\circ\text{C}$		320
I_I Input current at maximum input voltage	4	$V_{CC} = 5.5\text{ V}, V_I = 5.5\text{ V}$		$V_{CC} = 5.25\text{ V}, V_I = 5.5\text{ V}$		1
		$V_{CC} = 5.5\text{ V}, V_I = 2.4\text{ V}$		$V_{CC} = 5.25\text{ V}, V_I = 2.4\text{ V}$		50
		$V_{CC} = 5.5\text{ V}, V_I = 0.4\text{ V}$		$V_{CC} = 5.25\text{ V}, V_I = 0.4\text{ V}$		-2
I_{IH} High-level input current	5	$V_{CC} = 5.5\text{ V}, V_I = 4.5\text{ V}, V_X = 0.85\text{ V}, I_X = 0$		$V_{CC} = 5.25\text{ V}, V_I = 4.5\text{ V}, V_X = 0.85\text{ V}, I_X = 0$		1.9
		$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		$V_{CC} = 5.25\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		3.8
I_{IL} Low-level input current	7	$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		$V_{CC} = 5.25\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		3
		$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		$V_{CC} = 5.25\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		6
$I_{CC(on)}$ Supply current, expander on	'H60	$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		$V_{CC} = 5.25\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		5.4
		$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		$V_{CC} = 5.25\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		6.0
$I_{CC(off)}$ Supply current, expander off	'H62	$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		$V_{CC} = 5.25\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		5.4
		$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		$V_{CC} = 5.25\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		6.0
C_X Expander output capacitance	'H60	$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		$V_{CC} = 5.25\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		5.4
		$V_{CC} = 5.5\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		$V_{CC} = 5.25\text{ V}, V_I = 0, V_X = 0.85\text{ V}, I_X = 0$		6.0

† All typical values are at $V_{CC} = 5\text{ V}$ (except C_X), $T_A = 25^\circ\text{C}$.

recommended operating conditions

	SN64H61		SN74H61		UNIT	
	MIN	NOM	MAX	MIN		MAX
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	V
Operating free-air temperature, T_A	-55		125	0	70	$^{\circ}\text{C}$

The 'H52 is designed for use with up to six 'H61 expanders.

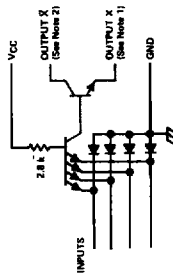
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH} High-level input voltage	17		2		0.8	V
V_{IL} Low-level input voltage	18					V
$V_X(\text{on})$ On-state expander output voltage	17	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $I_X = 4.5\text{ mA}$ for SN64H61, 5.35 mA for SN74H61, $T_A = \text{MIN}$			1	V
$I_X(\text{off})$ Off-state expander current	18	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8\text{ V}$, $V_X = 2.2\text{ V}$, $T_A = \text{MAX}$			50	μA
I_I Input current at maximum input voltage	4	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$			1	mA
I_{IH} High-level input current	4	$V_{CC} = 5.5\text{ V}$, $V_I = 2.4\text{ V}$			50	μA
I_{IL} Low-level input current	5	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-2	mA
$I_{CC}(\text{on})$ Supply current, expander on	7	$V_{CC} = 5.5\text{ V}$, $V_I = 4.5\text{ V}$			11	mA
$I_{CC}(\text{off})$ Supply current, expander off	7	$V_{CC} = 5.5\text{ V}$, $V_I = 0$			5	mA
C_X Expander output capacitance		V_{CC} and inputs open, $f = 1\text{ MHz}$			5.4	pF

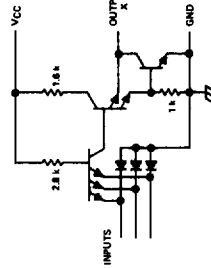
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5\text{ V}$ (except C_X). $T_A = 25^{\circ}\text{C}$.

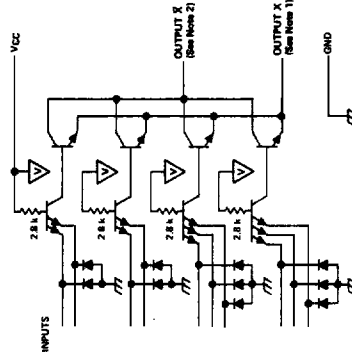
schematics (each gate)



'H60 CIRCUITS



'H61 CIRCUITS



'H62 CIRCUITS

NOTES: 1. Connect to X input of 'H60, 'H63, or 'H65 circuit.

2. Connect to X input of 'H60, 'H63, or 'H65 circuit.

Resistor values shown are nominal and in ohms.

SERIES 54/74 FLIP-FLOPS

recommended operating conditions

PARAMETER	SERIES 54/74		'70		'72, '73, '76, '107		'74		'109		'110		'111		UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM		MAX
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
High-level output current, I_{OH}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	μ A
Low-level output current, I_{OL}			-400			-400			-400			-400			-800	μ A
Pulse width, t_w	Clock high		18	20	16	30	16	20	16	20	16	20	16	20	16	ms
	Clock low		30	47	30	37	30	30	25	25	25	25	25	25	25	ms
Input setup time, t_{su}	Preset or clear low		25	30	25	30	25	30	25	30	25	30	25	30	25	ns
	Input		20†	0†	20†	0†	20†	0†	20†	0†	20†	0†	20†	0†	20†	ns
Input hold time, t_h	Input		5†	0†	5†	0†	5†	0†	5†	0†	5†	0†	5†	0†	5†	ns
	Operating free-air temperature, T_A		-55	125	-55	125	-55	125	-55	125	-55	125	-55	125	-55	125

† The arrow indicates the edge of the clock pulse used for reference; † for the rising edge, † for the falling edge.
 † electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		'70		'72, '73, '76, '107		'74		'109		'110		'111		UNIT	
	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡		MAX
V_{IH} High-level input voltage	2		0.8	0.8	2	0.8	2	0.8	2	0.8	2	0.8	2	0.8	V	
V_{IL} Low-level input voltage			-1.5	-1.5		-1.5		-1.5		-1.5		-1.5		-1.5	V	
V_{IK} Input clamp voltage															V	
V_{OH} High-level output voltage			2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V	
V_{OL} Low-level output voltage			0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		V	
I_I Input current at maximum input voltage	D, J, K, or \bar{K}		1	1	1	1	1	1	1	1	1	1	1	1	mA	
	Clear		40	40	40	40	40	40	40	40	40	40	40	40	40	μ A
I_{IH} High-level input current	Preset		80	80	80	120	160	80	80	80	80	160	80	80	80	μ A
	Clock		80	80	80	80	80	80	80	80	80	80	80	80	80	μ A
I_{IL} Low-level input current	D, J, K, or \bar{K}		-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	-1.6	mA
	Clear *		-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	mA
I_{OS} Short-circuit output current	Preset *		-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	mA
	Clock		-1.6	-1.6	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	-3.2	mA
I_{CC} Supply current (Average per flip-flop)	Series 54		-20	-57	-20	-57	-20	-57	-30	-85	-20	-57	-20	-57	-57	mA
	Series 74		-18	-57	-18	-57	-18	-57	-30	-85	-18	-57	-18	-57	-18	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ$ C.

* Clear is tested with preset high and preset is tested with clear high.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is at 4.5 V for the '70, '110, and '111; and

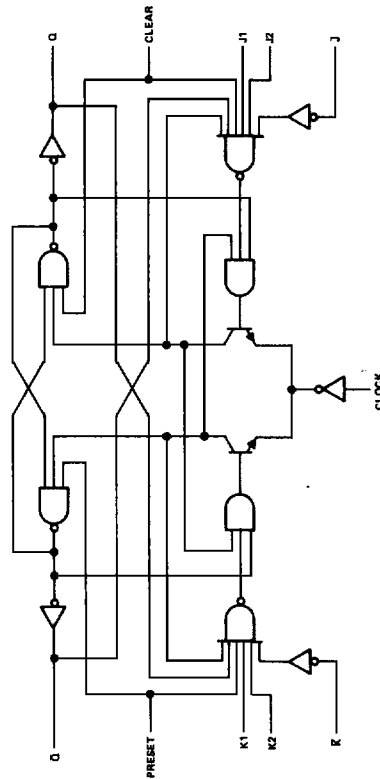
is grounded for all the others.

switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	70		72, 73 76, 107		74		109		110		111		UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f _{max}				20	35	15	20	15	25	25	25	25	25	25	25	MHz
t _{PLH}	Preset	Q	C _L = 15 pF, R _L = 400 Ω, See Note 2	50		16	25	25		10	15	12	20	12	18	ns
t _{PHL}	(as applicable)	\bar{Q}		50		25	40	40		23	35	18	25	21	30	
t _{PLH}	Clear	Q		50		16	25	25		10	15	12	20	12	18	ns
t _{PHL}	(as applicable)	\bar{Q}		50		25	40	40		17	25	18	25	21	30	
t _{PLH}	Clock	Q or \bar{Q}		27	50	16	25	14	25	10	16	20	30	12	17	ns
t _{PHL}			18	50	25	40	20	40	18	28	13	20	20	30		

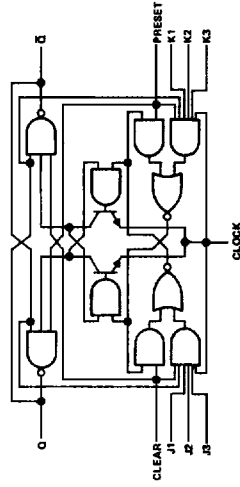
¹f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagrams



70-GATED J-K WITH CLEAR AND PRESET

See following pages for:
73-DUAL J-K WITH CLEAR
74-DUAL D WITH CLEAR AND PRESET
76-DUAL J-K WITH CLEAR AND PRESET
107-DUAL J-K WITH CLEAR

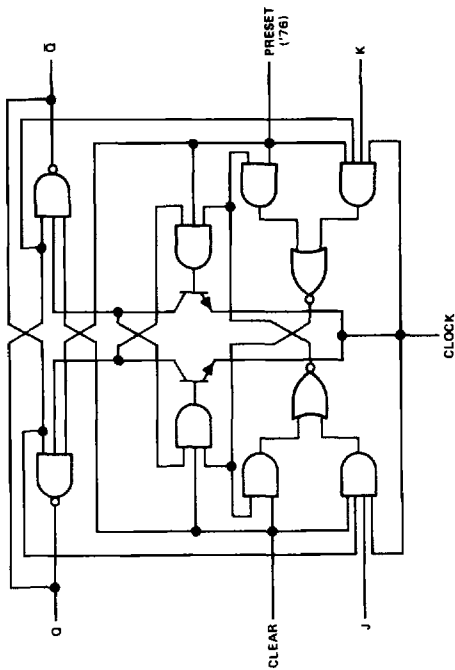


72-GATED J-K WITH CLEAR AND PRESET

109-DUAL $\bar{J}\bar{K}$ WITH CLEAR AND PRESET
110-GATED J-K WITH CLEAR AND PRESET
111-DUAL J-K WITH CLEAR AND PRESET

SERIES 54/74 FLIP-FLOPS

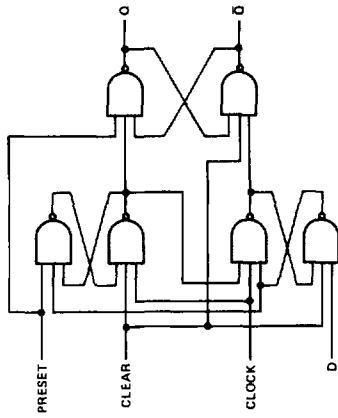
functional block diagrams (continued)



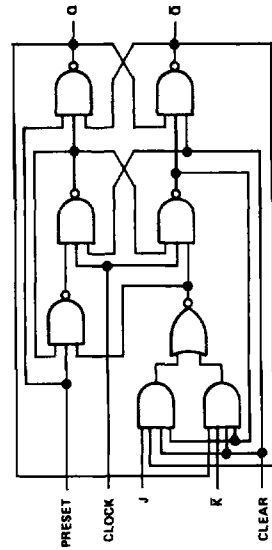
'73-DUAL J-K WITH CLEAR

'76-DUAL J-K WITH CLEAR AND PRESET

'107-DUAL J-K WITH CLEAR

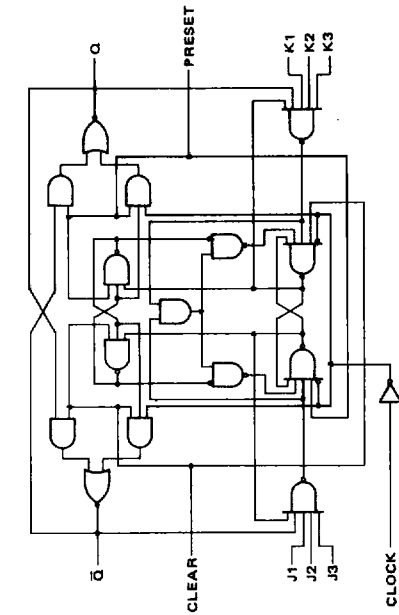


'74-DUAL D WITH CLEAR AND PRESET

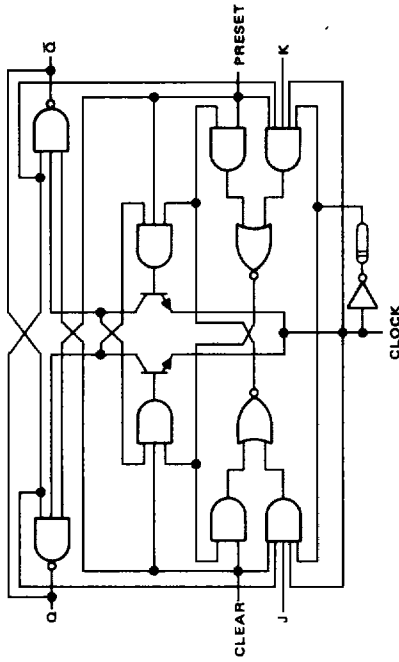


'108-DUAL J-K WITH CLEAR AND PRESET

functional block diagrams (continued)

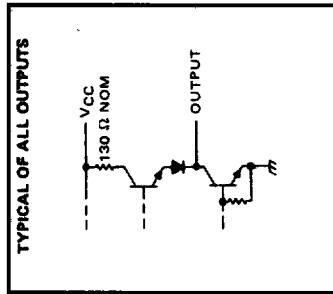
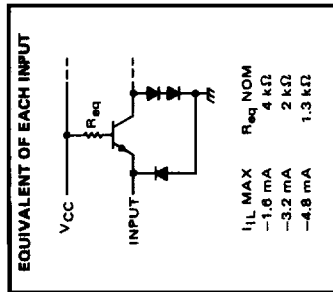


'110-GATED J-K WITH CLEAR AND PRESET



'111-DUAL J-K WITH CLEAR AND PRESET

schematics of inputs and outputs



SERIES 54H/74H PULSE-TRIGGERED J-K AND EDGE-TRIGGERED D-TYPE FLIP-FLOPS

recommended operating conditions

	SERIES 54H/74H		'H71		'H72, 'H73, 'H76		'H74		'H78		UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
High-level output current, I _{OH}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	μA
Low-level output current, I _{OL}			-500			-500			-1000			-800	μA
Pulse width, t _w			20			20			20			20	ns
Clear or preset low			28			28			13.5			28	ns
High-level data			0†			0†			10†			0†	ns
Low-level data			0†			0†			15†			0†	ns
Operating free-air temperature, T _A			-55			125			-55			125	°C

† The arrow indicates the edge of the clock pulse used for reference; † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		'H71		'H72, 'H73, 'H76		'H74		'H78		UNIT		
	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage			0.8			0.8			0.8			0.8	V
V _{IL} Low-level input voltage			-1.5			-1.5			-1.5			-1.5	V
V _{IK} Input clamp voltage													V
V _{OH} High-level output voltage			2.4			2.4			2.4			2.4	V
V _{OL} Low-level output voltage			0.2			0.2			0.2			0.2	V
I _I Input current at maximum input voltage			1			1			1			1	mA
I _{IH} High-level input current	D, J, or K		50			50			50			50	μA
	Clear					100			150			200	μA
	Preset					100			100			100	μA
I _{IL} Low-level input current	D, J, or K		-2			-2			-2			-2	μA
	Clear *					-4			-4			-4	μA
	Preset *					-6			-6			-6	μA
I _{OS} Short-circuit output current‡			-4			-2			-4			-4	mA
I _{CC} Supply current (Average per flip-flop)	V _{CC} = MAX		-40			-100			-100			-100	mA
	V _{CC} = MAX, See Note 1		19			30			15			25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

* Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

* Clear is tested with preset high and preset is tested with clear high.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

SERIES 54H/74H PULSE-TRIGGERED J-K AND EDGE-TRIGGERED D-TYPE FLIP-FLOPS

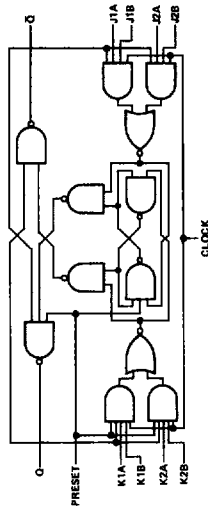
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'H71, 'H72, 'H73, 'H76, 'H78		'H74		UNIT
				MIN	TYP	MAX	MIN	
f_{max}		Q	$C_L = 25\text{ pF}$, $R_L = 280\ \Omega$, See Note 2	25	30	35	43	MHZ
t_{PLH}	Preset (as applicable)	\bar{Q}		6	13		20	ns
t_{PHL}	Clear (as applicable)	Q		12	24		30	ns
t_{PLH}	(as applicable)	Q		6	13		20	ns
t_{PHL}	Clock	Q or \bar{Q}		12	24		30	ns
t_{PHL}				14	21		8.5	15
			22	27		13	20	ns

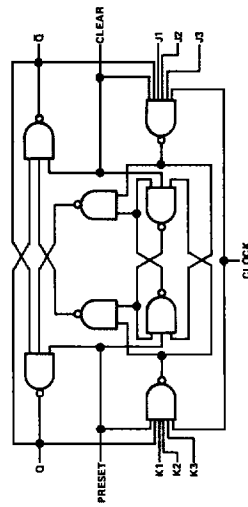
¹ t_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagrams



'H71-GATED J-K WITH PRESET



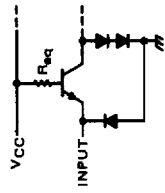
'H72-GATED J-K WITH CLEAR AND PRESET

Same functional block diagram as for '74, see page 6-48.

'H74-DUAL D WITH CLEAR AND PRESET

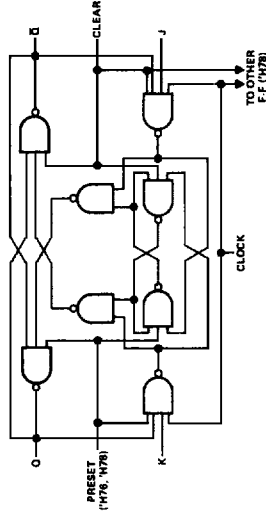
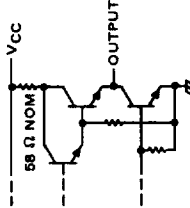
schematics of input and outputs

EQUIVALENT OF EACH INPUT



$I_{IL}\text{ MAX}$ $R_{eq}\text{ NOM}$
 -2 mA 2.8 k Ω
 -4 mA 1.4 k Ω
 -6 mA 933 Ω
 -8 mA 700 Ω

TYPICAL OF ALL OUTPUTS



'H73-DUAL J-K WITH CLEAR
 'H76-DUAL J-K WITH CLEAR AND PRESET
 'H78-DUAL J-K WITH PRESET, COMMON CLEAR,
 AND COMMON CLOCK

SERIES 54H/74H EDGE-TRIGGERED J-K FLIP-FLOPS

recommended operating conditions

	SERIES 54H/74H			'H101			'H102, 'H106			'H103			'H108			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
High-level output current, I_{OH}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	μ A
Low-level output current, I_{OL}			-500			-500			-500			-500			-500	mA
Pulse width, t_p	Clock high															
	Clock low															
	Clear or preset low															
Setup time, t_{su}	High-level data															
	Low-level data															
Hold time, t_h	0 \dagger															
Operating free-air temperature, T_A	Series 54H															
	Series 74H															

\dagger The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	'H101			'H102, 'H106			'H103			'H108			UNIT
		MIN	TYP \ddagger	MAX	MIN	TYP \ddagger	MAX	MIN	TYP \ddagger	MAX	MIN	TYP \ddagger	MAX	
V_{IH} High-level input voltage		2		0.8			0.8			0.8			0.8	V
V_{IL} Low-level input voltage				-1.5			-1.5			-1.5			-1.5	V
V_{IK} Input clamp voltage														V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, I_L = -8 \text{ mA}$ $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -600 \mu\text{A}$	2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$	0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1		1	1		1	1		1		1		mA
I_{IH} High-level input current	Any J or K			50			50			50			50	μ A
	Clear			100			100			100			100	μ A
	Preset			100			100			100			100	μ A
I_{IL} Low-level input current	Any J or K	0	-1	-2	0	-1	-2	0	-1	-2	0	-1	-2	mA
	Clear			-1			-1			-1			-1	mA
	Preset			-1			-1			-1			-1	mA
	Clock			-3			-4.8			-3			-4.8	mA
I_{OS} Short-circuit output current \S	$V_{CC} = \text{MAX}$	-40	-100	-100	-40	-100	-100	-40	-100	-100	-40	-100	-100	mA
I_{CC} Supply current (Average per flip-flop)	$V_{CC} = \text{MAX}$, See Note 1	20	38		20	38		20	38		20	38		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

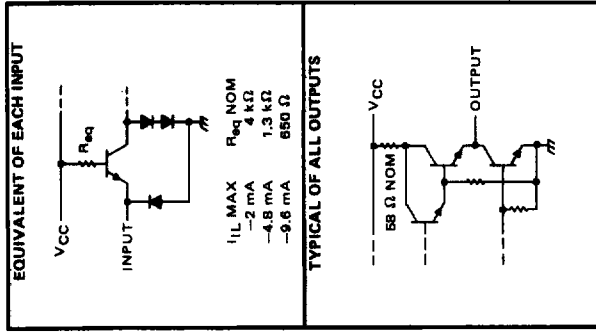
[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

[§]Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

SERIES 54H/74H EDGE-TRIGGERED J-K FLIP-FLOPS

schematics of inputs and outputs

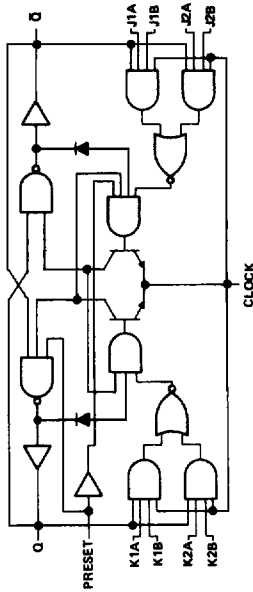


switching characteristics, $V_{CC} = 5 V$, $T_A = 25^\circ C$

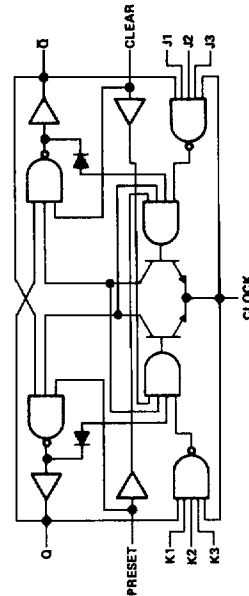
PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			UNIT
			MIN	TYP	MAX	
f_{max}			40	50		MHz
t_{PLH}	Preset or clear	Q or \bar{Q}		8	12	ns
t_{PHL}	Preset or clear (clock high)	Q or \bar{Q}		15	20	ns
t_{PLH}	Preset or clear (clock low)	Q or \bar{Q}		23	35	ns
t_{PHL}	Clock	Q or \bar{Q}		10	15	ns
t_{PHL}		Q or \bar{Q}		16	20	ns

¹ f_{max} = maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

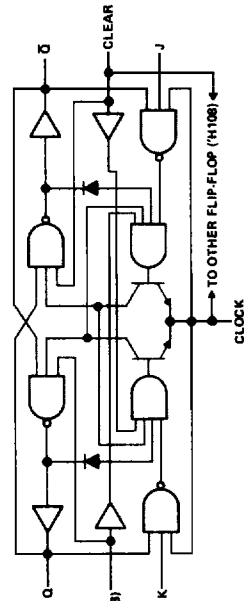
functional block diagrams



'H101—GATED J-K WITH PRESET



'H102—GATED J-K WITH CLEAR AND PRESET



'H103—DUAL J-K WITH CLEAR
 'H106—DUAL J-K WITH CLEAR AND PRESET
 'H108—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

SERIES 54L/74L FLIP-FLOPS

recommended operating conditions

	SERIES 54L/74L	'L71		'L72, 'L73		'L74		'L78		UNIT
		MIN	NOM MAX	MIN	MAX	MIN	NOM MAX	MIN	NOM MAX	
Supply voltage, V _{CC}	Series 54L	4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
	Series 74L	4.75	5.25	4.75	5.25	4.75	5.25	4.75	5.25	V
	Series 54L	-100	-100	-100	-100	-100	-100	-100	-100	μA
High-level output current, I _{OH}	Series 74L	-200	-200	-200	-200	-200	-200	-200	-200	mA
	Series 54L	2	2	2	2	2	2	2	2	mA
Low-level output current, I _{OL}	Series 74L	3.8	3.8	3.8	3.8	3.8	3.8	3.8	3.8	mA
	Series 54L	200	200	200	200	200	200	200	200	ns
Pulse width, t _w	Clock high	200	200	200	200	200	200	200	200	ns
Clear or preset low	Clock low	200	200	200	200	200	200	200	200	ns
	Clear or preset low	100	100	100	100	100	100	100	100	ns
Setup time, t _{su}		0†	0†	0†	0†	50†	50†	0†	0†	ns
Hold time, t _h		0‡	0‡	0‡	0‡	15‡	15‡	0‡	0‡	ns
Operating free-air temperature, T _A	Series 54L	-55	125	-55	125	-55	125	-55	125	°C
	Series 74L	0	70	0	70	0	70	0	70	°C

† The arrow indicates the edge of the clock pulse used for reference. ‡ for the rising edge, † for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'L71		'L72, 'L73		'L74		'L78		UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	
V _{IH} High-level input voltage	Clock input	2	2	0.6	0.6	2	2	2	2	V
	All other inputs			0.7	0.7			0.7	0.7	V
V _{OH} High-level output voltage	Series 54L	V _{CC} - MIN, V _{IH} = 2 V,		2.4	3.3	2.4	3.3	2.4	3.3	V
	Series 74L	V _{IH} = V _{IH} max, I _{OH} = MAX		2.4	3.2	2.4	3.2	2.4	3.2	V
V _{OL} Low-level output voltage	Series 54L	V _{CC} = MIN, V _{IH} = 2 V,		0.15	0.3	0.15	0.3	0.15	0.3	V
	Series 74L	V _{IH} = V _{IH} max, I _{OL} = MAX		0.2	0.4	0.2	0.4	0.2	0.4	V
I _I Input current at maximum input voltage	R, S, J, K, or D	100	100	100	100	100	100	100	100	μA
	Clear	200	200	200	200	200	200	200	200	μA
I _{IH} High-level input current	Preset	200	200	200	200	200	200	200	200	μA
	Clock	200	200	200	200	200	200	200	200	μA
I _{IL} Low-level input current	R, S, J, K, or D	10	10	10	10	10	10	10	10	μA
	Clear	20	20	20	20	20	20	20	20	μA
I _{OL} Short-circuit output current	Preset	-200	-200	-200	-200	-200	-200	-200	-200	mA
	Clock	-0.18	-0.18	-0.18	-0.18	-0.18	-0.18	-0.18	-0.18	mA
I _{CC} Supply current (Average per flip-flop)	R, S, J, K, or D	-0.36	-0.36	-0.36	-0.36	-0.36	-0.36	-0.36	-0.36	mA
	Clear	-0.36	-0.36	-0.36	-0.36	-0.36	-0.36	-0.36	-0.36	mA
I _{OS} Short-circuit output current	Preset	-0.36	-0.36	-0.36	-0.36	-0.36	-0.36	-0.36	-0.36	mA
	Clock	-3	-15	-3	-15	-3	-15	-3	-15	mA
I _{CC} Supply current (Average per flip-flop)	V _{CC} = MAX, See Note 1	0.76	1.44	0.76	1.44	0.8	1.5	0.76	1.44	mA
	V _{CC} = MAX	0.76	1.44	0.76	1.44	0.8	1.5	0.76	1.44	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

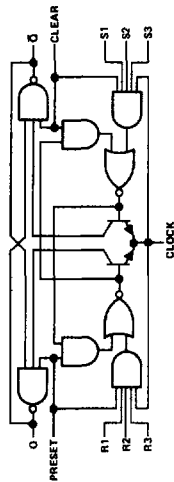
NOTE 1: With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

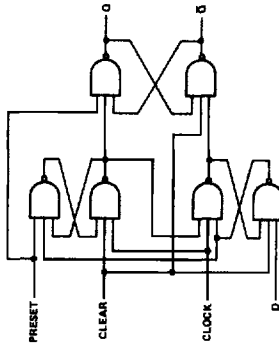
PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'L71, 'L72, 'L73, 'L78		'L74		UNIT
				MIN	TYP	MAX	MIN	
f_{max}	Preset or clear	Q or \bar{Q}	$C_L = 50\text{ pF}$, $R_L = 4\text{ k}\Omega$, See Note 2	2.5	3	2.5	3	MHz
t_{PLH}	Preset or clear (clock high)	\bar{Q} or Q		35	75	50	75	ns
t_{PHL}	Preset or clear (clock low)	Q or \bar{Q}		60	150	80	150	ns.
t_{PLH}	Clock	Q or \bar{Q}	10	35	75	15	65	100
t_{PHL}			10	60	150	15	85	

¹ f_{max} = maximum clock frequency
² t_{PLH} = propagation delay time, low-to-high-level output
³ t_{PHL} = propagation delay time, high-to-low-level output
 NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

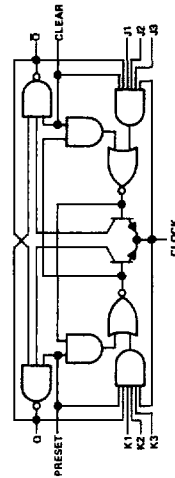
functional block diagrams



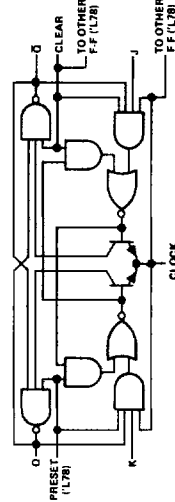
'L71—GATED R-S WITH CLEAR AND PRESET



'L74—DUAL D WITH CLEAR AND PRESET

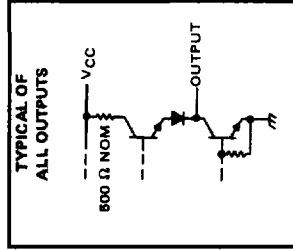
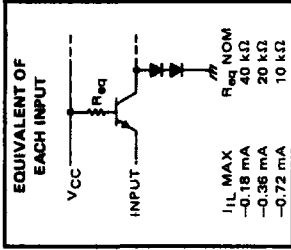


'L72—GATED J-K WITH CLEAR AND PRESET



'L73—DUAL J-K WITH CLEAR
 'L78—DUAL J-K WITH PRESET, COMMON CLEAR,
 AND COMMON CLOCK

schematics of inputs and outputs



SERIES 54LS/74LS FLIP-FLOPS

recommended operating conditions

PARAMETER	SERIES 54LS/74LS		'L574A, 'L574A, 'L574A		'L574A, 'L574A, 'L574A		'L574A, 'L574A, 'L574A		'L574A, 'L574A, 'L574A		UNIT	
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN		TYP
Supply voltage, V_{CC}	4.5	5	6.5	4.5	5	6.5	4.5	5	6.5	4.5	5	6.5
High-level output current, I_{OH}	4.75	5	6.25	4.75	5	6.25	4.75	5	6.25	4.75	5	6.25
Low-level output current, I_{OL}	-400			-400			-400			-400		
Low-level output current, I_{L}	4			4			4			4		
Low-level output current, I_{L}	8			8			8			8		
Low-level output current, I_{L}	25			25			25			25		
Low-level output current, I_{L}	30			30			30			30		
Low-level output current, I_{L}	20			20			20			20		
Low-level output current, I_{L}	20			20			20			20		
Low-level output current, I_{L}	20			20			20			20		
Low-level output current, I_{L}	0.1			0.1			0.1			0.1		
Operating free-air temperature, T_A	-55	125	85	-55	125	85	-55	125	85	-55	125	85
Operating free-air temperature, T_A	0	70	0	70	0	70	0	70	0	70	0	70

† The arrow indicates the edge of the clock pulse used for reference; † for the rising edge, † for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		'L574A		'L574A, 'L574A, 'L574A		'L574A, 'L574A, 'L574A		'L574A, 'L574A, 'L574A		UNIT	
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN		TYP
V_{IH} High-level input voltage	2			2			2			2		
Low-level input voltage	0.7			0.7			0.7			0.7		
Input voltage	0.8			0.8			0.8			0.8		
Input clamp voltage	-1.5			-1.5			-1.5			-1.5		
High-level output voltage	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4	
Low-level output voltage	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4	
Low-level output voltage	0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4	
Low-level output voltage	0.35	0.5		0.35	0.5		0.35	0.5		0.35	0.5	
Low-level output voltage	0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4	
Input current at maximum input voltage	0.1			0.1			0.1			0.1		
Input current at maximum input voltage	0.3			0.3			0.3			0.3		
Input current at maximum input voltage	0.3			0.3			0.3			0.3		
Input current at maximum input voltage	0.4			0.4			0.4			0.4		
High-level input current	20			20			20			20		
High-level input current	40			40			40			40		
High-level input current	60			60			60			60		
High-level input current	80			80			80			80		
Low-level input current	-0.4			-0.4			-0.4			-0.4		
Low-level input current	-0.8			-0.8			-0.8			-0.8		
Low-level input current	-0.8			-0.8			-0.8			-0.8		
Low-level input current	-0.8			-0.8			-0.8			-0.8		
Short-circuit output current	-20			-20			-20			-20		
Short-circuit output current	-20			-20			-20			-20		
Supply current	4	6		4	6		4	6		4	6	
Supply current	4	6		4	6		4	6		4	6	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ$ C.

§ Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

SERIES 54LS/74LS FLIP-FLOPS

switching characteristics, $V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS73A, 'LS76A, 'LS78A, 'LS107A, 'LS112A, 'LS113A, 'LS114A		'LS74A, 'LS109A		UNIT
				MIN	TYP	MAX	MIN	
f_{max}			$C_L = 15\text{ pF}$ $R_L = 2\text{ k}\Omega$, See Note 2	30	45	25	33	MHZ
t_{PLH}		0 or Q		15	20	13	26	ns
t_{PHL}		0 or Q		15	20	26	40	ns

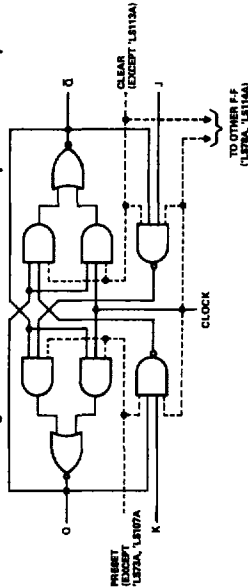
¹ f_{max} = maximum clock frequency

² t_{PLH} = propagation delay time, low-to-high-level output

³ t_{PHL} = propagation delay time, high-to-low-level output

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

functional block diagrams and schematics of inputs and outputs



'LS73A, 'LS107A—DUAL J-K WITH CLEAR

'LS78A, 'LS112A—DUAL J-K WITH CLEAR AND PRESET

'LS78A, 'LS114A—DUAL J-K WITH PRESET, COMMON CLEAR,

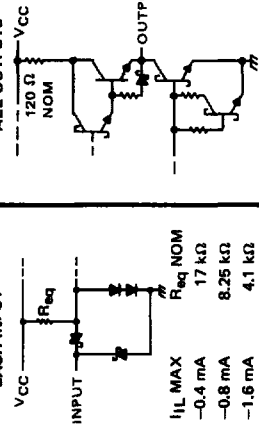
AND COMMON CLOCK

'LS113A—DUAL J-K WITH PRESET

'LS73A, 'LS76A, 'LS78A, 'LS112A, 'LS113A, 'LS114A

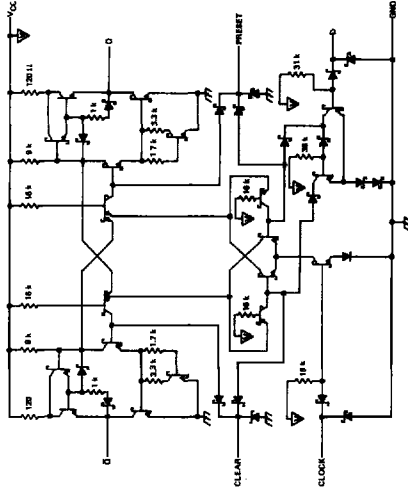
EQUIVALENT OF EACH INPUT

TYPICAL OF ALL OUTPUTS

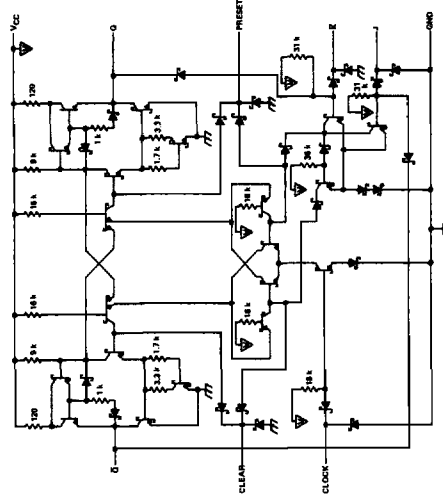


$I_{IL}\text{ MAX}$	$R_{eq}\text{ NOM}$
-0.4 mA	17 k Ω
-0.8 mA	8.25 k Ω
-1.6 mA	4.1 k Ω

schematics of 'LS74A and 'LS109A



'LS74A—DUAL D WITH CLEAR AND PRESET



'LS109A—DUAL J-K WITH CLEAR AND PRESET

SERIES 54S/74S FLIP-FLOPS

recommended operating conditions

	SERIES 54S/74S		'S74		'S112		'S113		'S114		UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN		NOM
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5
High-level output current, I_{OH}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25
Low-level output current, I_{OL}			-1			-1			-1			-1
			20			20			20			20
Pulse width, t_w			6			6			6			6
			7.3			6.5			6.5			6.5
Clear or preset low			7			8			8			8
High-level data			31			31			31			31
Low-level data			31			31			31			31
Input hold time, t_H			21			0.1			0.1			0.1
Operating free-air temperature, T_A	-55		125	-55		125	-55		125	-55		125
			0			70			70			70

† The arrow indicates the edge of the clock pulse used for reference; † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'S74		'S112		'S113		'S114		UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	
V_{IH} High-level input voltage		2		2		2		2		V
V_{IL} Low-level input voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		0.8		0.8		0.8		0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$		-1.2		-1.2		-1.2		-1.2	V
V_{OH} High-level output voltage	Series 54S	2.5	3.4	2.5	3.4	2.5	3.4	2.5	3.4	V
	Series 74S	2.7	3.4	2.7	3.4	2.7	3.4	2.7	3.4	V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$		0.5		0.5		0.5		0.5	V
	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		1		1		1	mA
I_I Input current at maximum input voltage	J, K, or D		50		50		50		50	mA
	Clear		150		100		100		200	µA
	Preset		100		100		100		100	µA
	Clock		100		100		100		200	µA
I_{IH} High-level input current	J, K, or D		-2		-1.6		-1.6		-1.6	mA
	Clear *		-6		-7		-7		-14	mA
	Preset *		-4		-4		-4		-4	mA
I_{IL} Low-level input current	Clock		-4		-4		-4		-4	mA
			-4		-4		-4		-4	mA
I_{OS} Short-circuit output current‡	$V_{CC} = \text{MAX}$	-40	-100	-40	-100	-40	-100	-40	-100	mA
I_{CC} Supply current (average per flip-flop)	$V_{CC} = \text{MAX}$, See Note 1	15	25	15	25	15	25	15	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

* Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

† Clear is tested with preset high and preset is tested with clear high.

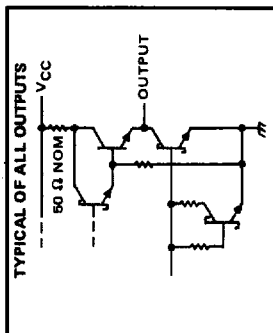
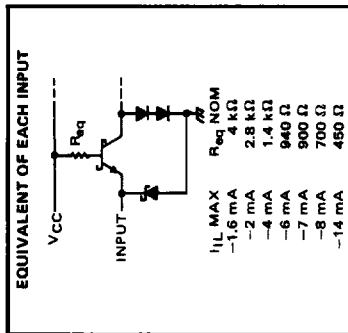
NOTE 1: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

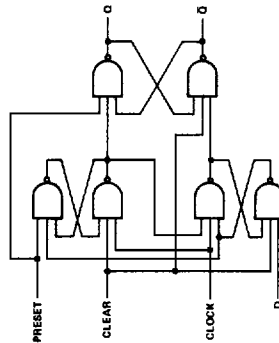
PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'S74		'S112, 'S113, 'S114		UNIT
			MIN	MAX	TYP	MAX	MIN	TYP	
f_{max}			75	110	4	6	80	125	MHz
t_{PLH}	Preset or clear	Q or \bar{Q}			9	13.5			ns
t_{PHL}	Preset or clear (clock high)	\bar{Q} or Q			5	8			ns
t_{PLH}	Preset or clear (clock low)	Q or \bar{Q}			6	9			ns
t_{PHL}	Clock	Q or \bar{Q}			6	9			ns

¹ f_{max} = maximum clock frequency
² t_{PLH} = propagation delay time, low-to-high-level output
³ t_{PHL} = propagation delay time, high-to-low-level output
 NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

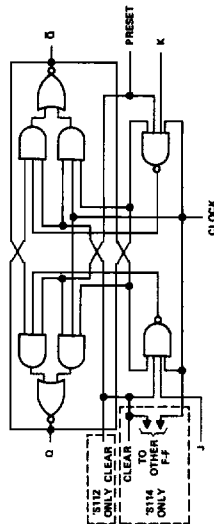
schematics of inputs and outputs



functional block diagrams



'S74-DUAL D WITH CLEAR AND PRESET



'S112-DUAL J-K WITH CLEAR AND PRESET

'S113-DUAL J-K WITH PRESET

'S114-DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

54LS LATCHES

recommended operating conditions

PARAMETER	54 FAMILY		SN64279		SN54LS279		SN74LS279		UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.5	5	5.5	4.5	5.5	V
High-level output current, I _{OH}	4.75	5	5.25	4.5	5	5.25	-800	-400	μA
Low-level output current, I _{OL}							16	4	mA
Operating free-air temperature, T _A	-55	125	-65	0	70	0	70	70	°C

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN64279		SN54LS279		SN74LS279		UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level output voltage		2		0.8	2		0.7	V
V _{IL} Low-level output voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MAX, I _I = §			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4	3.4	2.5	3.4			V
V _{OL} Low-level output voltage	V _{CC} = MIN, I _{OL} = MAX	0.2	0.4	0.25	0.4			V
	V _{IL} = V _{IL} max, V _{IH} = 2 V, I _{OL} = 4 mA	0.2	0.4	0.35	0.4			V
I _I Input current at maximum input voltage	V _{CC} = MAX			1				mA
I _{IH} High-level input current	V _I = 2.4 V			40				μA
	V _I = 2.7 V					20		μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-1.8				mA
	V _{CC} = MAX	-18	-55	-20	-100			mA
I _{CS} Short-circuit output current*		-18	-57	-20	-100			mA
I _{CC} Supply current	V _{CC} = MAX, See note 1	18	30	3.8	7			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN64/SN74 and -18 mA for SN54LS/SN74LS.

* Not more than one output should be shorted at a time, and for SN64LS/SN74LS, duration of the output short circuit should not exceed one second.

NOTE 1: I_{CC} is measured with all I_I inputs grounded, all S inputs at 4.5 V, and all outputs open.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{ C}$

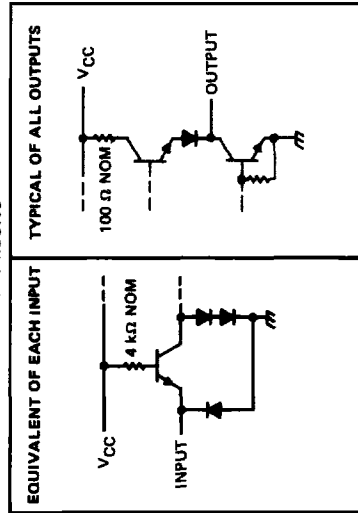
PARAMETER	TEST CONDITIONS		'LS279		UNIT
	MIN	MAX	MIN	MAX	
t_{pLH} Propagation delay time, low-to-high-level output from S input	12	22	12	22	ns
t_{pHL} Propagation delay time, high-to-low-level output from S input	9	15	13	21	
t_{pHL} Propagation delay time, high-to-low-level output from R input	15	27	15	27	

$C_L = 15\text{ pF}$,
See Notes 2 and 3

NOTE 2: Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.
NOTE 3: $R_L = 400\ \Omega$ for '279, $R_L = 2\text{ k}\Omega$ for 'LS279.

schematics of inputs and outputs

'279 CIRCUITS



'LS279 CIRCUITS

