8-Bit Bus Front-Loading-Latch Transceivers

SN54/74LS646
SN54/74LS648

SN54/74LS647
SN54/74LS649

Features/Benefits

- **Bidirectional bus transceivers and registers**
- **Independent registers for A and B buses**
- **Real-time data transfer or stored data transfer**
- **24-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Three-state or open-collector outputs drive bus lines**

Description

The 8-bit bus transceivers with 3-state ('LS646, 'LS648) or open-collector ('LS647, 'LS649) outputs have 16 D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS646/647 and 'LS648/649 are given in their respective Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path or "feed-through" into a two-way mux, is sometimes called a "front-loading latch."

A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by enable line $\overline{E}$, and direction line DIR.

When $\overline{E}$ is High data from the buses can be stored into register A and B. When $\overline{E}$ is Low and DIR is High, the direction of operation is from A to B; when $\overline{E}$ and DIR are LOW, the direction of operation is from B to A.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	O/P	PWR
SN54LS646	JS,W,L (28)	Mil	Noninvert	Three-state	LS
SN54LS646	NS,JS NL (28)	Com	Noninvert	Three-state	LS
SN54LS647	JS,W,L (28)	Mil	Noninvert	Open-collector	LS
SN74LS647	NS,JS NL (28)	Com	Noninvert	Open-collector	LS
SN54LS648	JS,W,L (28)	Mil	Invert	Three-state	LS
SN54LS648	NS,JS NL (28)	Com	Invert	Three-state	LS
SN54LS649	JS,W,L (28)	Mil	Invert	Open-collector	LS
SN74LS649	NS,JS NL (28)	Com	Invert	Open-collector	LS

Pin Configurations

'LS646/647/648/649
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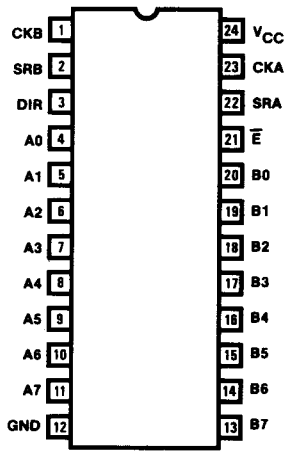

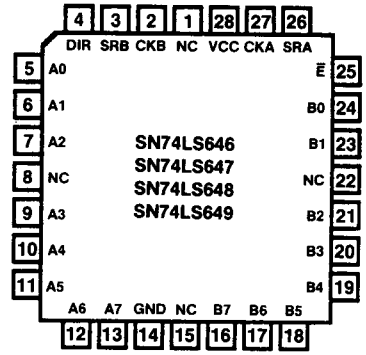

Plastic Chip Carrier

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