

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCX162373FT

Low-Voltage 16-Bit D-Type Latch with 3.6-V Tolerant Inputs and Outputs

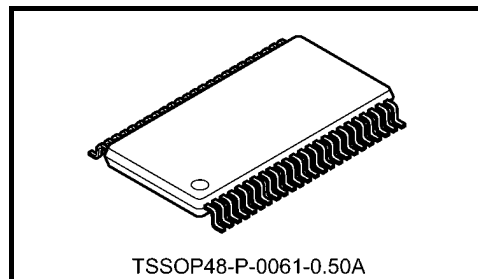
The TC74VCX162373FT is a high-performance CMOS 16-bit D-type latch. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to 3.6 V.

This 16-bit D-type latch is controlled by a latch enable input (LE) and an output enable input (\overline{OE}) which are common to each byte. It can be used as two 8-bit latches or one 16-bit latch. When the \overline{OE} input is high, the outputs are in a high-impedance state.

The 26- Ω series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge.



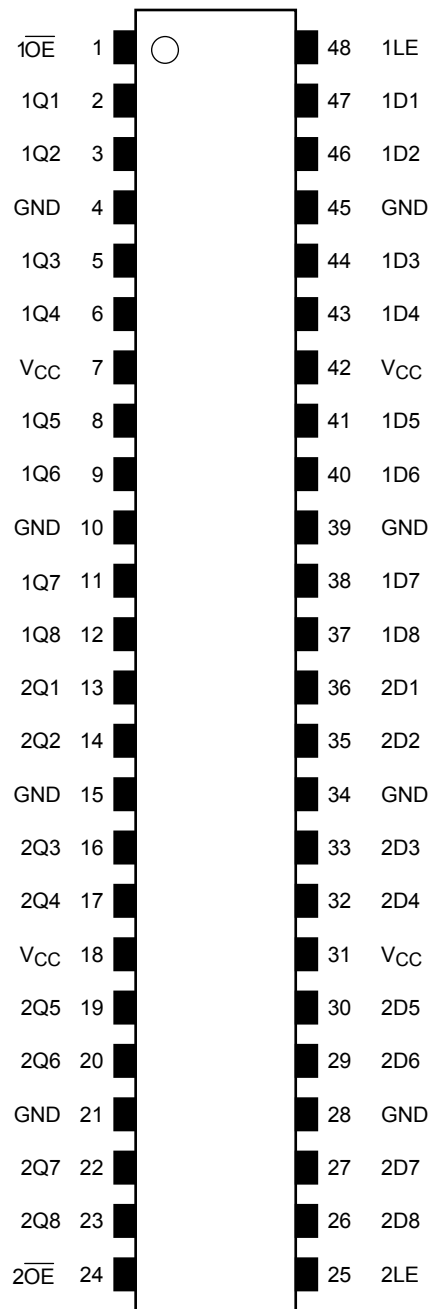
Weight: 0.25 g (typ.)

Features

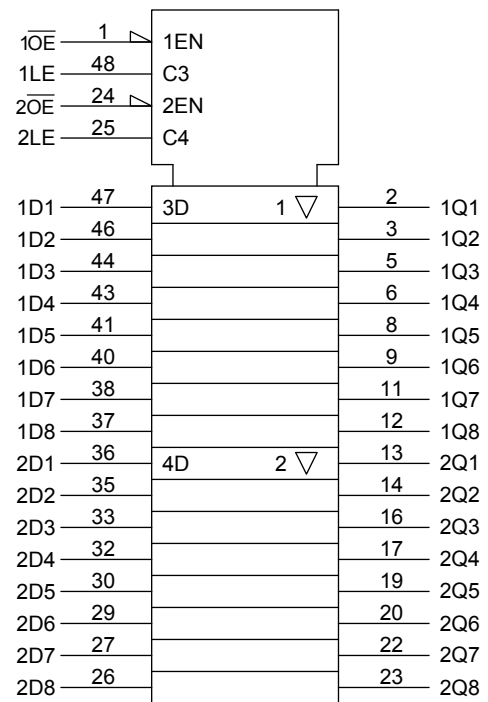
- 26- Ω series resistors on outputs
- Low-voltage operation: $V_{CC} = 1.8$ to 3.6 V
- High-speed operation: $t_{pd} = 3.3$ ns (max) ($V_{CC} = 3.0$ to 3.6 V)
: $t_{pd} = 4.5$ ns (max) ($V_{CC} = 2.3$ to 2.7 V)
: $t_{pd} = 5.8$ ns (max) ($V_{CC} = 1.8$ V)
- Output current: $I_{OH}/I_{OL} = \pm 12$ mA (min) ($V_{CC} = 3.0$ V)
: $I_{OH}/I_{OL} = \pm 8$ mA (min) ($V_{CC} = 2.3$ V)
: $I_{OH}/I_{OL} = \pm 4$ mA (min) ($V_{CC} = 1.8$ V)
- Latch-up performance: -300 mA
- ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- Package: TSSOP
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs

Start of commercial production
1997-03

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs			Outputs
$\overline{1OE}$	1LE	1D1-1D8	1Q1-1Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

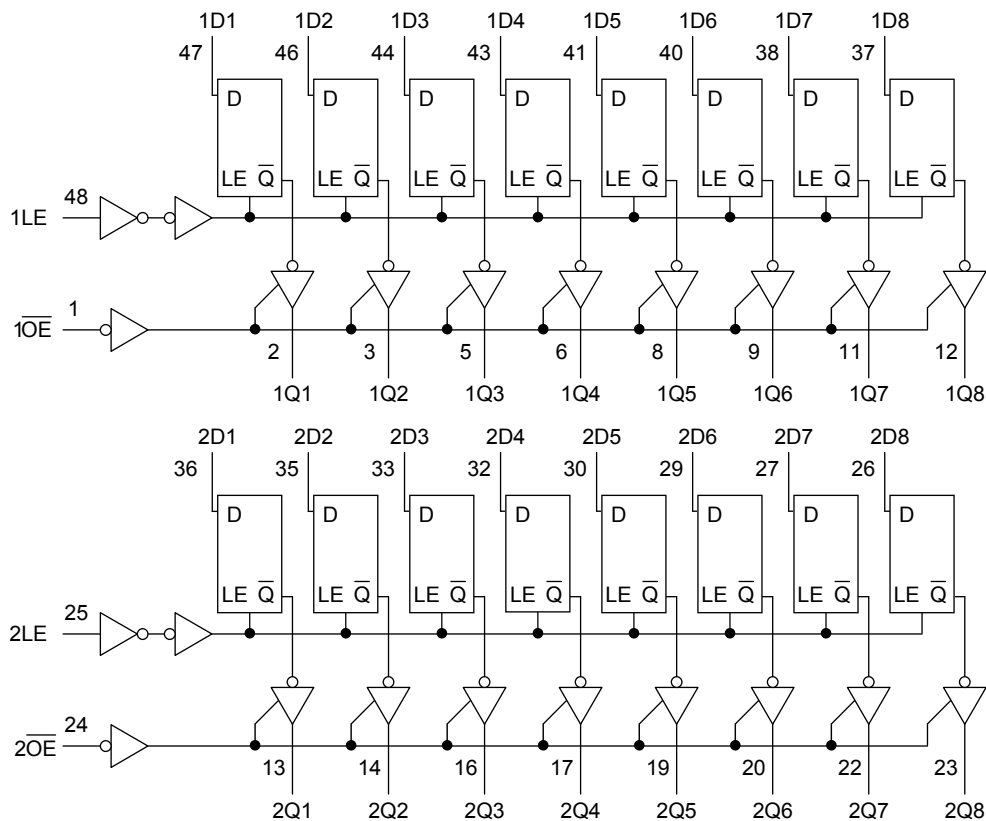
Inputs			Outputs
$\overline{2OE}$	2LE	2D1-2D8	2Q1-2Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5 to 4.6	V
DC input voltage	V_{IN}	-0.5 to 4.6	V
DC output voltage	V_{OUT}	-0.5 to 4.6 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	I_{IK}	-50	mA
Output diode current	I_{OK}	± 50 (Note 4)	mA
DC output current	I_{OUT}	± 50	mA
Power dissipation	P_D	400	mW
DC V_{CC} /ground current per supply pin	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.8 to 3.6	V
		1.2 to 3.6 (Note 2)	
Input voltage	V_{IN}	-0.3 to 3.6	V
Output voltage	V_{OUT}	0 to 3.6 (Note 3)	V
		0 to V_{CC} (Note 4)	
Output current	I_{OH}/I_{OL}	± 12 (Note 5)	mA
		± 8 (Note 6)	
		± 4 (Note 7)	
Operating temperature	T_{opr}	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dv	0 to 10 (Note 8)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: Data retention only

Note 3: OFF state

Note 4: High or low state

Note 5: $V_{CC} = 3.0$ to 3.6 V

Note 6: $V_{CC} = 2.3$ to 2.7 V

Note 7: $V_{CC} = 1.8$ V

Note 8: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} = 3.0$ V

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C, 2.7 V < VCC ≤ 3.6 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V _{IL}	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.7 to 3.6	V _{CC} - 0.2	—	V
				I _{OH} = -6 mA	2.7	2.2	—	
				I _{OH} = -8 mA	3.0	2.4	—	
				I _{OH} = -12 mA	3.0	2.2	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.7 to 3.6	—	0.2	
				I _{OL} = 6 mA	2.7	—	0.4	
				I _{OL} = 8 mA	3.0	—	0.55	
				I _{OL} = 12 mA	3.0	—	0.8	
Input leakage current		I _{IN}	V _{IN} = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V		2.7 to 3.6	—	±10.0	μA
Power-off leakage current		I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		2.7 to 3.6	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		2.7 to 3.6	—	±20.0	
Increase in I _{CC} per input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V		2.7 to 3.6	—	750	

DC Characteristics (Ta = -40 to 85°C, 2.3 V ≤ VCC ≤ 2.7 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	—		2.3 to 2.7	1.6	—	V
	L-level	V _{IL}	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.3 to 2.7	V _{CC} - 0.2	—	V
				I _{OH} = -4 mA	2.3	2.0	—	
				I _{OH} = -6 mA	2.3	1.8	—	
				I _{OH} = -8 mA	2.3	1.7	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.3 to 2.7	—	0.2	
				I _{OL} = 6 mA	2.3	—	0.4	
				I _{OL} = 8 mA	2.3	—	0.6	
Input leakage current		I _{IN}	V _{IN} = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V		2.3 to 2.7	—	±10.0	μA
Power-off leakage current		I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		2.3 to 2.7	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		2.3 to 2.7	—	±20.0	

DC Characteristics (Ta = -40 to 85°C, 1.8 V ≤ VCC < 2.3 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	—		1.8 to 2.3	0.7 × V _{CC}	—	V
	L-level	V _{IL}	—		1.8 to 2.3	—	0.2 × V _{CC}	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	1.8	V _{CC} - 0.2	—	V
				I _{OH} = -4 mA	1.8	1.4	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.8	—	0.2	
				I _{OL} = 4 mA	1.8	—	0.3	
Input leakage current		I _{IN}	V _{IN} = 0 to 3.6 V		1.8	—	±5.0	μA
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 3.6 V		1.8	—	±10.0	μA
Power-off leakage current		I _{OFF}	V _{IN} , V _{OUT} = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		1.8	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		1.8	—	±20.0	

AC Characteristics (Ta = -40 to 85°C, input: tr = tf = 2.0 ns, CL = 30 pF, RL = 500 Ω) (Note 1)

Characteristics	Symbol	Test Condition	VCC (V)	Min	Max	Unit
Propagation delay time (D-Q)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.8	1.5	5.8	ns
			2.5 ± 0.2	1.0	4.5	
			3.3 ± 0.3	0.8	3.3	
Propagation delay time (LE-Q)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.8	1.5	6.2	ns
			2.5 ± 0.2	1.0	4.9	
			3.3 ± 0.3	0.8	3.6	
3-state output enable time	t _{pZL} t _{pZH}	Figure 1, Figure 3	1.8	1.5	7.6	ns
			2.5 ± 0.2	1.0	5.4	
			3.3 ± 0.3	0.8	3.9	
3-state output disable time	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	1.8	1.5	5.3	ns
			2.5 ± 0.2	1.0	4.4	
			3.3 ± 0.3	0.8	4.0	
Minimum pulse width (LE)	t _w (H)	Figure 1, Figure 2	1.8	3.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum setup time	t _s	Figure 1, Figure 2	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time	t _h	Figure 1, Figure 2	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to output skew	t _{osLH} t _{osHL}	(Note 2)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 2: Parameter guaranteed by design.

(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)

Dynamic Switching Characteristics (Ta = 25°C, input: tr = tf = 2.0 ns, CL = 30 pF)

Characteristics	Symbol	Test Condition	VCC (V)	Typ.	Unit
Quiet output maximum dynamic VOL	VOLP	VIH = 1.8 V, VIL = 0 V (Note)	1.8	0.15	V
		VIH = 2.5 V, VIL = 0 V (Note)	2.5	0.25	
		VIH = 3.3 V, VIL = 0 V (Note)	3.3	0.35	
Quiet output minimum dynamic VOL	VOLV	VIH = 1.8 V, VIL = 0 V (Note)	1.8	-0.15	V
		VIH = 2.5 V, VIL = 0 V (Note)	2.5	-0.25	
		VIH = 3.3 V, VIL = 0 V (Note)	3.3	-0.35	
Quiet output minimum dynamic VOH	VOHV	VIH = 1.8 V, VIL = 0 V (Note)	1.8	1.55	V
		VIH = 2.5 V, VIL = 0 V (Note)	2.5	2.05	
		VIH = 3.3 V, VIL = 0 V (Note)	3.3	2.65	

Note: Parameter guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	VCC (V)	Typ.	Unit
Input capacitance	CIN	—	1.8, 2.5, 3.3	6	pF
Output capacitance	CO	—	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	CPD	fIN = 10 MHz (Note)	1.8, 2.5, 3.3	20	pF

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$$

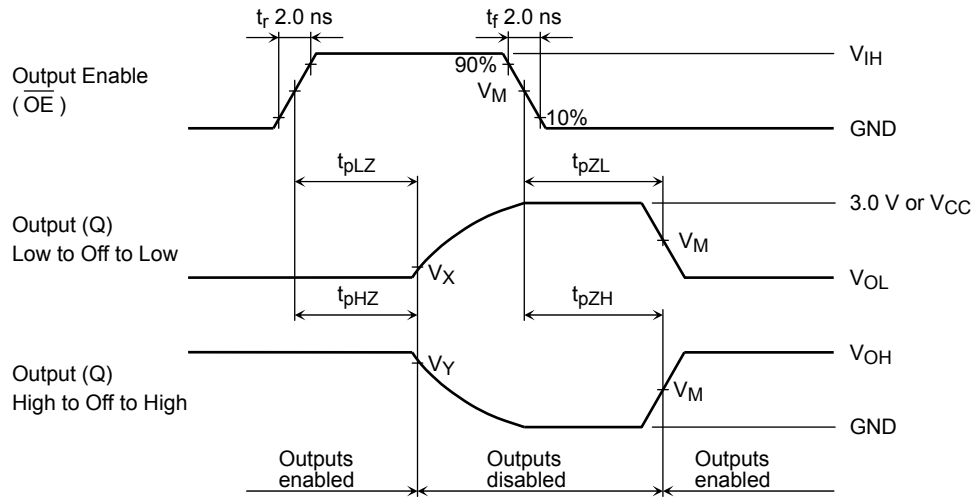


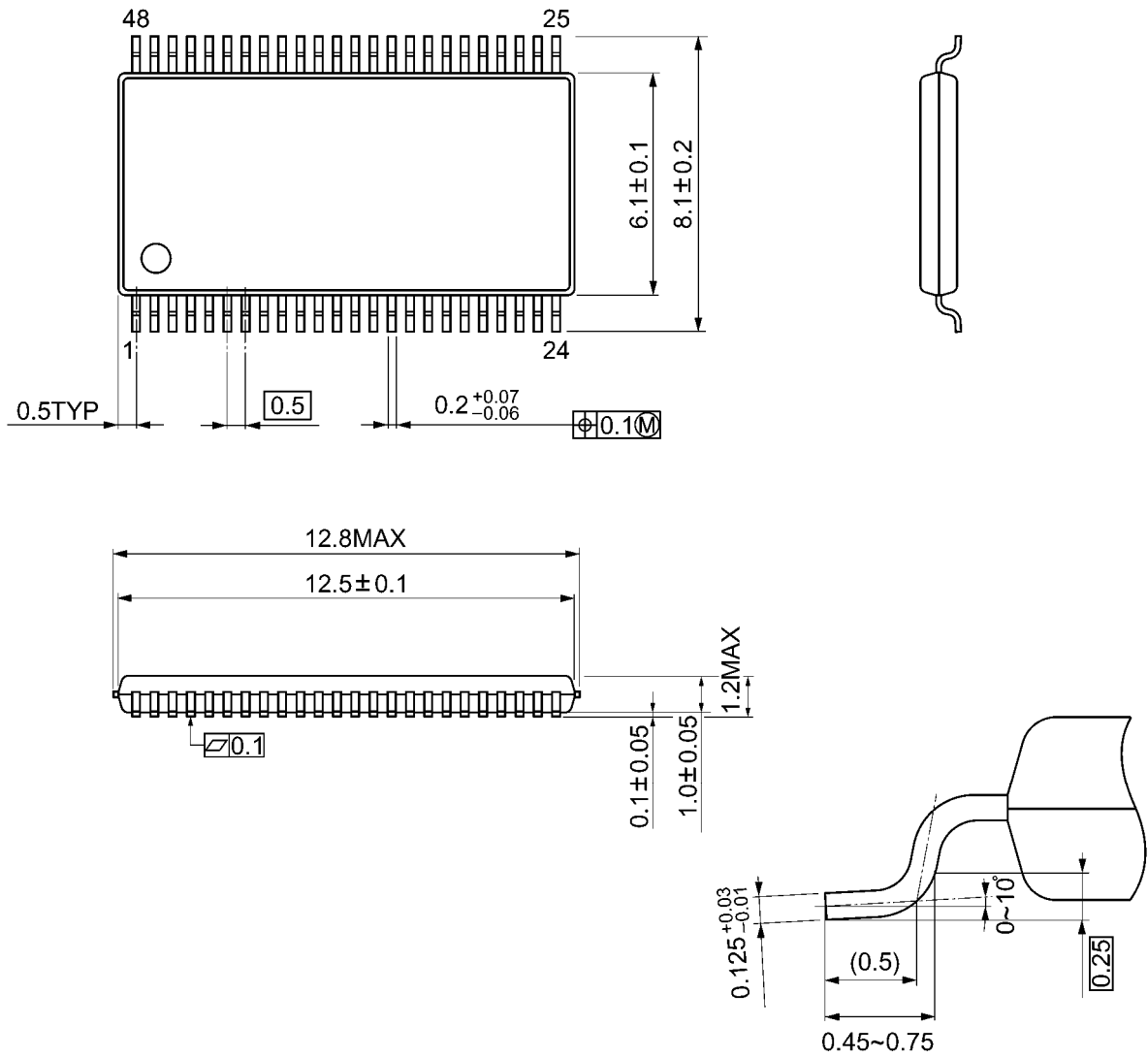
Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3$ V	$V_{OL} + 0.15$ V	$V_{OL} + 0.15$ V
V_Y	$V_{OH} - 0.3$ V	$V_{OH} - 0.15$ V	$V_{OH} - 0.15$ V

Package Dimensions

TSSOP48-P-0061-0.50A

Unit: mm



Weight: 0.25 g (typ.)

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