MOTOROLA

MC14023B
MC14023UB

CMOS SSI
(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NAND" GATE

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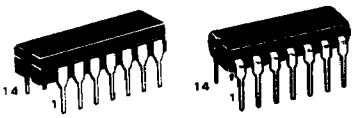
The MC14023B and MC14023UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14023B only)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14023B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4023B and CD4023UB.



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL or UBAL (Ceramic Package Only)

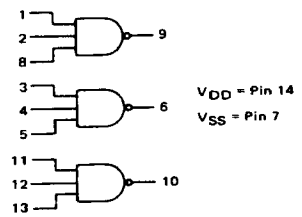
C Series: −40°C to +85°C
MC14XXXBCP or UBCP (Plastic Package)
MC14XXXBCL or UBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

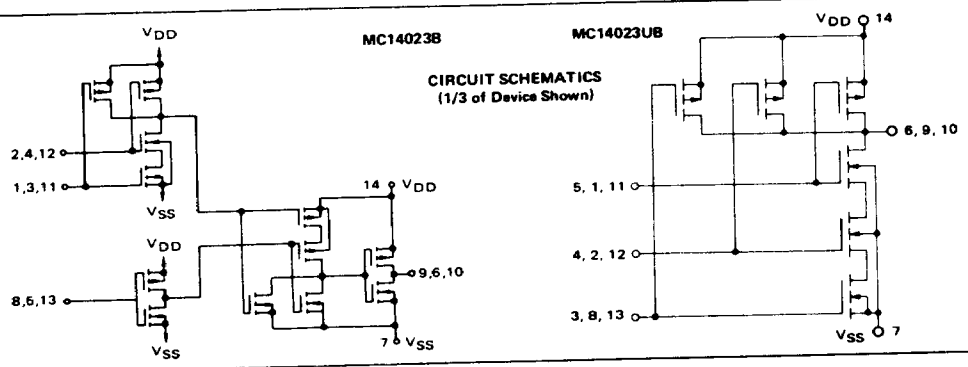
LOGIC DIAGRAM



See the MC14001B data sheet for complete characteristics of the B-Series device.

See the MC14001UB data sheet for complete characteristics for the UB device.

CIRCUIT SCHEMATICS
(1/3 of Device Shown)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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