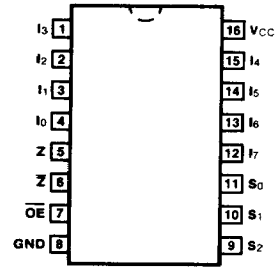
54S/74S251 010647
54LS/74LS251 610646
8-INPUT MULTIPLEXER
(With 3-State Outputs)

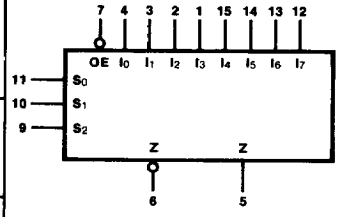
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '251 is a high speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- **MULTIFUNCTIONAL CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **INVERTING AND NON-INVERTING 3-STATE OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND 4 Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S251PC, 74LS251PC		9B
Ceramic DIP (D)	A	74S251DC, 74LS251DC	54S251DM, 54LS251DM	6B
Flatpak (F)	A	74S251FC, 74LS251FC	54S251FM, 54LS251FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. defintions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{S_0} - S_2$	Select Inputs	1.25/1.25	0.5/0.25
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)	1.25/1.25	0.5/0.25
$I_0 - I_7$	Multiplexer Input	1.25/1.25	0.5/0.25
Z	Multiplexer Output	162/12.5 (50)	65/5.0 (25)/(2.5)
$\overline{Z}$	Complementary Multiplexer Output	162/12.5 (50)	65/5.0 (25)/(2.5)

FUNCTIONAL DESCRIPTION — This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

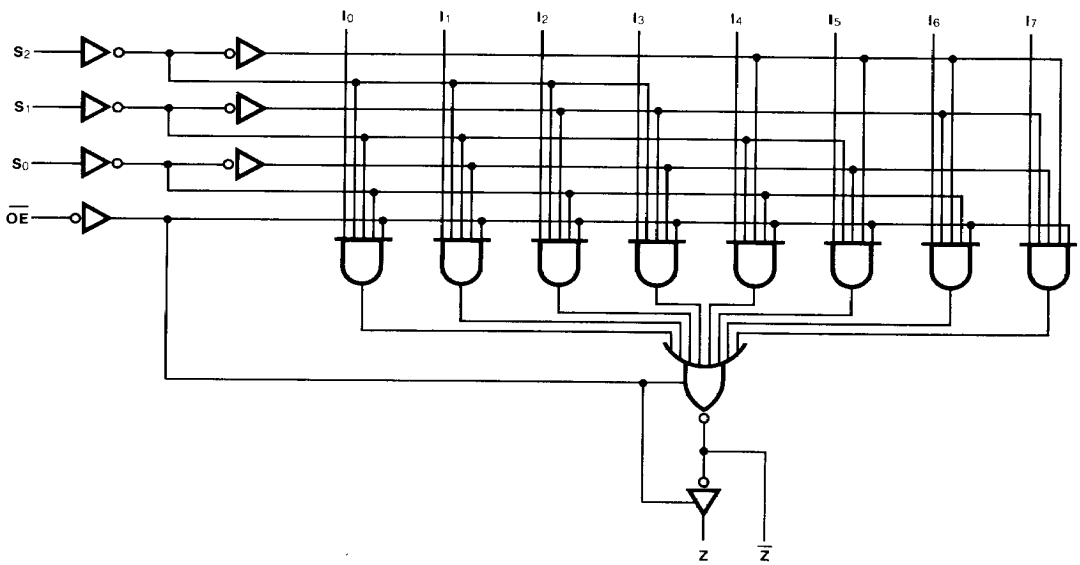
When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I_0}$	I_0
L	L	L	H	$\overline{I_1}$	I_1
L	L	H	L	$\overline{I_2}$	I_2
L	L	H	H	$\overline{I_3}$	I_3
L	H	L	L	$\overline{I_4}$	I_4
L	H	L	H	$\overline{I_5}$	I_5
L	H	H	L	$\overline{I_6}$	I_6
L	H	H	H	$\overline{I_7}$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current		-40	-100	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current	Outputs ON				10	mA	V_{CC} = Max; I_n, S_n = 4.5 V; $\overline{OE}$ = Gnd
		Outputs OFF		85		12		V_{CC} = Max; $\overline{OE}$, I_n = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$		15 13.5		23 33	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay S_n to Z		18 19.5		45 30	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_n to Z		12 12		28 26	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$		7.0 7.0		15 15	ns	Figs. 3-1, 3-4
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$		19.5 21		20 25	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS251)
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$		8.5 14		25 20	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS251) C_L = 5 pF