Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL D REGISTER (3-STATE)

ADVANCE INFORMATION
IDT54/74FBT374
IDT54/74FBT374A
IDT54/74FBT374C

FEATURES:

- IDT54/74FBT374 equivalent to the 54/74BCT374
- **IDT54/74FBT374A 25% faster than the 374**
- **IDT54/74FBT374C 10% faster than the 374A**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

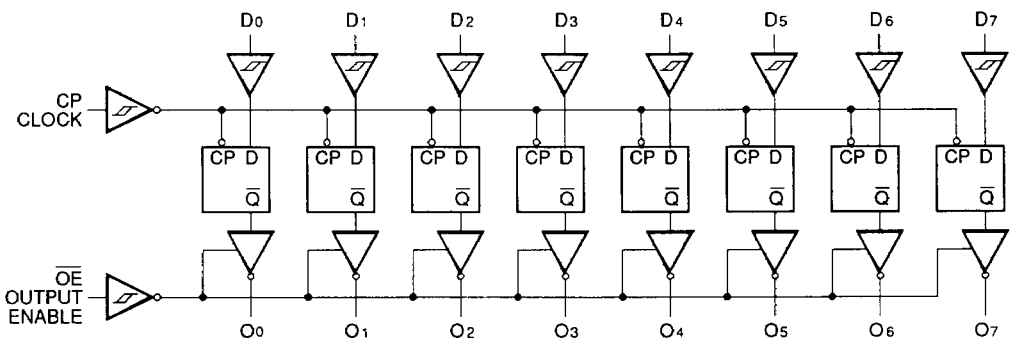
The FBT series of BiCMOS Octal D Registers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT374 series are 8-bit registers consisting of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the Output Enable ($\overline{OE}$) is LOW, the eight outputs are enabled. When $\overline{OE}$ is HIGH, the outputs are in the three-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

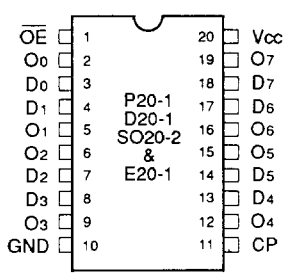
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM

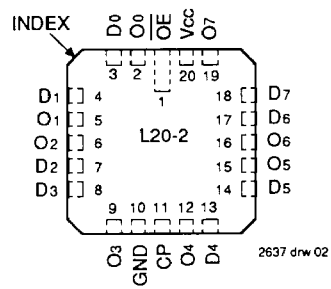


2637 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
D_0-D_7	The D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
O_0-O_7	The register three-state outputs.
$\overline{OE}$	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

2637 tbl 01

FUNCTION TABLE[1]

Function	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	Clock	D_I	O_I	$\overline{Q}_I$
Load Register	L	∫	L	L	H
	L	∫	H	H	L
	H	∫	L	Z	H
	H	∫	H	Z	L

2637 tbl 02

NOTE:
1. H = HIGH
   L = LOW
   X = Don't Care
   Z = High Impedance
   ∫ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2637 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2637 tbl 05
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}			V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		-75	-150	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.4	3.3	—	V
			I_{OH} = -18mA MIL. I_{OH} = -24mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2637 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	7.8[5]	
		$\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	—	16.8[5]	

NOTES:

2637 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT374				IDT54/74FBT374A				IDT54/74FBT374C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to On	C_L = 50pF R_L = 500Ω	2.0	10.0	—	—	2.0	6.5	—	—	—	5.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.3	—	—	1.5	6.5	—	—	—	5.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	6.8	—	—	1.5	5.5	—	—	—	5.0	—	—	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CP		6.5	—	—	—	2.0	—	—	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW D_n to CP		0	—	—	—	1.5	—	—	—	1.5	—	—	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	—	—	5.0	—	—	—	5.0	—	—	—	ns

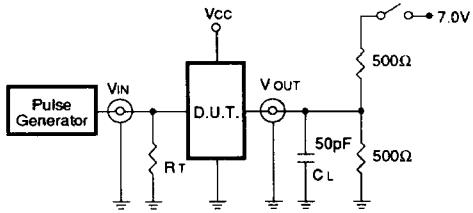
NOTES:

2637 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

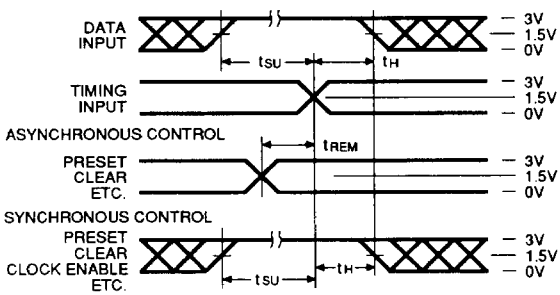
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

2637 tbl 08

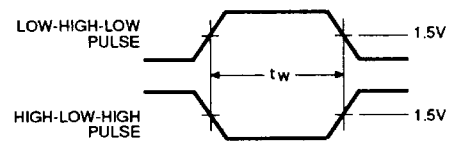
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

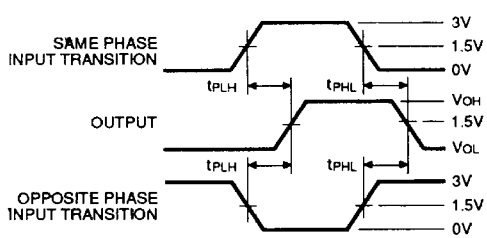
SET-UP, HOLD AND RELEASE TIMES



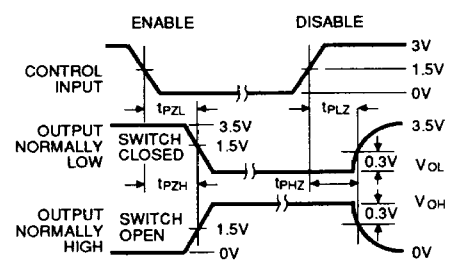
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



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NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

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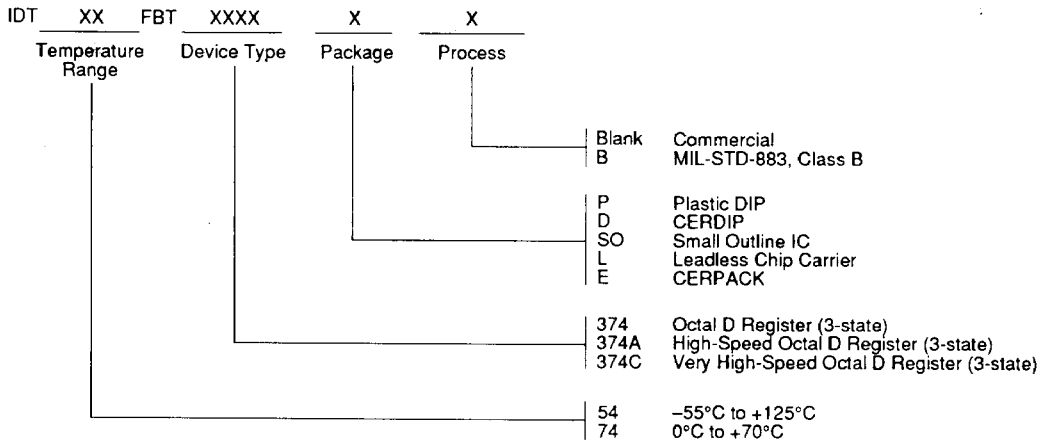
ORDERING INFORMATION



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