SN74I VC241 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Typical VOLP (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V Vcc)
- Package Options include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DВ,	DW,	OR	PW	PA	CKA	GE
	(TOP	VIE	W)		

		_	
10E [1	\bigcup_{20}] v _{cc}
1A1 [2	19] 20E
2Y4 [3	18] 1Y1
1A2 [4	17	2A4
2Y3 [5	16] 1Y2
1A3 [6	15] 2A3
2Y2 [7	14	1Y3
1A4 [8	13	2A2
2Y1 [9	12	1Y4
GND [10	11	2A1

description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC241 is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the LVC240 and LVC244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical \overline{OE} (active-low output-enable) inputs, and complementary OE and \overline{OE} inputs.

The SN74LVC241 is organized as two 4-bit line drivers with separate output-enable (1OE, 2OE) inputs. When 10E is low or 20E is high, the device passes data from the A inputs to the Y outputs. When 10E is high or 20E is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

The SN74LVC241 is characterized for operation from -40°C to 85°C.

FUNCTION TABLES

L Incompany					
INP	UTS	OUTPUT			
10E 1A		1Y			
L	н_	Н			
L	L	L			
н	Х	Z			

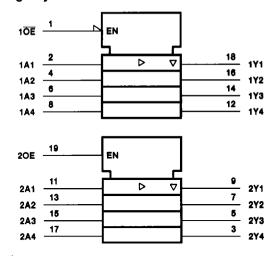
INPUTS		OUTPUT		
2OE	2A	2Y		
Н	Н	Н		
н	L	L		
L_	Х	z		

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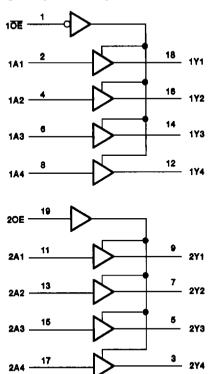
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	state
or power-off state, VO (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, IOK (VO < 0)	
Continuous output current, IO (VO = 0 to VCC)	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see	Note 3): DB package 0.6 W
	DW package 1.6 W
	PW package 0.7 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V _{CC} Supply voltage	Cumply voltage	Operating	2	3.6	v
	Supply voltage	Data retention only	1.5		'
V _{IH} _	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧
٧ _I	Input voltage		0	5.5	V
	Output voltage	High or low state	0	Vcc	V
v _o	Output Voltage	3 state	0 5.5	'	
IOH High-	Litab lavial autorit arment	V _{CC} = 2.7 V	T	0.8 0 5.5 0 V _{CC}	mA
	High-level output current	V _{CC} = 3 V		-24	
loL	Law lavel autout auropat	V _{CC} = 2.7 V		3.6 0.8 5.5 VCC 5.5 -12 -24 12 24	
	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP\$	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
	10 114	2.7 V	2.2		
Vон	IOH = - 12 mA	3 V	2.4		
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	٧
VOL	I _{OL} = 12 mA	2.7 V		0.4	
	I _{OL} = 24 mA	3 V		0.55	l
lj	V _I = 5.5 V or GND	3.6 V		±5	μА
loz	V _O = 5.5 V or GND	3.6 V		±10	μΑ
lcc	V _I = V _{CC} or GND, I _O = 0	3.6 V		20	μА
Δlcc	One input at VCC - 0.6 V, Other inputs at VCC or GND	3 V to 3.6 V		500	μА
Ci	VI = VCC or GND	3.3 V			ρF
Co	Vo = Vcc or GND	3.3 V			ρF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.