



FAST CMOS 18-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16500/AT/CT/ET

FEATURES:

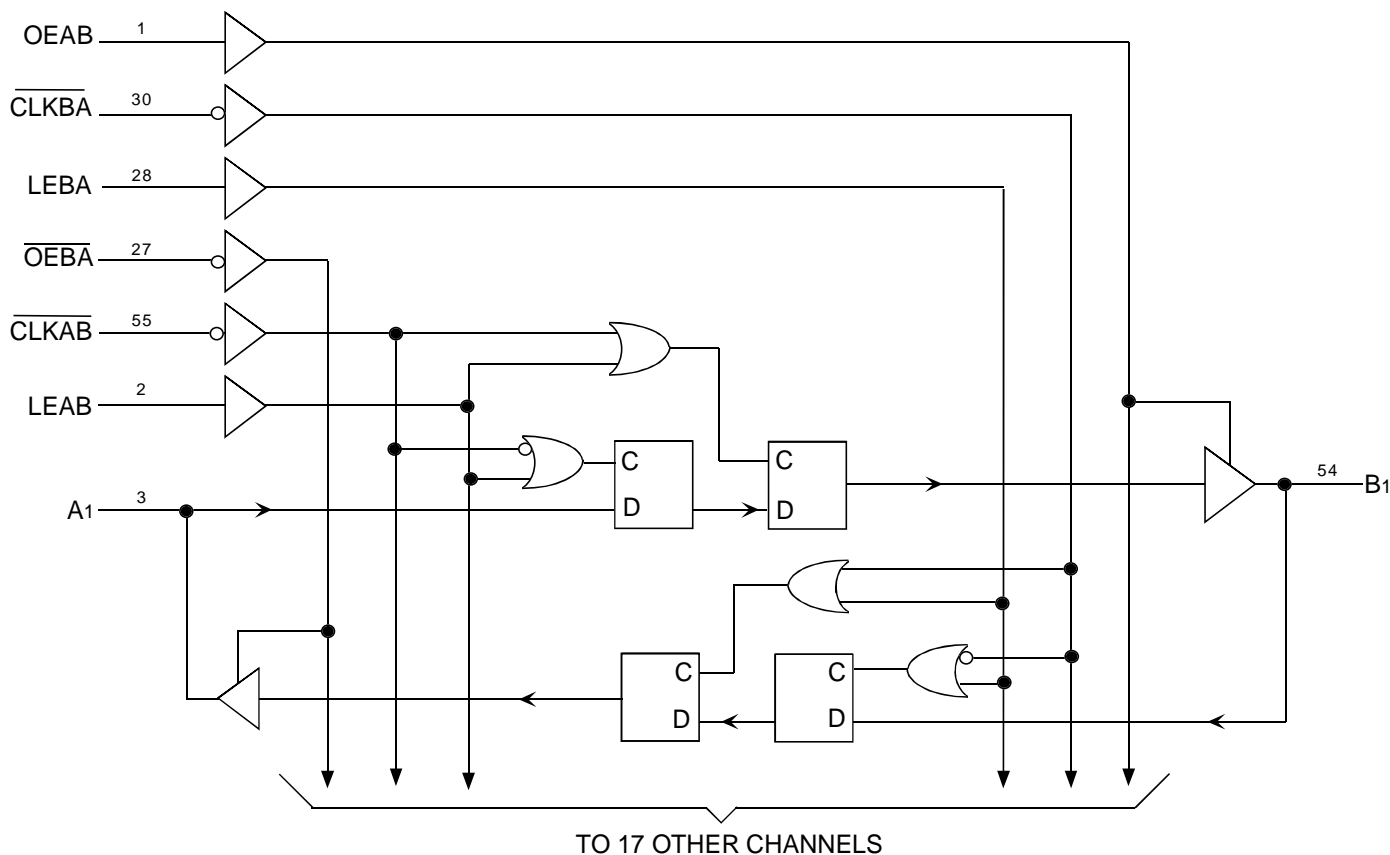
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu A$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch CERPACK packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 5V \pm 10\%$
- High drive outputs (-32mA I_{OH} , 64mA I_{OL})
- Power off disable outputs permit "live insertion"
- Typical VOLP (Output Ground Bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^\circ C$

DESCRIPTION:

The FCT16500AT/CT/ET 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch enable (\overline{LEAB} and \overline{LEBA}) and clock (\overline{CLKAB} and \overline{CLKBA}) inputs. For A-to-B data flow, the device operates in transparent mode when \overline{LEAB} is high. When \overline{LEAB} is low, the A data is latched if \overline{CLKAB} is held at a high or low logic level. If \overline{LEAB} is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of \overline{CLKAB} . \overline{OEAB} performs the output enable function on the B port. Data flow from B port to A port is similar but uses \overline{OEBA} , \overline{LEBA} and \overline{CLKBA} . Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16500AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

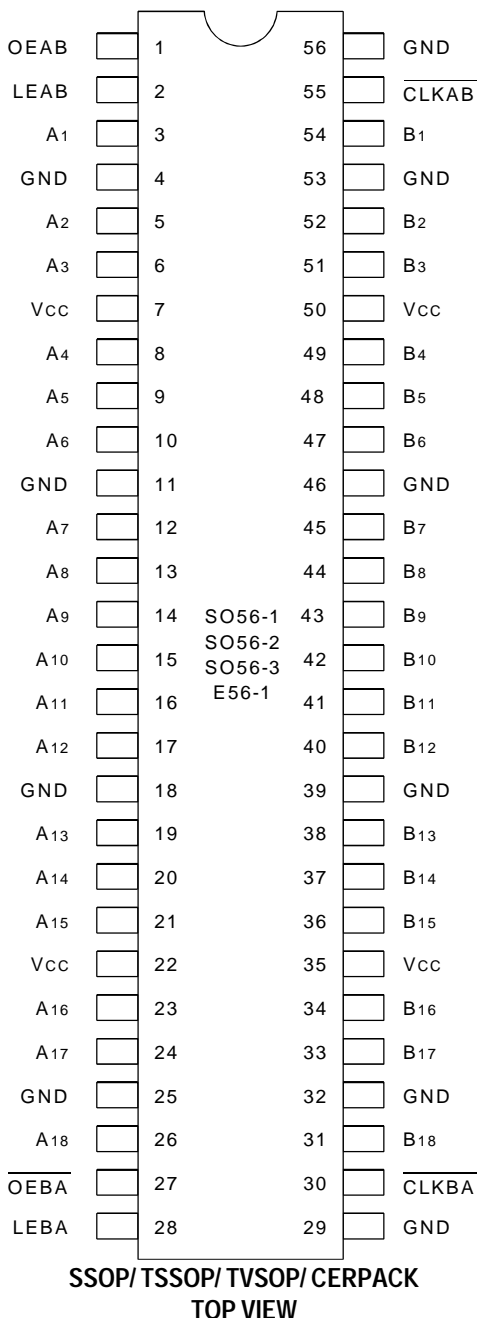
FUNCTIONAL BLOCK DIAGRAM



MILITARY AND COMMERCIAL TEMPERATURE RANGES

AUGUST 1999

PIN CONFIGURATION



PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
\overline{CLKAB}	A-to-B Clock Input (Active LOW)
\overline{CLKBA}	B-to-A Clock Input (Active LOW)
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	3.5	6	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	3.5	8	pF

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NOTE:

- This parameter is measured at characterization but not tested.

FUNCTION TABLE^(1,4)

Inputs				Outputs	
OEAB	LEAB	\overline{CLKAB}	Ax	Bx	
L	X	X	X	Z	
H	H	X	L	L	
H	H	X	H	H	
H	L	↓	L	L	
H	L	↓	H	H	
H	L	H	X	B ⁽²⁾	
H	L	L	X	B ⁽³⁾	

NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{OEBA} , LEBA, and \overline{CLKBA} .
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that \overline{CLKAB} was LOW before LEAB went LOW.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-impedance
↓ = HIGH-to-LOW Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}	(3-State Output pins) ⁽⁵⁾		$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

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OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_O	Output Drive Current	$V_{CC} = \text{Max.}, V_O = 2.5\text{V}^{(3)}$		-50	—	-180	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.4	3.5	—	V
			$I_{OH} = -24\text{mA MIL.}$ $I_{OH} = -32\text{mA COM'L.}^{(4)}$	2	3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 48\text{mA MIL.}$ $I_{OL} = 64\text{mA COM'L.}$	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	± 1	μA

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $OEAB = \overline{OEBA} = V_{CC} \text{ or GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu A /$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz} (\overline{CLKAB})$ 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz} (\overline{CLKAB})$ 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ Eighteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.5	20.8 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current} (I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input} (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

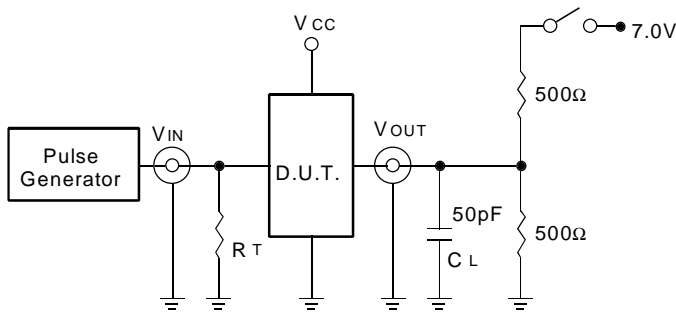
Symbol	Parameter	Condition ⁽¹⁾	FCT16500AT				FCT16500CT				FCT16500ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
f _{MAX}	CLKAB or CLKBA frequency ⁽⁴⁾	C _L = 50pF	—	150	—	150	—	150	—	150	—	150	—	—	MHz
t _{PLH} t _{PHL}	Propagation Delay Ax to Bx or Bx to Ax	RL = 500Ω	1.5	5.1	1.5	5.6	1.5	4.6	1.5	4.6	—	3.8	—	—	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	1.5	6	1.5	5.3	1.5	5.6	—	4.2	—	—	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	6	1.5	5.3	1.5	5.4	—	4.2	—	—	ns
t _{PZH} t _{PZL}	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	6	1.5	6.4	1.5	5.6	1.5	6	—	4.8	—	—	ns
t _{PHZ} t _{PLZ}	Output Disable Time OEBA to Ax, OEAB to Bx		1.5	5.6	1.5	6	1.5	5.2	1.5	5.6	—	4	—	—	ns
t _{SU}	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		3	—	3	—	3	—	3	—	2.4	—	—	—	ns
t _H	Hold Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	0	—	0	—	0	—	—	—	ns
t _{SU}	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock HIGH	3	—	3	—	3	—	3	—	2	—	—	—	ns
		Clock LOW	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
t _H	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	1.5	—	1.5	—	0.5	—	—	—	ns
t _W	LEAB or LEBA Pulse Width HIGH ⁽⁴⁾		3	—	3	—	3	—	3	—	3	—	—	—	ns
t _W	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁴⁾		3	—	3	—	3	—	3	—	3	—	—	—	ns
t _{SK(0)}	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

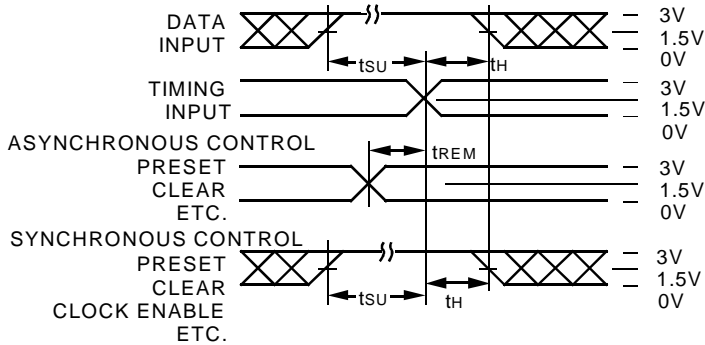
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DEFINITIONS:

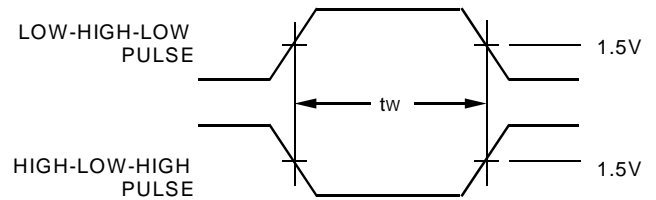
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

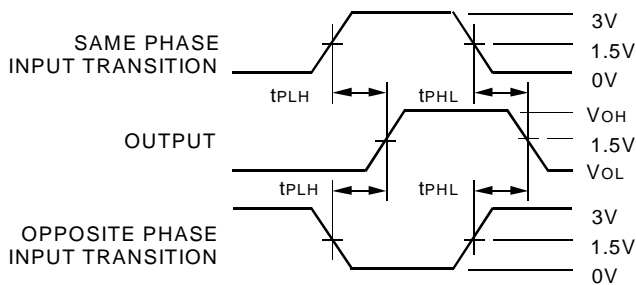
SET-UP, HOLD, AND RELEASE TIMES



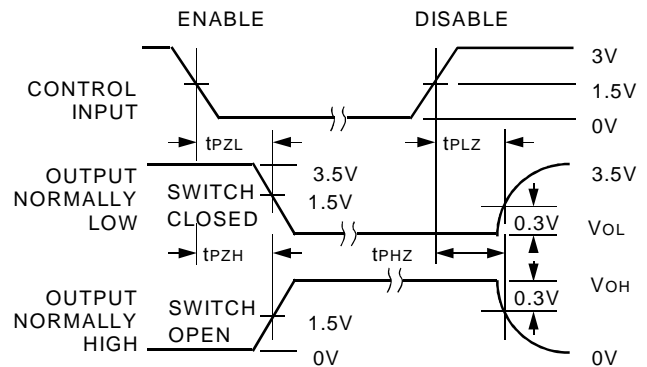
PULSE WIDTH



PROPAGATION DELAY



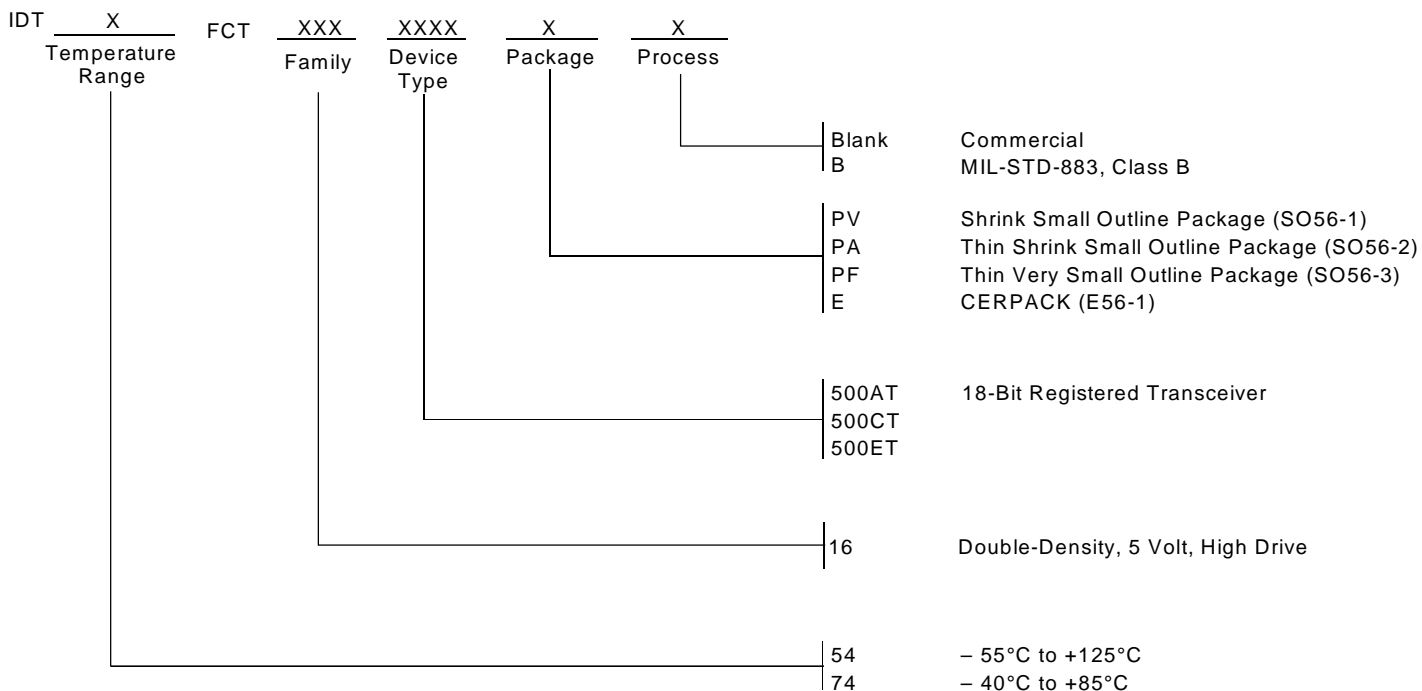
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.

ORDERING INFORMATION



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