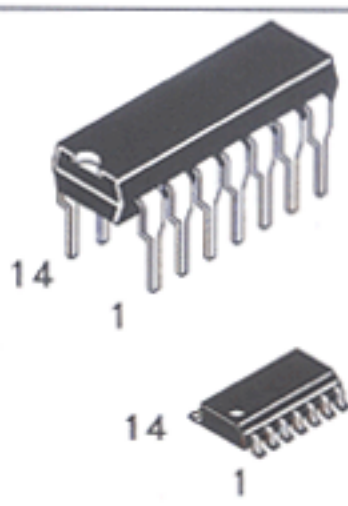
DV74ACT74 Available Q2, 1995

Dual D-Type Positive Edge-Triggered Flip-Flop

DV74AC74
DV74ACT74



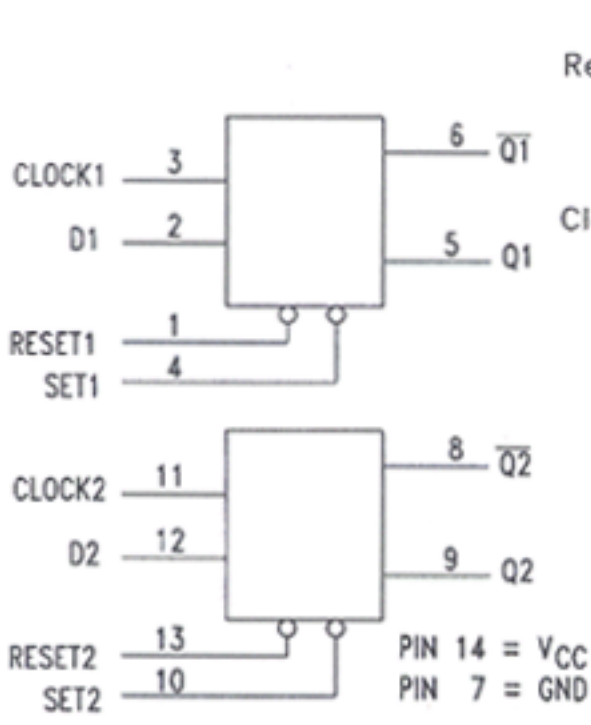
N Suffix
Plastic DIP
AVG-001 Case

D Suffix
Plastic SOP
AVG-002 Case

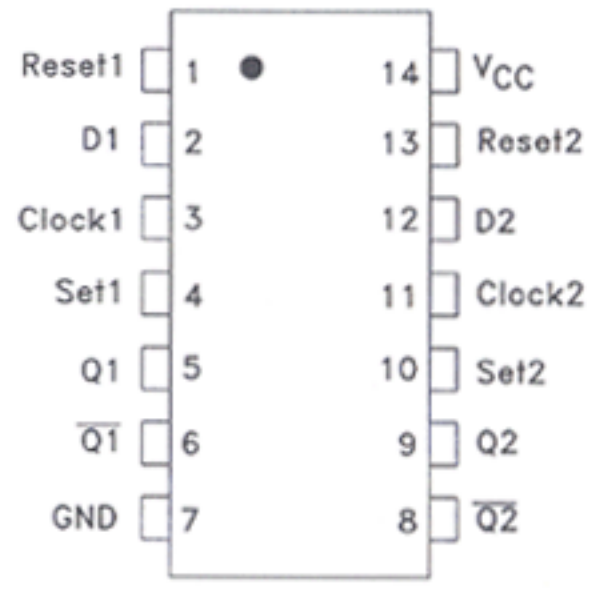
This is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q,$\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

- **Advanced very high speed CMOS**
- **Outputs source/sink 24 mA**
- **Transmission line driving 50 ohms**
- **ACT has TTL compatible inputs**
- **AC device operation guaranteed from 2 to 6 volts**
- **DC & AC Parameters guaranteed over –40 to +85°C**

CONNECTION DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE
(Each Flip-Flop)

Inputs				Outputs	
Set	Reset	Clock	Dn	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$
H	H	H	X	Q_0	$\overline{Q}_0$
H	H	↓	X	Q0	$\overline{Q}_0$

* Both outputs will remain high as long as set and re set are low, but the output states are unpredictable i set and reset go high simultaneously
H=HighLevelLogic
L=LowLevelLogic
X=EitherLoworHighLogicLevel
↑= TransitionLowtoHigh
↓=TransitionHightoLow
Q_0=Previous Q($\overline{Q}$) before LOW to HIGH of Clock

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	AC74, ACT74	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
Tstg	Storage Temperature	– 65 to +150	°C

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GUARANTEED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage, (Ref. to GND)		0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) **'AC** Devices	V_{CC} @ 3.0 V			150	ns/V
		V_{CC} @ 4.5 V			40	ns/V
		V_{CC} @ 5.5 V			25	ns/V
t_r, t_f	Input Rise and Fall Time (Note 2) **'ACT** Devices	V_{CC} @ 4.5 V			10	ns/V
		V_{CC} @ 5.5 V			8.0	ns/V
T_A	Operating Ambient Temperature Range		–40	25	85	°C
C_{IN}	Input Capacitance	V_{CC} = 5.0 V		4.5		pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0 V		35		pF

1. V_{IN} from 30% to 70% V_{CC}
2. V_{IN} from 0.8 to 2.0 V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	AC74			Unit
				TA = +25°C		TA = –40 to +85°C	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1 V	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1 V	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High Level Output Voltage	I_{OUT}= –50 µA	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V
		V_{IN} = V_{IL} or V_{IH} –12mA I_{OH} –24mA –24mA	3.0 4.5 5.5		2.56 3.86 4.86	2.46 3.76 4.76	V
V_{OL}	Maximum Low Level Output Voltage	I_{OUT} = 50 µA	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN} = V_{IL} or V_{IH} 12mA I_{OL} 24mA 24mA	3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = V_{CC} or GND	5.5		±0.1	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5		4.0	40	µA

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AC CHARACTERISTICS over full operating conditions

Symbol	Parameter	V_{CC} ±10% (V)	AC74				Unit
			T_A = +25°C, C_L = 50 pF		T_A = – 40°C to +85°C, C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	3.3 5.0	100 140		95 125		MHz
t_{PLH}	Propagation Delay Reset or Set to Qn or $\overline{Q}_n$	3.3 5.0	5.0 3.5	12.5 9.0	4.0 3.0	13.0 10.0	ns
t_{PHL}	Propagation Delay Reset or Set to Q_n or $\overline{Q}_n$	3.3 5.0	4.0 3.0	12.0 9.5	3.5 2.5	13.5 10.5	ns
t_{PLH}	Propagation Delay Clock to Q_n or $\overline{Q}_n$	3.3 5.0	4.5 3.5	13.5 10.0	4.0 5.0	16.0 10.5	ns
t_{PHL}	Propagation Delay Clock to Q_n or $\overline{Q}_n$	3.3 5.0	3.5 2.5	14.0 10.0	3.5 2.5	14.5 10.5	ns
t_s	Set-up Time, HIGH or LOW D_n to Clock	3.3 5.0	4.0 3.0		4.5 3.0		ns
t_h	Hold Time, HIGH or LOW D_n to Clock	3.3 5.0	0.5 0.5		0.5 0.5		ns
t_w	Clock or Reset or Set Pulse Width	3.3 5.0	5.5 4.5		7.0 5.0		ns
t_{rec}	Recovery Time Reset or Set to Clock	3.3 5.0	0 0		0 0		ns

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	ACT74			Unit
				TA = +25°C		TA = –40 to +85°C	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1 V	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC} – 0.1 V	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High Level Output Voltage	I_{OUT} = –50 µA	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V
		V_{IN} = V_{IL} or V_{IH} I_{OH} –24mA –24 mA	4.5 5.5		3.86 4.86	3.76 4.76	V
V_{OL}	Maximum Low Level Output Voltage	I_{OUT} = 50 µA	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V
		V_{IN} = V_{IL} or V_{IH} I_{OL} 24mA 24 mA	4.5 5.5		0.36 0.36	0.44 0.44	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = VCC or GND	5.5		±0.1	±1.0	µA
ΔI_{CCT}	Additional Max I_{CC}/Input	V_{IN} = V_{CC} – 2.1 V	5.5	0.6		1.5	mA

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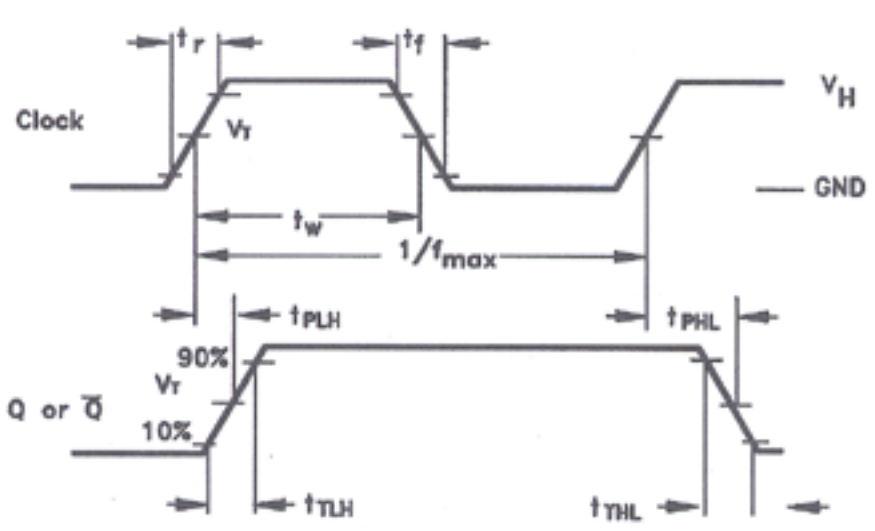
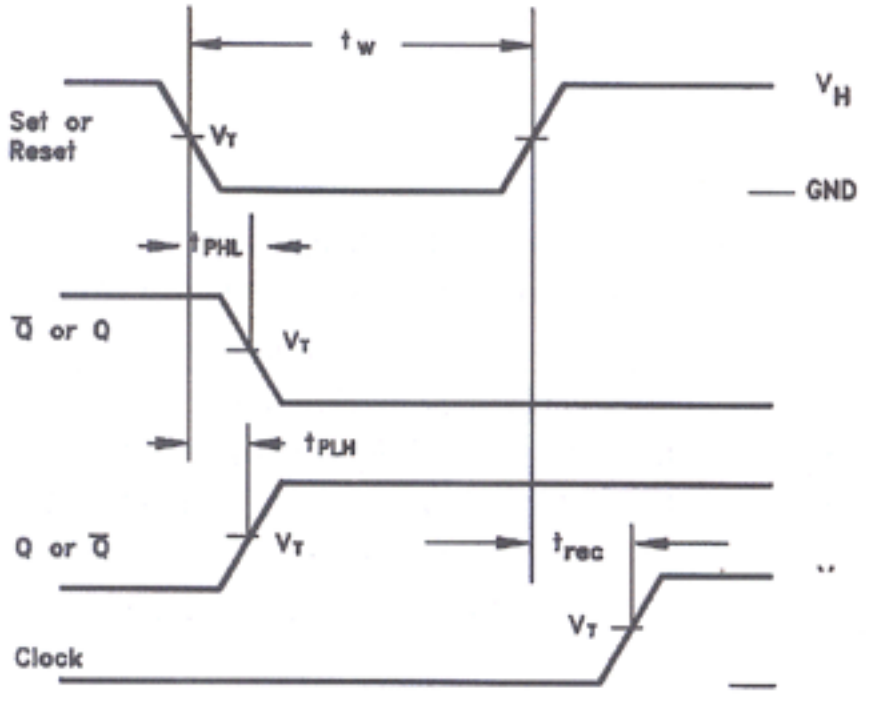
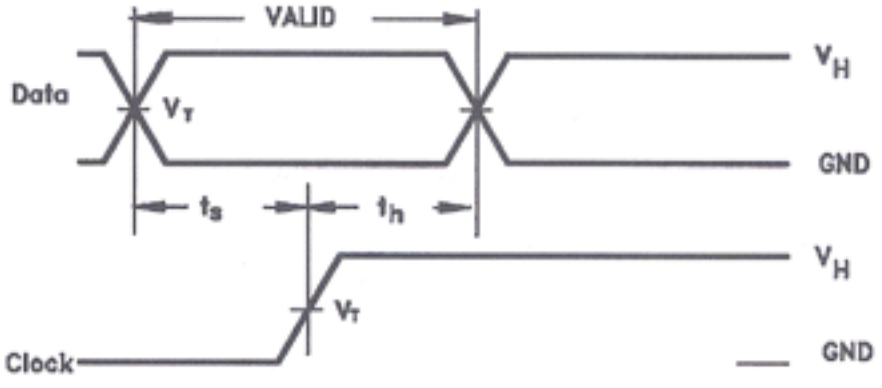
AC CHARACTERISTICS over full operating conditions

Symbol	Parameter	Vcc ±10% (V)	ACT74				Unit
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	5.0	145		125		MHz
t_{PLH}	Propagation Delay Reset or Set to Q_n or $\overline{Q}_n$	5.0	3.0	9.5	2.5	10.5	ns
t_{PHL}	Propagation Delay Reset or Set to Q_n or $\overline{Q}_n$	5.0	3.0	10.0	3.0	11.5	ns
t_{PLH}	Propagation Delay Clock to Q_n or $\overline{Q}_n$	5.0	4.0	11.0	4.0	13.0	ns
t_{PHL}	Propagation Delay Clock to Q_n or $\overline{Q}_n$	5.0	3.5	10.0	3.0	11.5	ns
t_s	Set-up Time, HIGH or LOW D_n to Clock	5.0	3.0		3.5		ns
t_h	Hold Time, HIGH or LOW D_n to Clock	5.0	1.0		1.0		ns
t_w	Clock or Reset or Set Pulse Width	5.0	5.0		6.0		ns
t_{rec}	Recovery Time Reset or Set to Clock	5.0	0		0		ns

SWITCHING WAVEFORMS







Input and output threshold voltage:
V_T = 50% Vcc for AC; 1.5V for ACT
V_H = Vcc for AC, 3V for ACT

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