BURR-BROWN®

ADS7811

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

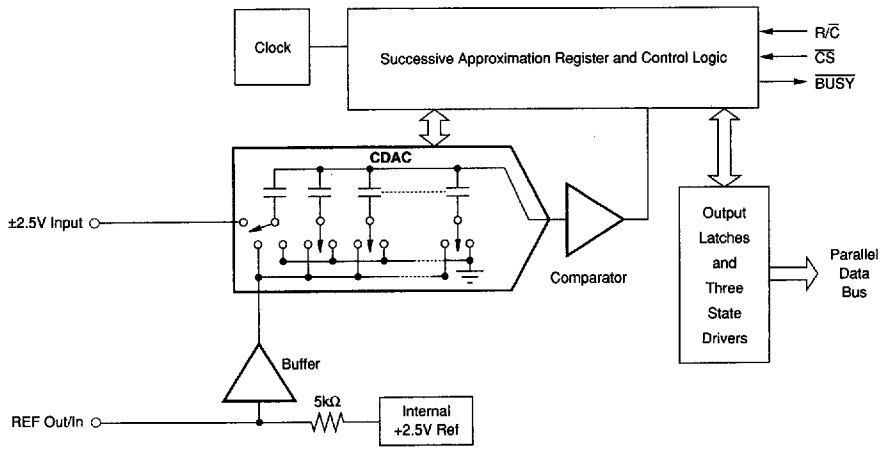
16-Bit 250kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

- **250kHz SAMPLING RATE**
- **±2.5V INPUT RANGE**
- **COMPLETE WITH S/H, REF, CLOCK, ETC.**
- **FULL PARALLEL DATA OUTPUT WITH LATCHES**
- **28-PIN 0.3" PLASTIC DIP AND SOIC**
- **86dB min SINAD WITH 100kHz INPUT**
- **INL: ±1.5 LSB max**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **DNL: 16 Bits "No Missing Codes"**

DESCRIPTION

The ADS7811 is a complete 16-bit sampling analog-to-digital converter using state-of-the art CMOS structures. It contains a 16-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers. The 28-pin ADS7811 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –25°C to +85°C range. The ADS7811 is specified at a 250kHz sampling rate, and guaranteed over the full temperature range. A ±2.5V input range allows development of precision systems using only ±5V supplies.



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SPECIFICATIONS

At T_A = –25°C to +85°C, f_S = 250kHz, V_{DIG} = $+V_{ANA}$ = +5V ±5%, and $-V_{ANA}$ = –5V ±5%, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7811P, U			ADS7811PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Range			±2.5V			*		V
Impedance			100			*		MΩ
Capacitance			50			*		pF
THROUGHPUT SPEED								
Conversion Cycle	Acquire and Convert			4.0			*	µs
Throughput Rate		250			*			kHz
DC ACCURACY								
Integral Linearity Error			±3			±1.5	±3	LSB[1]
No Missing Codes		14			15			Bits
Transition Noise[2]			1			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Bipolar Zero Error[3]				±10			*	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Power Supply Sensitivity								
(V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V,		±4			*		LSB
	–5.25V < $-V_{ANA}$ < –4.75V		±4			*		LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 100kHz	90			96			dB[5]
Total Harmonic Distortion	f_{IN} = 100kHz			–90			–96	dB
Signal-to-(Noise+Distortion)	f_{IN} = 100kHz	84			86			dB
	–60dB Input		28			30		dB
Signal-to-Noise	f_{IN} = 100kHz	84			86			dB
Full Power Bandwidth[6]			1			*		MHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Transient Response	FS Step		600			*		ns
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current			1			*		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	V_{REF} = +2.5V			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.8		V_D +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format				Parallel 16 bits				
Data Coding				Binary Two's Complement				
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 200µA	+4			*			V
Leakage Current	High-Z State,			±5			*	µA
	V_{OUT} = 0V to V_{DIG}							
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				65			*	ns
Bus Relinquish Time				65			*	ns

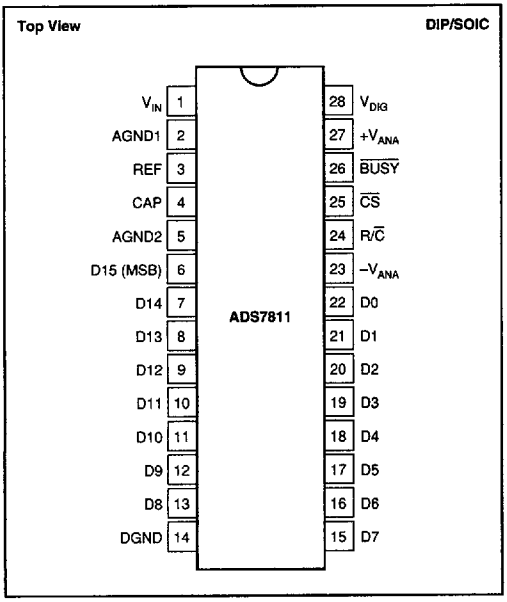
SPECIFICATIONS (CONT)

At T_A = –25°C to +85°C, f_S = 250kHz, V_{DIG} = $+V_{ANA}$ = +5V ±5%, and $-V_{ANA}$ = –5V ±5%, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7811P, U			ADS7811PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
V_{DIG}		+4.75	+5	+5.25	*	*	*	V
$+V_{ANA}$		+4.75	+5	+5.25	*	*	*	V
$-V_{ANA}$		–5.25	–5	–4.75	*	*	*	V
Power Dissipation	f_S = 250kHz		160	250			*	mW
TEMPERATURE RANGE								
Specified Performance		–25		+85	*		*	°C
Storage		–55		+125	*		*	°C

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±2.5V input ADS7811, one LSB is 76µV. (2) Typical rms noise at worst case transitions and temperatures. (3) Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±2.5V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

PIN CONFIGURATION



PIN #	NAME	DESCRIPTION
1	V_{IN}	Analog Input. Full-scale input range is ±2.5V.
2	AGND1	Analog Ground. Used internally as ground reference point.
3	REF	Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, connect to ground with a 0.1µF ceramic capacitor.
4	CAP	Reference compensation capacitor. 2.2µF tantalum capacitor to ground.
5	AGND2	Analog ground.
6	D15 (MSB)	Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND	Digital Ground.
15	D7	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	$-V_{ANA}$	Analog negative supply input. Nominally –5V. Decouple to analog ground with 0.1µF ceramic and 10µF tantalum capacitors.
24	R/$\overline{C}$	Read/convert input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the output data bits.
25	$\overline{CS}$	Chip select. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH, a falling edge on $\overline{CS}$ will enable the output data bits.
26	$\overline{BUSY}$	Busy output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises or another conversion will start without time for signal acquisition.
27	$+V_{ANA}$	Analog positive supply input. Nominally +5V. Connect directly to pin 28. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}	Digital supply input. Nominally +5V. Connect directly to pin 27. Decouple to digital ground with 0.1µF ceramic and 10µF tantalum capacitors.

TABLE I. Pin Assignments.