SN74LVC16245
16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

- Member of the Texas Instruments *Widebus*™ Family
- *EPIC* ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DGG OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	1OE
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2OE

description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.
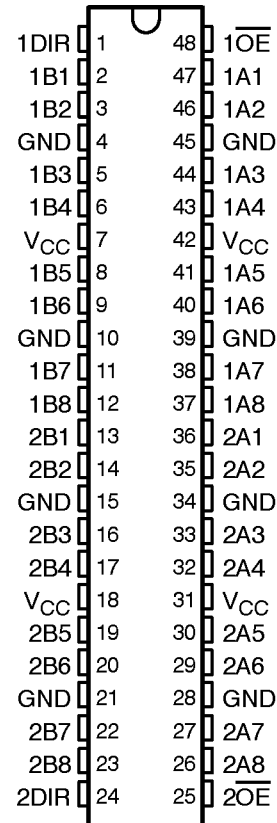
The SN74LVC16245 is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TEXAS INSTRUMENTS
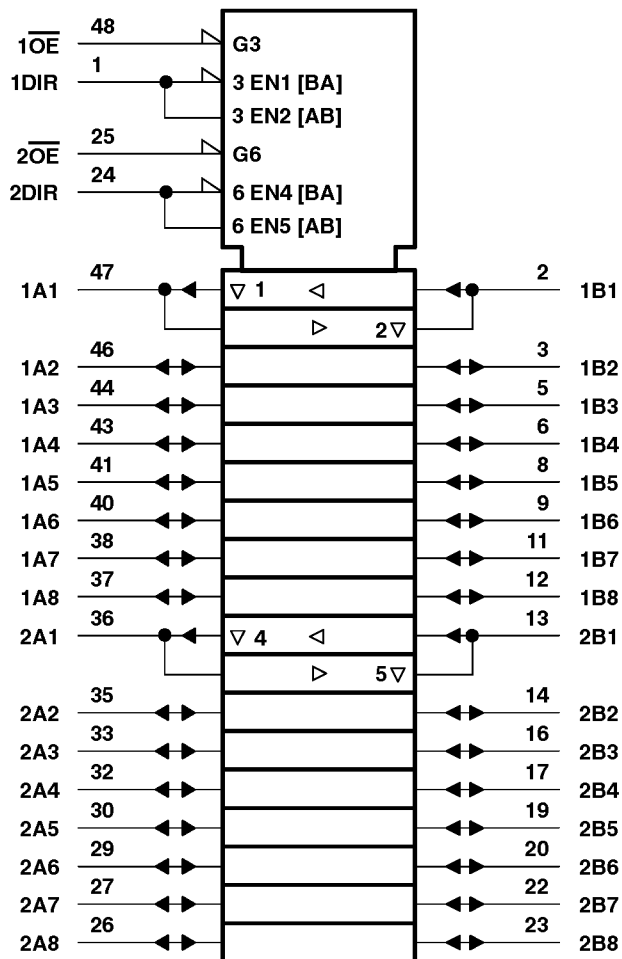
logic symbol†

logic diagram (positive logic)

To Seven Other Channels

To Seven Other Channels
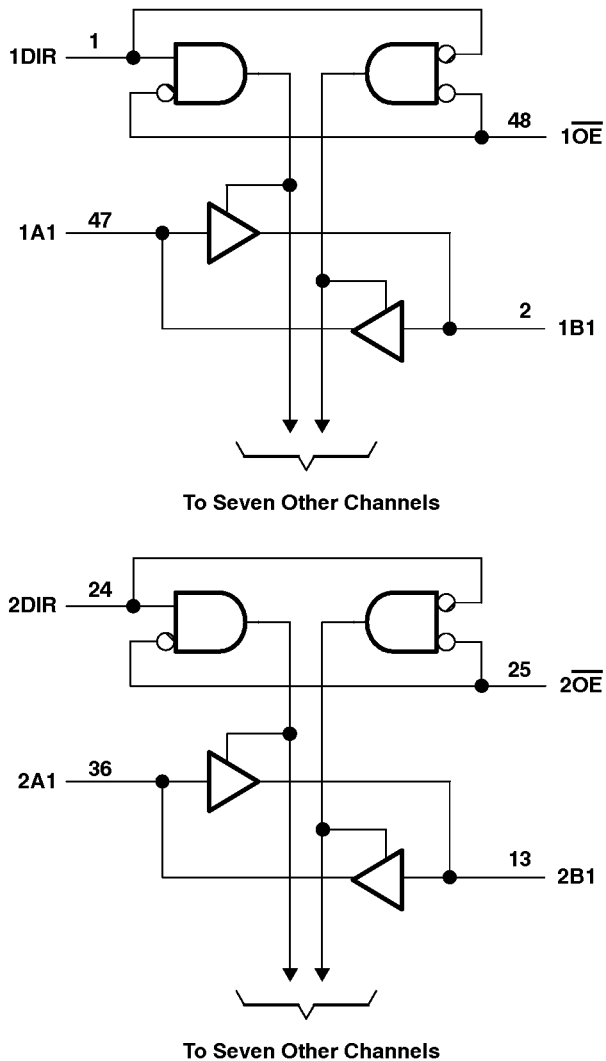
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... −0.5 V to 4.6 V
Input voltage range, V_I (I/O ports) (see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) .... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package .... 0.85 W
DL package .... 1.2 W
Operating free-air temperature range, T_A .... −40°C to 85°C
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V		−12	mA
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V		12	mA
		V_{CC} = 3 V		24	
Δt/ΔV	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: Unused or floating control pins must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu A$		MIN to MAX‡	$V_{CC}-0.2$			V
		$I_{OH} = -12\ mA$		2.7	2.2			
				3	2.4			
		$I_{OH} = -24\ mA$		3	2			
V_{OL}		$I_{OL} = 100\ \mu A$		MIN to MAX‡			0.2	V
		$I_{OL} = 12\ mA$		2.7			0.4	
		$I_{OL} = 24\ mA$		3			0.55	
I_I	Control inputs	$V_I = V_{CC}$ or GND		3.6			±5	μA
$I_{I(hold)}$	Data inputs	$V_I = 0.8\ V$		3		75		μA
		$V_I = 2\ V$				-75		
I_{OZ}§		$V_O = V_{CC}$ or GND		3.6			±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	$I_O = 0$	3.6			40	μA
ΔI_{CC}		$V_{CC} = 3\ V$ to 3.6 V, One input at $V_{CC} - 0.6\ V$, Other inputs at V_{CC} or GND					500	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND		3.3		2.5		pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3		3.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
t_{pd}	A	B	1.5	3.8	6.5		7.5	ns
t_{en}	$\overline{OE}$	B	1.5	4.7	8		9	ns
t_{dis}	$\overline{OE}$	B	1.5	4.8	7.5		8.5	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

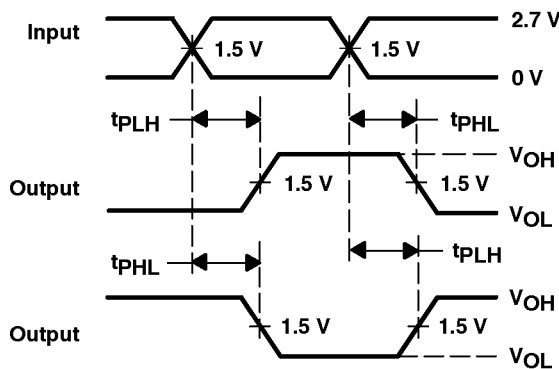## PARAMETER MEASUREMENT INFORMATION
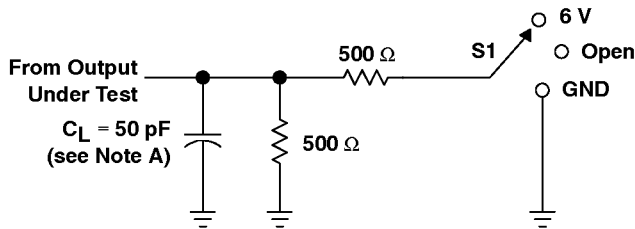
LOAD CIRCUIT FOR OUTPUTS

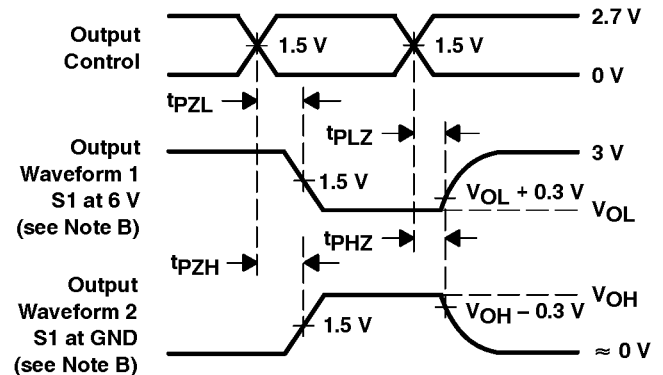| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
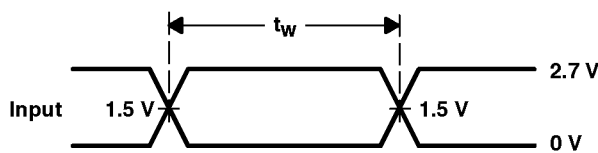
VOLTAGE WAVEFORMS
PULSE DURATION
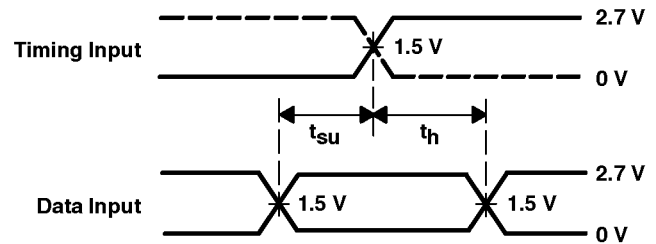
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms