



Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUS TRANSCEIVER/ REGISTERS (3-STATE)

IDT54/74FCT16646T/AT/CT/ET
IDT54/74FCT162646T/AT/CT/ET

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **High-speed, low-power CMOS replacement for ABT functions**
 - **Typical tsk(o) (Output Skew) < 250ps**
 - **Low input and output leakage $\leq 1\mu\text{A}$ (max.)**
 - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
 - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
 - Extended commercial range of -40°C to +85°C
 - Vcc = 5V \pm 10%
- **Features for FCT16646T/AT/CT/ET:**
 - High drive outputs (-32mA IOH, 64mA IOL)
 - Power off disable outputs permit "live insertion"
 - Typical VOLP (Output Ground Bounce) < 1.0V at Vcc = 5V, TA = 25°C
- **Features for FCT162646T/AT/CT/ET:**
 - Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
 - Reduced system switching noise
 - Typical VOLP (Output Ground Bounce) < 0.6V at Vcc = 5V, TA = 25°C

74FCT162646T/AT/CT/ET 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (xDIR), over-riding Output Enable control (xOE) and Select lines (xSAB and xSBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the LOW-to-HIGH transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16646T/AT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

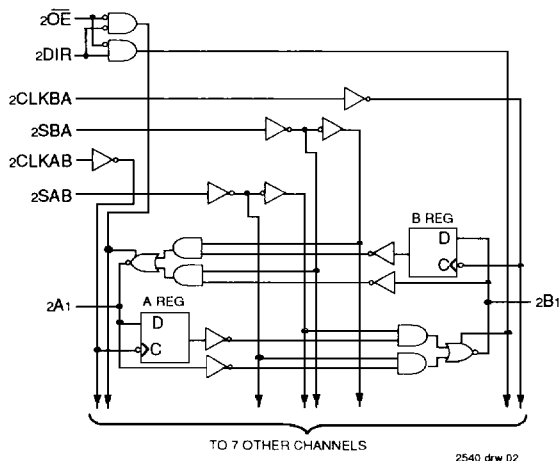
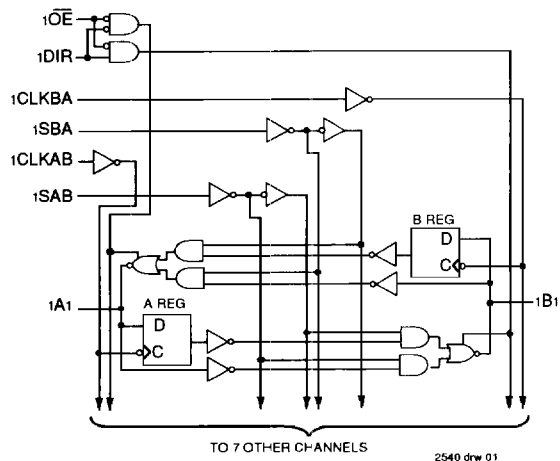
The IDT54/74FCT162646T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The IDT54/74FCT162646T/AT/CT/ET are plug-in replacements for the IDT54/74FCT16646T/AT/CT/ET and 54/74ABT16646 for on-board bus interface applications.

DESCRIPTION:

The IDT54/74FCT16646T/AT/CT/ET and IDT54/

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FUNCTIONAL BLOCK DIAGRAM

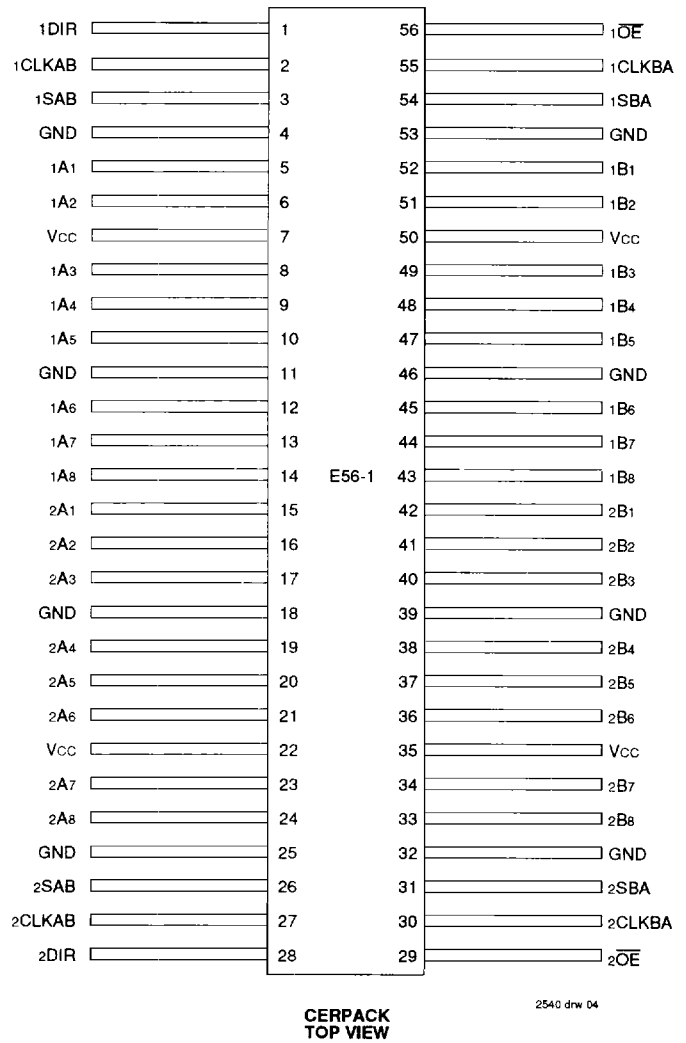
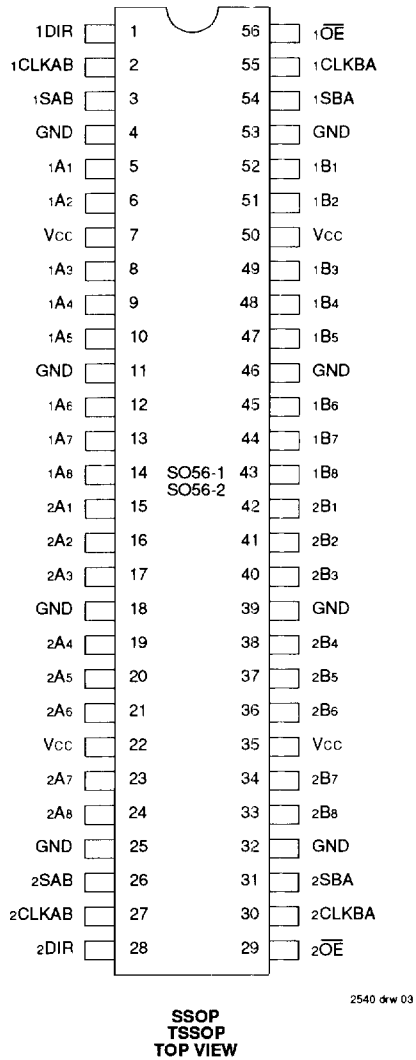


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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1994

PIN CONFIGURATIONS



PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xDIR, xOE	Output Enable Inputs

2540 tbl 01

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6.0	pF
CI/O	I/O Capacitance	VOUT = 0V	3.5	8.0	pF

NOTE:

1. This parameter is measured at characterization but not tested.

2540 tbl 02

FUNCTION TABLE⁽²⁾

Inputs						Data I/O ⁽¹⁾		Operation or Function
xOE	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus
L	L	X	H or L	X	H			
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus
L	H	H or L	X	H	X			

NOTES:

- The data output functions may be enabled or disabled by various signals at the xOE or xDIR inputs. Data input functions are always enabled i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition

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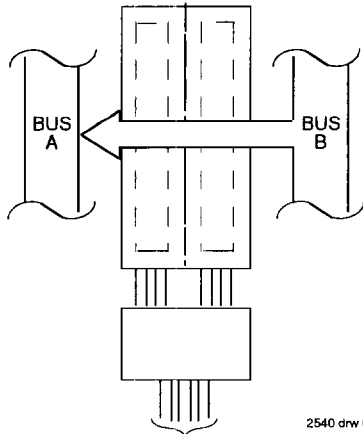
ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc +0.5	-0.5 to Vcc +0.5	V
TA	Operating Temperature	-40 to +85	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

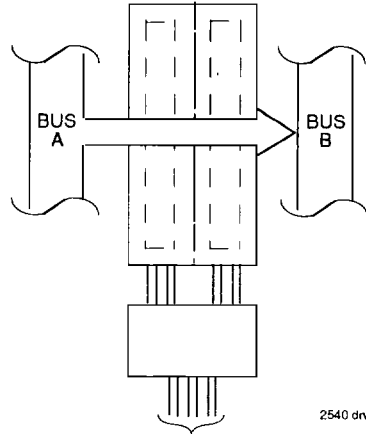
2540 tbl 04



2540 drw 05

xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

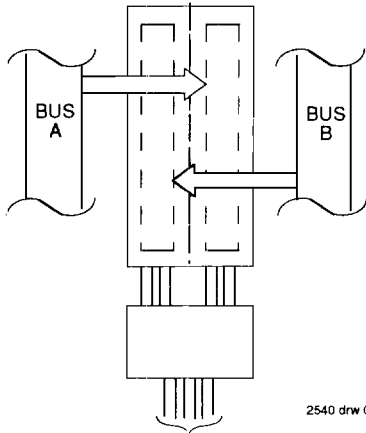
REAL-TIME TRANSFER
 BUS B TO A



2540 drw 06

xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

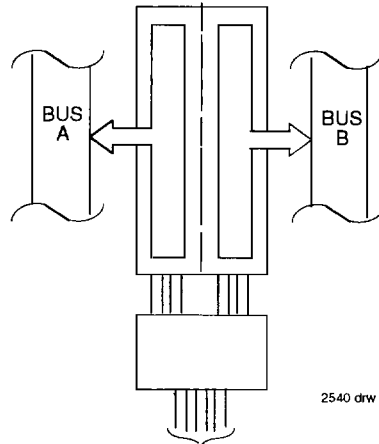
REAL-TIME TRANSFER
 BUS A TO B



2540 drw 07

xDIR	xOE	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

STORAGE FROM
 A AND/OR B



2540 drw 08

xDIR ⁽¹⁾	xOE	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

TRANSFER STORED
 DATA TO A AND/OR B

NOTE:

1. Cannot transfer data to A bus and B bus simultaneously.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁵⁾		—	—	—	± 1	
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}	(3-State Output pins) ⁽⁵⁾		$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{CS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-225	mA
I_O	Output Drive Current	$V_{CC} = \text{Max.}, V_O = 2.5\text{V}^{(3)}$		-50	—	-180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or V_{CC}		—	5	500	μA

2540 Ink 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16646T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -12\text{mA MIL.}$	2.4	3.5	—	V
			$I_{OH} = -15\text{mA COM'L.}$	—	—	—	—
			$I_{OH} = -24\text{mA MIL.}$ $I_{OH} = -32\text{mA COM'L.}^{(4)}$	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 48\text{mA MIL.}$ $I_{OL} = 64\text{mA COM'L.}$	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$		—	—	± 1	μA

2540 Ink 06

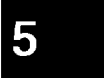
OUTPUT DRIVE CHARACTERISTICS FOR FCT162646T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		60	115	150	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		-60	-115	-150	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -16\text{mA MIL.}$	2.4	3.3	—	V
			$I_{OH} = -24\text{mA COM'L.}$	—	—	—	—
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16\text{mA MIL.}$	—	0.3	0.55	V
			$I_{OL} = 24\text{mA COM'L.}$	—	—	—	—

2540 Ink 07

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}, +25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current(4)	$V_{CC} = \text{Max.}$ Outputs Open $xDIR = xOE = GND$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	75	120	$\mu A/$ MHz
I_C	Total Power Supply Current(6)	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ (xCLKBA) 50% Duty Cycle $xDIR = xOE = GND$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ (xCLKBA) 50% Duty Cycle $xDIR = xOE = GND$ Sixteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	3.8	6.5(5)	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	8.3	20.0(5)	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current } (I_{CC1}, I_{CC2} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16646T/162646T				FCT16646AT/162646AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tpZH tpZL	Output Enable Time xDIR or xOE to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
tpHZ tpLZ	Output Disable Time xDIR or xOE to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
tsu	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

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Symbol	Parameter	Condition ⁽¹⁾	FCT16646CT/162646CT				FCT16646ET/162646ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	1.5	5.4	1.5	6.0	1.5	3.8	—	—	ns
tpZH tpZL	Output Enable Time xDIR or xOE to Bus		1.5	7.8	1.5	8.9	1.5	4.8	—	—	ns
tpHZ tpLZ	Output Disable Time xDIR or xOE to Bus		1.5	6.3	1.5	7.7	1.5	4.0	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		1.5	6.2	1.5	7.0	1.5	4.2	—	—	ns
tsu	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	—	—	ns
th	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	0.0	—	—	—	ns
tw	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	3.0 ⁽⁴⁾	—	—	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	—	ns

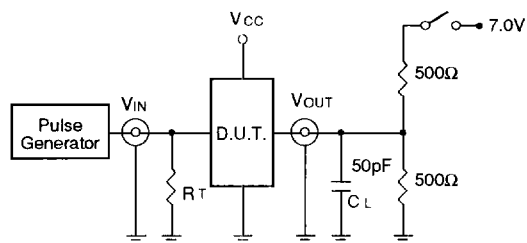
2540 IBI 0

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2556 drw 05

SWITCH POSITION

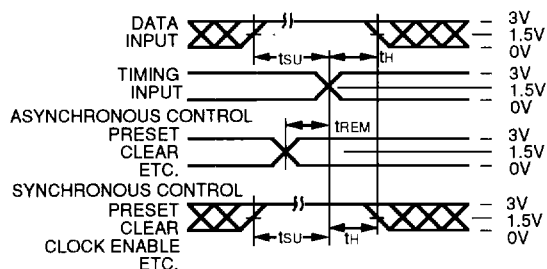
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to Zout of the Pulse Generator.

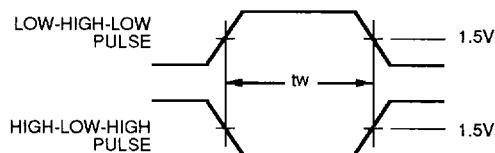
2556 Ink 10

SET-UP, HOLD AND RELEASE TIMES



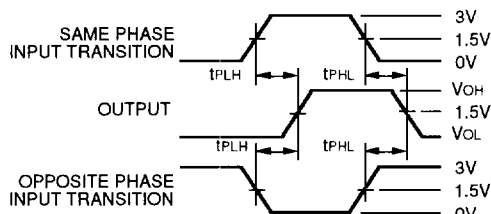
2556 drw 06

PULSE WIDTH



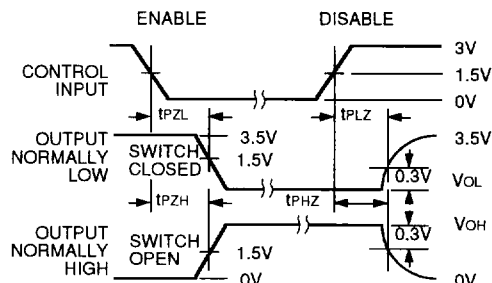
2556 drw 07

PROPAGATION DELAY



2556 drw 08

ENABLE AND DISABLE TIMES

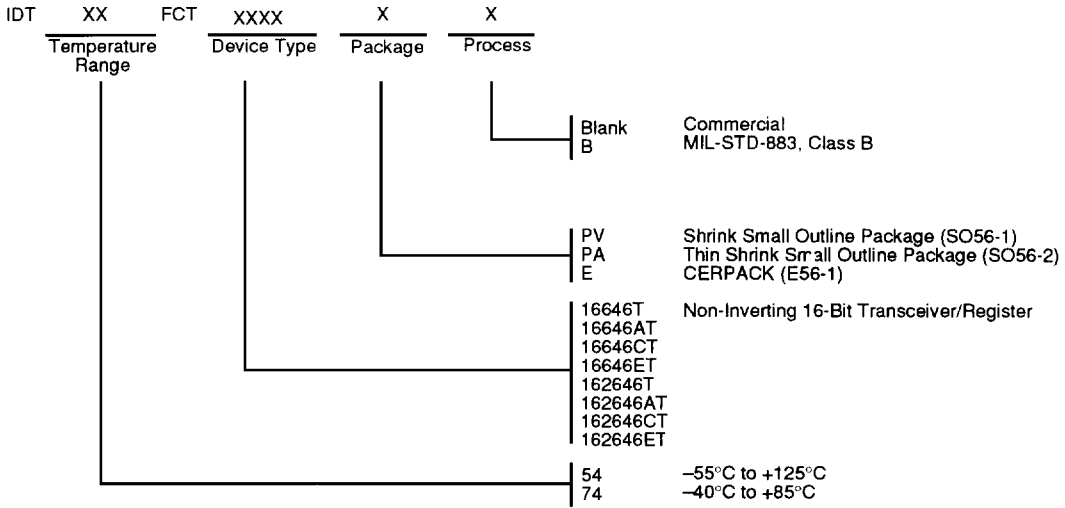


2556 drw 09

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



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