

# Octal D-type transparent latch (3-State)

# 74ABT573

### FEATURES

- 74ABT573 is broadside pinout version of 74ABT373
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State output buffers
- Common output enable
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Power-up reset

### DESCRIPTION

The 74ABT573 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT573 device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable (OE) control gates. The 74ABT573 is functionally identical to the 74ABT373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay Dn to Qn	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	4.2	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{V or } V_{CC}$	4	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0\text{V or } V_{CC}$	7	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	nA

### ORDERING INFORMATION

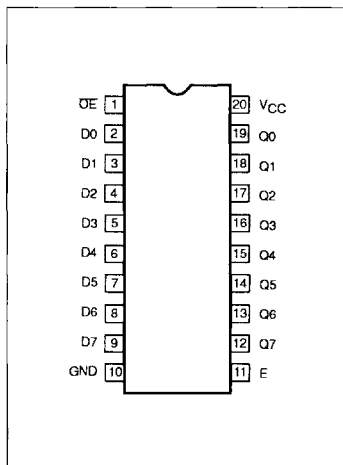
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	-40°C to +85°C	74ABT573N	0408B
20-pin plastic SOL	-40°C to +85°C	74ABT573D	0172D
20-pin plastic SSOP Type II	-40°C to +85°C	74ABT573D	1640A

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

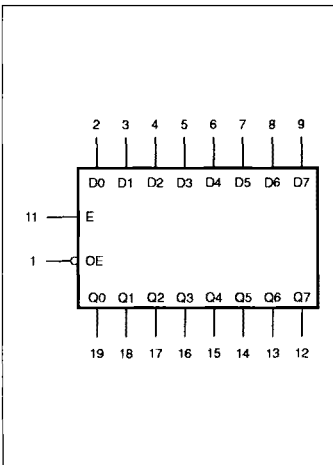
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable (OE) controls all eight 3-State buffers independent of the latch operation.

When OE is Low, the latched or transparent data appears at the outputs. When OE is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

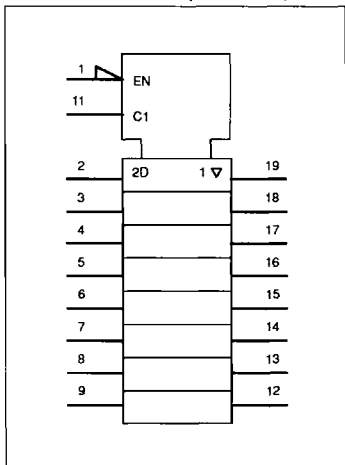
### PIN CONFIGURATION



### LOGIC SYMBOL



### LOGIC SYMBOL (IEEE/IEC)



# Octal D-type transparent latch (3-State)

74ABT573

## PIN DESCRIPTION

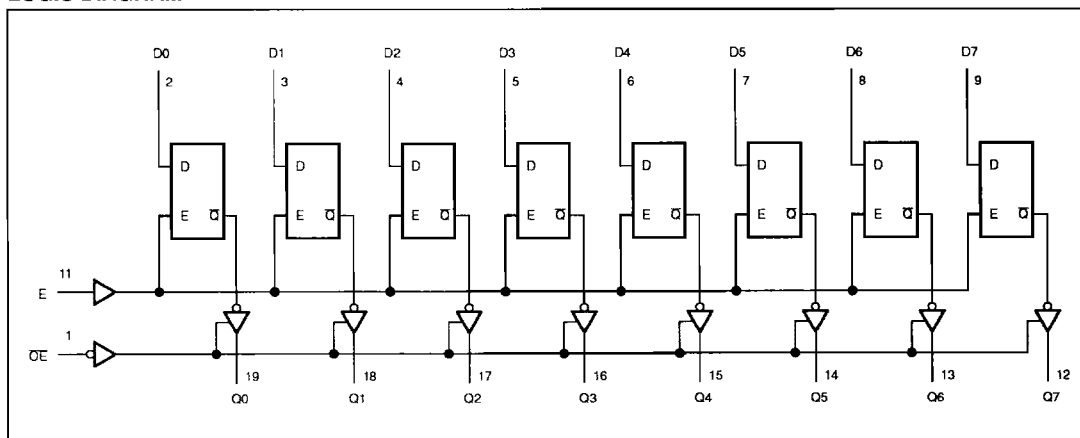
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive supply voltage

## FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D <sub>n</sub>	REGISTER	Q0 - Q7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X D <sub>n</sub>	NC D <sub>n</sub>	Z Z	Disable outputs

- H = High voltage level
- h = High voltage level one set-up time prior to the High-to-Low E transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the High-to-Low E transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- ↓ = High-to-Low E transition

## LOGIC DIAGRAM



## Octal D-type transparent latch (3-State)

74ABT573

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +7.0	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-18	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	output in Off or High state	-0.5 to +5.5	V
I <sub>OUT</sub>	DC output current	output in Low state	128	mA
T <sub>stg</sub>	Storage temperature range		-65 to 150	°C

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V <sub>CC</sub>	DC supply voltage	4.5	5.5	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage	2.0		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
I <sub>OH</sub>	High-level output current		-32	mA
I <sub>OL</sub>	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	5	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

## Octal D-type transparent latch (3-State)

74ABT573

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA		-0.9	-1.2		-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9		2.5		V
		V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.0	3.4		3.0		V
		V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.0	2.4		2.0		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.42	0.55		0.55	V
V <sub>RST</sub>	Power-up output low voltage <sup>3</sup>	V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>		0.13	0.55		0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V		±0.01	±1.0		±1.0	µA
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V		±5.0	±100		±100	µA
I <sub>PU</sub> /I <sub>PD</sub>	Power-up/down 3-State output current	V <sub>CC</sub> = 2.0V; V <sub>O</sub> = 0.5V; V <sub>OE</sub> = V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub>		±5.0	±50		±50	µA
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.7V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		5.0	50		50	µA
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		-5.0	-50		-50	µA
I <sub>CEx</sub>	Output High leakage current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		5.0	50		50	µA
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V	-50	-100	-180	-50	-180	mA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	50		50	µA
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>		24	30		30	mA
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	50		50	µA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND		0.5	1.5		1.5	mA

## NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

## AC CHARACTERISTICS

GND = 0V, t<sub>R</sub> = t<sub>F</sub> = 2.5ns, C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V			T <sub>amb</sub> = -40 to +85°C V <sub>CC</sub> = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dn to Qn	2	1.9	3.2	5.4	1.9	5.9	ns
			2.2	4.2	5.7	2.2	6.2	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay E to Qn	1	2.2	4.0	6.1	2.2	6.6	ns
			3.2	5.2	6.7	3.2	7.2	
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to High and Low level	4 5	1.2	3.2	4.7	1.2	5.2	ns
			2.7	4.7	6.2	2.7	6.7	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from High and Low level	4 5	2.5	4.9	6.4	2.5	6.9	ns
			2.0	4.2	6.0	2.0	6.5	

# Octal D-type transparent latch (3-State)

74ABT573

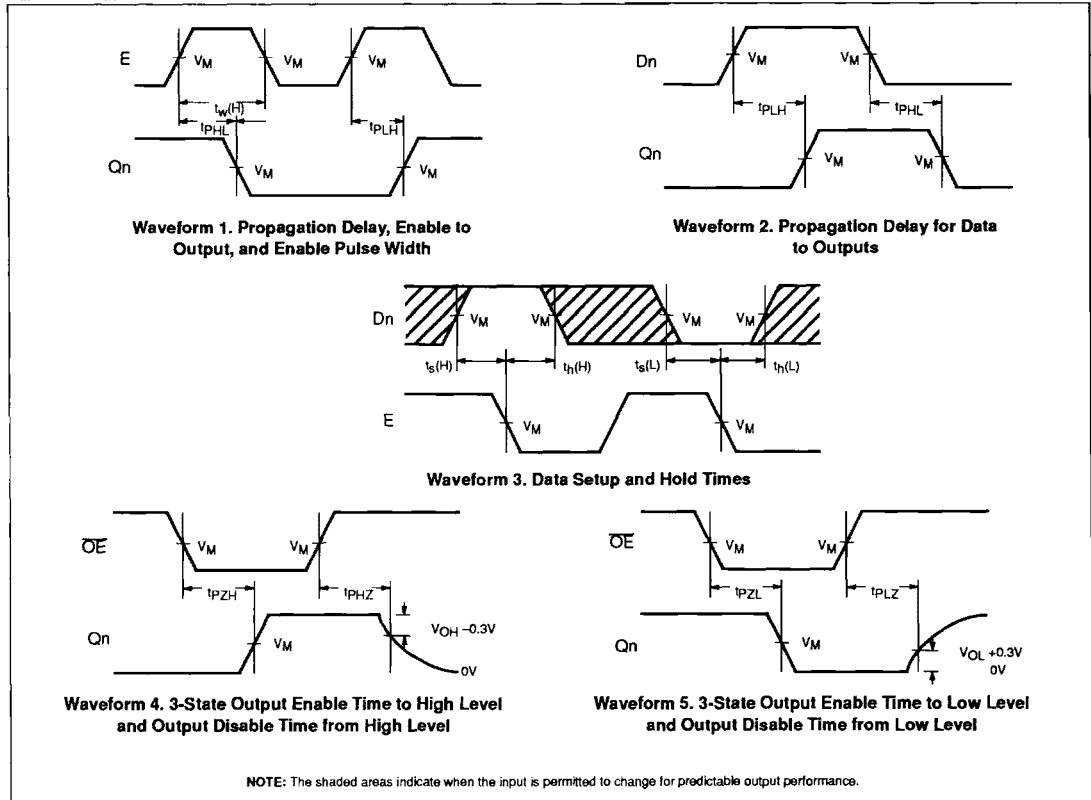
## AC SETUP REQUIREMENTS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_{amb} = -40$ to $+85^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 0.5\text{V}$	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to E	3	1.9 1.5	0.6 0.0	1.9 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to E	3	1.0 1.0	0.2 -0.3	1.0 1.0	ns
$t_w(H)$	E pulse width High	1	3.3	2.0	3.3	ns

## AC WAVEFORMS

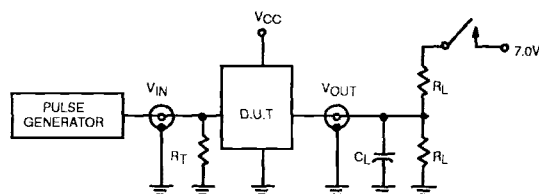
$V_M = 1.5\text{V}$ ,  $V_{IN} = \text{GND to } 3.0\text{V}$



# Octal D-type transparent latch (3-State)

74ABT573

## TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs

### SWITCH POSITION

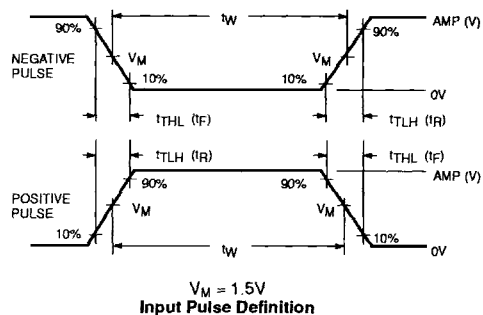
TEST	SWITCH
$t_{PLZ}$	closed
$t_{pZL}$	closed
All other	open

### DEFINITIONS

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



$V_M = 1.5V$   
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_w$	$t_R$	$t_F$
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns