



MC5404 • MC7404

2

ISSUE A

0A16

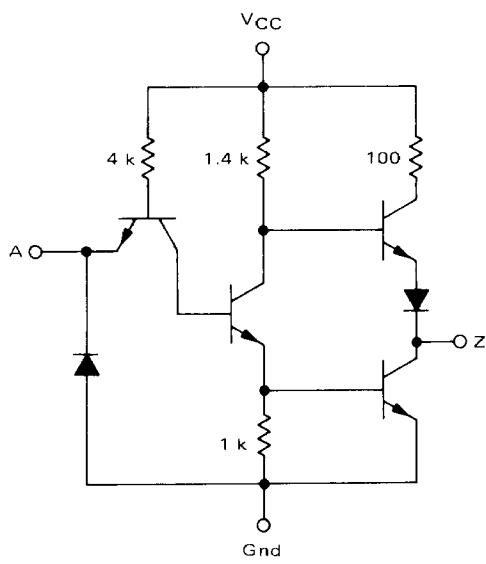
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MOT

Add Suffix F for TO-86 ceramic package (Case 607).
 Suffix L for TO-116 ceramic package (Case 632).
 Suffix P for TO-116 plastic package (Case 646) MC7404 only.

CIRCUIT SCHEMATIC
1/6 OF CIRCUIT SHOWN



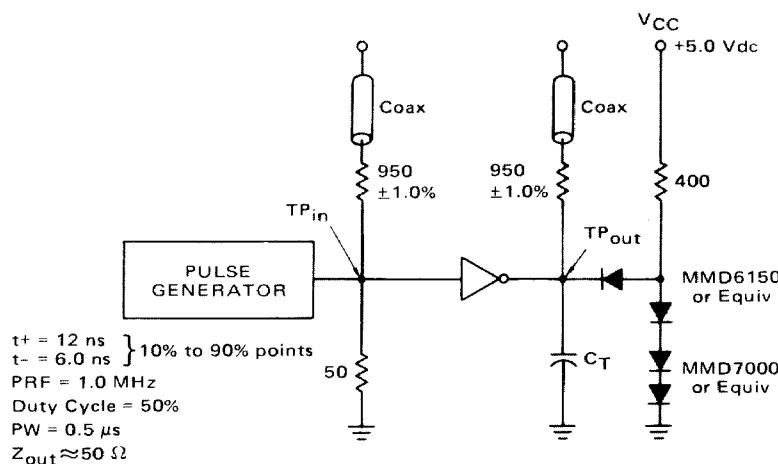
V_{CC} = Pin 14 [4]
 Gnd = Pin 7 [11]

[FLAT Pkg Pin]	DIL Pkg Pin
[1] 1	A → Z 2 [14]
[3] 3	→ 4 [2]
[5] 5	→ 6 [6]
[7] 9	→ 8 [8]
[9] 11	→ 10 [10]
[13] 13	→ 12 [12]

Positive Logic: $Z = \bar{A}$

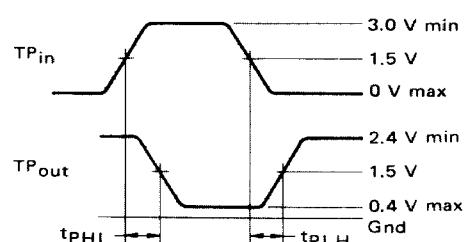
Input Loading Factor = 1
 Output Loading Factor = 10
 Total Power Dissipation = 60 mW typ/pkg
 Propagation Delay Time = 13 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



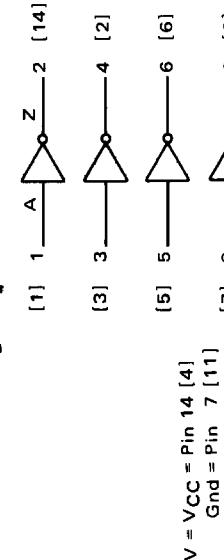
$C_T = 15 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

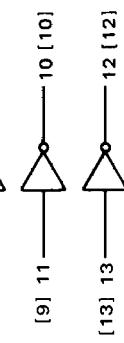


ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



V = V_{CC} = Pin 14 [4]
Gnd = Pin 7 [11]



TEST CURRENT/VOLTAGE VALUES (All Temperatures)

Characteristic	Pin Under Test	MC5404 Test Limits			MC7404 Test Limits			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
		Min	Max	Unit	Min	Max	Unit	I _O	I _{OH}	V _L	V _H	V _{IHH}	V _{R1}	V _{R2}	V _{th0}	V _{cc}	V _{CCCL}	V _{CCH}	Gnd	
Input Forward Current	I _F	A	-	-1.6	mAdc	-	-1.6	mAdc	-	A	-	-	-	-	-	-	-	-	V	*
Leakage Current	I _{R1}	A	-	40	μAdc	-	40	μAdc	-	-	A	-	-	-	-	-	-	-	V	*
	I _{R2}	A	-	1.0	mAdc	-	1.0	mAdc	-	-	A	-	-	-	-	-	-	-	V	*
Output Output Voltage	V _{OL}	Z	-	0.4	Vdc	-	0.4	Vdc	Z	-	-	-	-	A	-	-	V	-	*	
	V _{OH}	Z	2.4	-	Vdc	2.4	-	Vdc	-	Z	-	-	-	-	A	-	V	-	*	
Short-Circuit Current	I _{OS} [†]	Z	-20	-55	mAdc	-18	-55	mAdc	-	-	-	-	-	-	-	-	-	V	A,Z*	
Power Requirements (Total Device)	I _{PDH}	V	-	33	mAdc	-	33	mAdc	-	-	-	-	-	All Inputs	-	-	V	-		
Switching Parameters	I _{PDL}	V	-	12	mAdc	-	12	mAdc	-	-	-	-	-	-	-	-	-	V	All Inputs	
Turn-On Delay	t _{PHL}	A,Z	-	15*	ns	-	15*	ns	A	Z	-	-	-	-	-	-	-	V	-	
Turn-Off Delay	t _{PLH}	A,Z	-	22**	ns	-	22**	ns	A	Z	-	-	-	-	-	-	-	V	-	

* Ground inputs to inverters not under test.

[†] Tested only at 25°C.
† Only one output should be shorted at a time.



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