



GUARANTEED LOW SKEW 3.3V CMOS CLOCK DRIVER/BUFFER

QS532806/A

FEATURES:

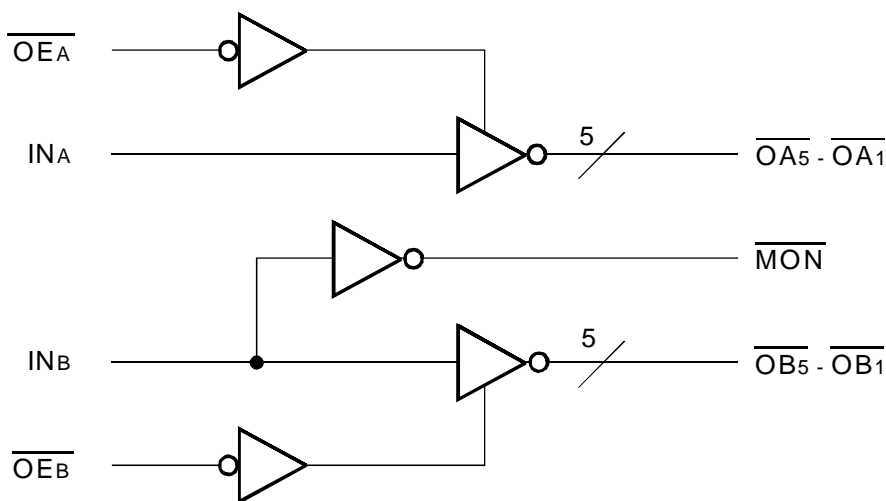
- JEDEC compatible LVTTTL level
- 10 low skew clock outputs
- Monitor output
- Clock inputs are 5V tolerant
- Pinout and function compatible with QS5806
- 25Ω on-chip resistors for low noise
- Input hysteresis for better noise margin
- Guaranteed low skew:
 - 0.7ns output skew (same bank)
 - 0.9ns output skew (different bank)
 - 1ns part-to-part skew
- Std. and A speed grades
- Available in QSOP and SOIC packages

DESCRIPTION

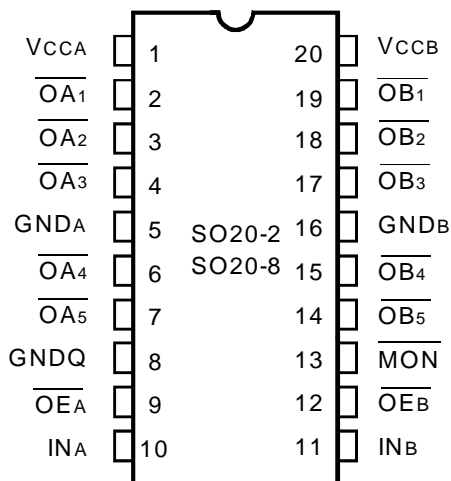
The QS532806 clock driver/buffer circuit can be used for clock buffering schemes where low skew is a key parameter. The QS532806 offers two banks of five inverting outputs. Designed in IDT's proprietary CMOS process, these devices provide low propagation delay buffering with on-chip skew of 0.7ns for same-transition, same-bank signals.

The QS532806 has on-chip series termination resistors for lower noise clock signals. The series resistor versions are recommended for driving unterminated lines with capacitive loading and other noise sensitive clock distribution circuits. These clock buffer products are designed for use in high-performance workstations, embedded and personal computing systems. Several devices can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP/ SOIC
 TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Supply Voltage to Ground	- 0.5 to +7	V
	DC Output Voltage V _{OUT}	- 0.5 to V _{CC} +0.5	V
V _{TERM} ⁽³⁾	DC Input Voltage V _{IN}	- 0.5 to +7	V
V _{AC}	AC Input Voltage (pulse width ≤20ns)	-3	V
I _{OUT}	DC Output Current V _{IN} < 0	-20	mA
	DC Output Current Max. Sink Current/Pin	120	mA
T _{STG}	Storage Temperature	- 65 to +150	°C
T _J	Junction Temperature	150	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} Terminals.
- All terminals except V_{CC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, V_{IN} = 0V, V_{OUT} = 0V)

Pins	QSOP		SOIC		Unit
	Typ.	Max. ⁽¹⁾	Typ.	Max. ⁽¹⁾	
All Pins	4	6	5	7	pF

NOTE:

- This parameter is guaranteed but not production tested.

PIN DESCRIPTION

Pin Names	I/O	Description
$\overline{OE}A$, $\overline{OE}B$	I	Output Enable Inputs
INA, INB	I	Clock Inputs
$\overline{OA}n$, $\overline{OB}n$	O	Clock Outputs
\overline{MON}	O	Monitor Outputs (non-disable)

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Inputs	2	—	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Inputs	-0.5	—	0.8	V
V_{IC}	Clamp Diode Voltage ⁽³⁾	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$	—	—	V
		$V_{CC} = \text{Min.}, I_{OH} = -8\text{mA}$	2.4	—	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 100\mu\text{A}$	—	—	0.2	V
		$V_{CC} = \text{Min.}, I_{OL} = 6\text{mA}$	—	—	0.4	V
		$V_{CC} = \text{Min.}, I_{OL} = 8\text{mA}$	—	—	0.5	V
I_{IN}	Input Leakage Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$ or GND	—	—	± 1	μA
I_{OZ}	Output Leakage Current	$V_{CC} = \text{Max.}, V_{OUT} = V_{CC}$ or GND	—	—	± 1	μA
I_{OFF}	Input Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN} = V_{CC}$ or GND	—	—	± 1	μA
I_{ODH}	Output HIGH Current ⁽²⁾	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}$	-30	-100	-200	mA
I_{ODL}	Output LOW Current ⁽²⁾	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}$	30	100	200	mA
I_{OS}	Short Circuit Current ^(2,3)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}$	-60	—	—	mA
R_{OUT}	Output Resistance ⁽⁴⁾	$V_{CC} = \text{Min}$	—	28	—	Ω

NOTES:

1. Typical values are at $V_{CC} = 3.3\text{V}, T_A = 25^\circ\text{C}$.
2. Not more than one output should be used to test this high power condition. Duration is less than one second.
3. Guaranteed by design but not tested.
4. Output resistance represents the total output impedance of the logic device and includes added series termination resistance.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ. ⁽³⁾	Max.	Unit	
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or V_{CC}	0.01	100	μA	
ΔI_{CC}	Supply Current per Input HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3\text{V}$	0.1	30	μA	
I_{CCD}	Dynamic Power Supply Current per Output ⁽²⁾	$V_{CC} = \text{Max.}, \overline{OE\bar{A}} = \overline{OE\bar{B}} = \text{GND}$ Outputs Toggling at 50% duty cycle	65	100	$\mu\text{A}/\text{MHz}$	
I_C	Total Power Supply Current Examples ^(2,4)	$V_{CC} = \text{Max.},$ $\overline{OE\bar{A}} = \overline{OE\bar{B}} = \text{GND}$ 50% duty cycle, $f_i = 10\text{MHz}$ five outputs	$V_{IN} = \text{GND}$ or V_{CC}	3.5	5.2	mA
			$V_{IN} = \text{GND}$ or 3V	3.5	5.2	mA
		$V_{CC} = \text{Max.},$ $\overline{OE\bar{A}} = \overline{OE\bar{B}} = \text{GND}$ 50% duty cycle, $f_i = 2.5\text{MHz}$ All outputs toggling	$V_{IN} = \text{GND}$ or V_{CC}	1.8	2.9	mA
			$V_{IN} = \text{GND}$ or 3V	1.8	2.9	mA

NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Guaranteed by design but not tested. $C_L = 0\text{pF}$.
3. Typical values are for reference only. Conditions are $V_{CC} = 3.3\text{V}, T_A = 25^\circ\text{C}$.
4. $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_o)(N_o)$
where:
 D_H = Input Duty Cycle
 N_T = Number of TTL HIGH inputs at D_H (one or two)
 f_o = Output Frequency
 N_o = Number of outputs at f_o (five or ten)

SKEW CHARACTERISTICS OVER OPERATING RANGE

T_A = -40°C to +85°C, V_{CC} = 3.3V ± 0.3V

C_{LOAD} = 50pF (no resistor)

Symbol	Parameter ⁽¹⁾	QS532806		QS532806A		Unit
		Min.	Max.	Min.	Max.	
t _{SK(01)}	Skew between all outputs, same transition, same bank	—	0.7	—	0.7	ns
t _{SK(02)}	Skew between two outputs, same transition, different banks	—	0.9	—	0.9	ns
t _{SK(P)}	Pulse Skew; skew between opposite transitions of the same output (t _{PHL} - t _{PLH})	—	1.4	—	1.4	ns
t _{SK(T)}	Part-to-part skew ⁽²⁾	—	1.5	—	1	ns

NOTES:

1. This parameter is guaranteed but not production tested. Skew parameters apply to propagation delays only.
2. t_{SK(T)} only applies to devices of the same transition, part type, temperature, power supply voltage, loading package, and speed grade.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T_A = -40°C to +85°C, V_{CC} = 3.3V ± 0.3V

C_{LOAD} = 50pF (no resistor)

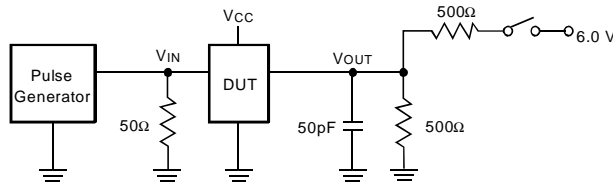
Symbol	Parameter ⁽¹⁾	QS53806		QS532806A		Unit
		Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay ⁽²⁾	1.5	6.5	1.5	5.8	ns
t _R	Output Rise Time, 0.8V to 2V ⁽³⁾	—	2	—	2	ns
t _F	Output Fall Time, 2V to 0.8V ⁽³⁾	—	2	—	2	ns
t _{PZL} t _{PZH}	Output Enable Time	1.5	8	1.5	8	ns
t _{PLZ} t _{PZH}	Output Disable Time	1.5	7	1.5	7	ns

NOTES:

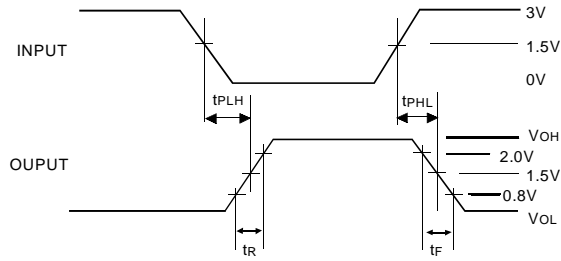
1. Minimums guaranteed but not production tested.
2. The propagation delay other range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delays do not imply limit skew.
3. This parameter is guaranteed but not production tested.

TEST CIRCUITS AND WAVEFORMS

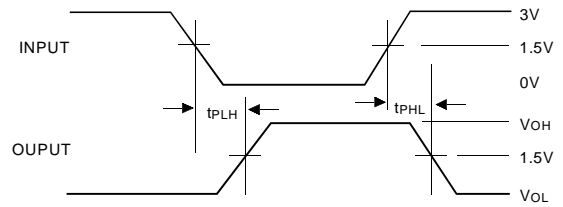
Parameter Tested	Switch Position
tPLZ, tPZL	Closed
All Others	Open



Pulse generator for all pulses: $f \leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

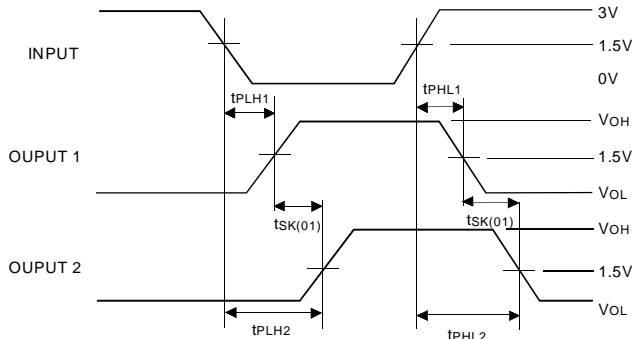


PROPAGATION DELAY



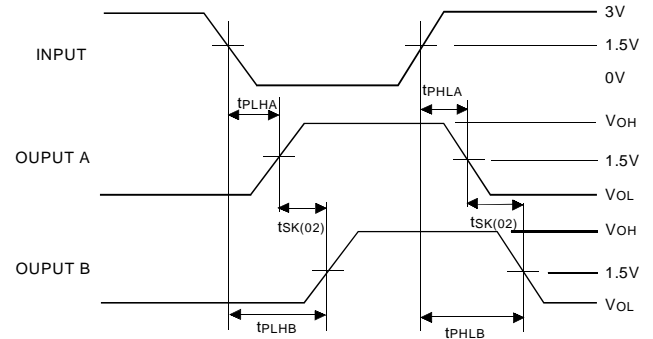
$$t_{SK(p)} = |t_{PHL} - t_{PLH}|$$

PULSE SKEW — tsk(p)



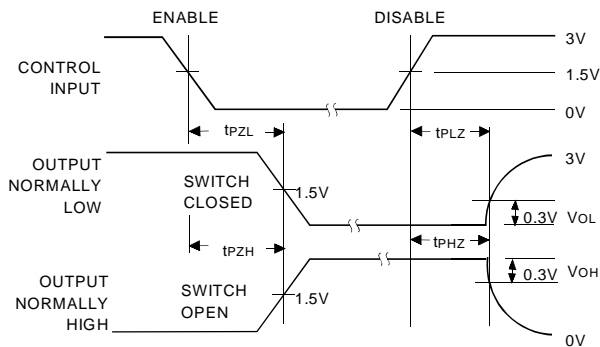
$$t_{SK(01)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

OUTPUT SKEW (SAME BANK) — tsk(01)

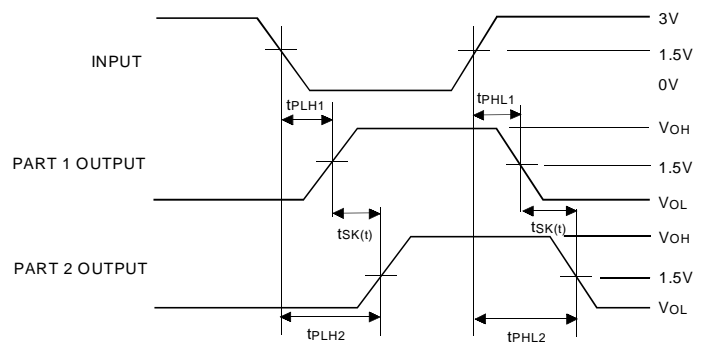


$$t_{SK(02)} = |t_{PLHB} - t_{PLHA}| \text{ or } |t_{PHLB} - t_{PHLA}|$$

OUPUT SKEW (DIFFERENT BANKS) — tsk(02)



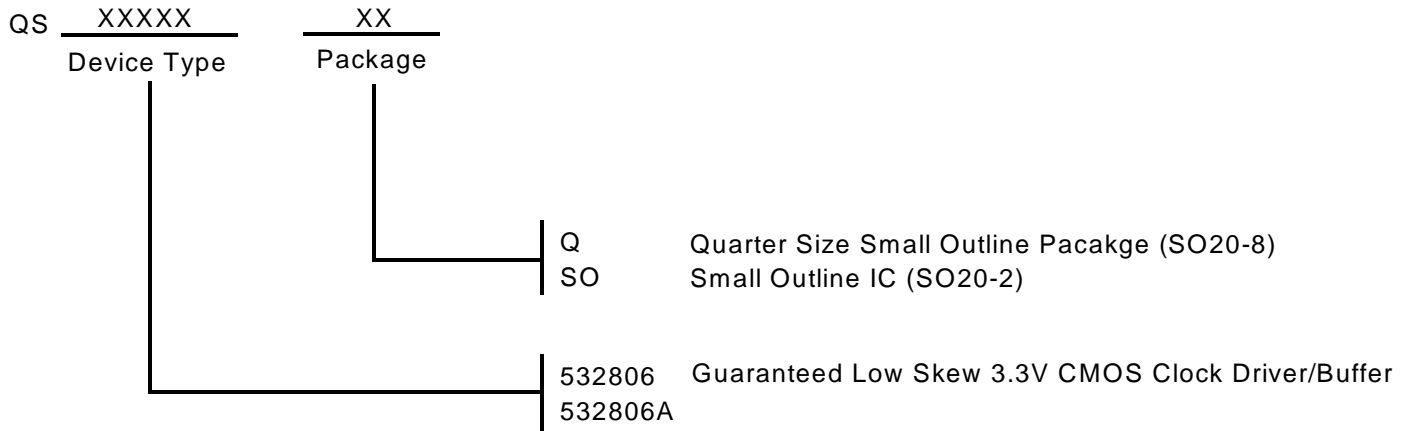
ENABLE AND DISABLE TIMES



$$t_{SK(i)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

PART-TO-PART SKEW — tsk(i)

ORDERING INFORMATION



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