

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

T-416-07-05

Octal 3-State Noninverting D Flip-Flop
High-Performance Silicon-Gate CMOS

The MC54/74HC574 is identical in pinout to the LS574. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

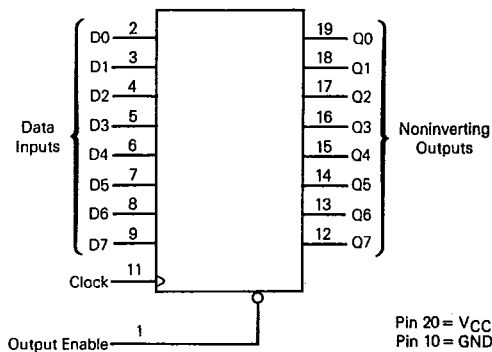
Data meeting the setup time is clocked to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, all device outputs are forced to the high-impedance state. Thus, data may be stored even when the outputs are not enabled.

The HC574 is identical in function to the HC374 but has the flip-flop inputs on the opposite side of the package from the outputs to facilitate PC board layout.

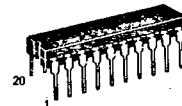
The HC574 is the noninverting version of the HC564.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 266 FETs or 66.5 Equivalent Gates

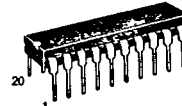
LOGIC DIAGRAM



MC54/74HC574



J SUFFIX
 CERAMIC
 CASE 732-03



N SUFFIX
 PLASTIC
 CASE 738-03



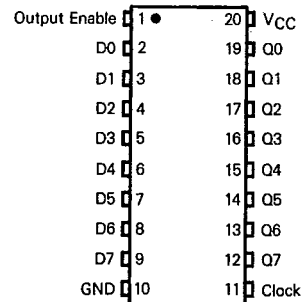
DW SUFFIX
 SOIC
 CASE 751D-03

ORDERING INFORMATION

- MC74HCXXXN Plastic
- MC54HCXXXJ Ceramic
- MC74HCXXXDW SOIC

T_A = -55° to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

Output Enable	Inputs		Output
	Clock	D	Q
L		H	H
L		L	L
L	L, H,	X	no change
H	X	X	Z

X = don't care
 Z = high impedance

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} =2.0 V V _{CC} =4.5 V V _{CC} =6.0 V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit			
				25°C to -55°C	≤85°C	≤125°C				
V _{IH}	Minimum High-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V			
			4.5	3.15	3.15	3.15				
			6.0	4.2	4.2	4.2				
V _{IL}	Maximum Low-Level Input Voltage	V _{out} =0.1 V or V _{CC} -0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V			
			4.5	0.9	0.9	0.9				
			6.0	1.2	1.2	1.2				
V _{OH}	Minimum High-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V			
			4.5	4.4	4.4	4.4				
			6.0	5.9	5.9	5.9				
V _{OL}	Maximum Low-Level Output Voltage	V _{in} =V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V			
			4.5	0.1	0.1	0.1				
			6.0	0.1	0.1	0.1				
I _{in}	Maximum Input Leakage Current	V _{in} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA			
			I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} =V _{IL} or V _{IH} V _{out} =V _{CC} or GND	6.0		±0.5	±5.0	±10.0
						6.0		±0.5	±5.0	±10.0
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} =V _{CC} or GND I _{out} =0 μA	6.0	8	80	160	μA			

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C_{in}	Maximum Input Capacitance	--	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	--	15	15	15	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, VCC=5.0 V		pF
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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r , t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

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SWITCHING WAVEFORMS

FIGURE 1

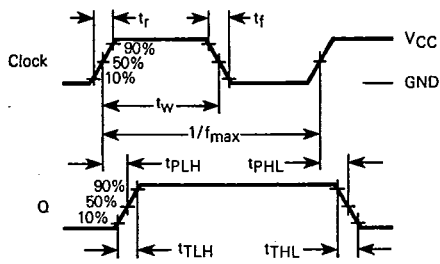


FIGURE 2

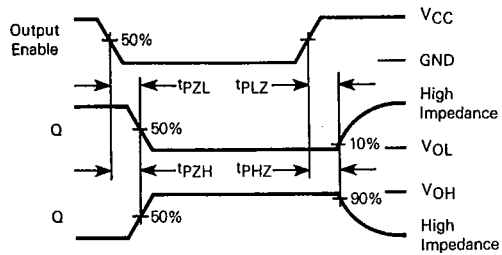


FIGURE 3

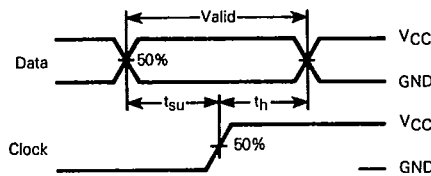
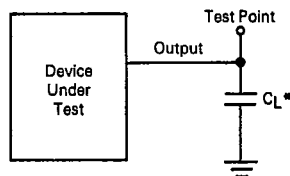
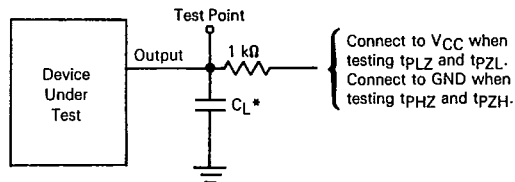


FIGURE 4 - TEST CIRCUIT



* Includes all probe and jig capacitance.

FIGURE 5 - TEST CIRCUIT



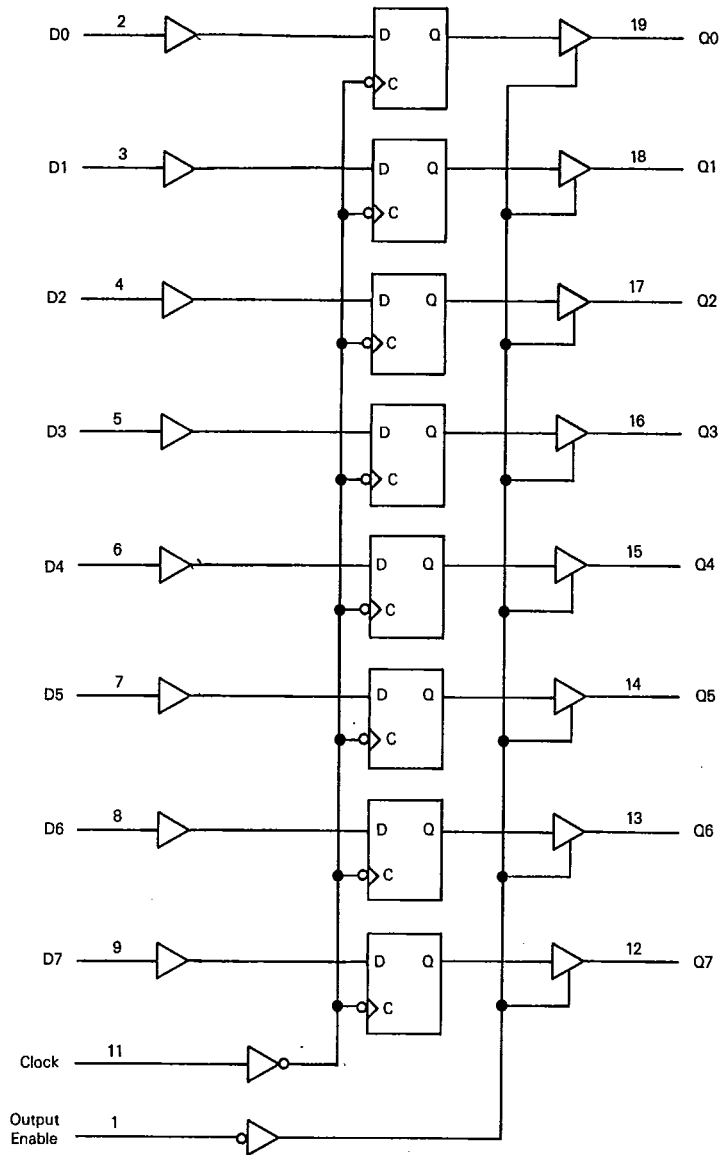
* Includes all probe and jig capacitance.

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EXPANDED LOGIC DIAGRAM



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