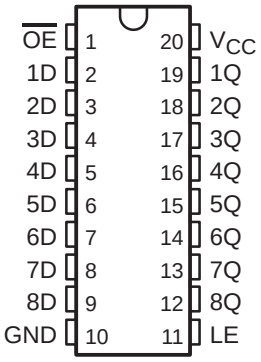
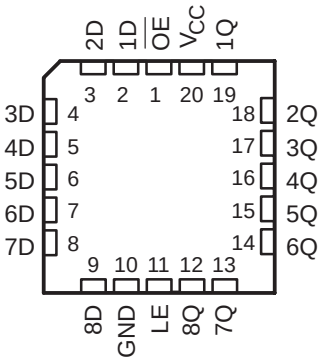
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Full Parallel Access for Loading**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Plastic and Ceramic 300-mil DIPs (J, N)**

SN54BCT573 . . . J OR W PACKAGE
SN74BCT573 . . . DW OR N PACKAGE
(TOP VIEW)



SN54BCT573 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ′BCT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs will be latched at the logic levels that were set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

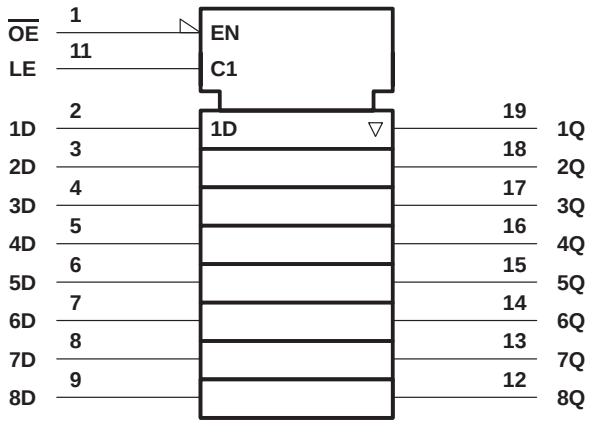
The output enable ($\overline{OE}$) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54BCT573 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74BCT573 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each latch)

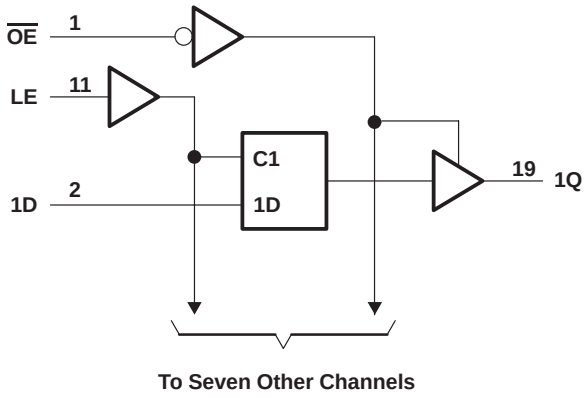
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . – 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . – 0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) . . . . . –30 mA
Current into any output in the low state, I_O: SN54BCT573 . . . . . 96 mA
SN74BCT573 . . . . . 128 mA
Operating free-air temperature range: SN54BCT573 . . . . . – 55°C to 125°C
SN74BCT573 . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		SN54BCT573			SN74BCT573			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT573			SN74BCT573			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = –12 mA	2	3.2					
		I_{OH} = –15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.4			0.4	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			–0.6			–0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	–100		–225	–100		–225	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			–50			–50	µA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open			62			62	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open			8			8	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open			8			8	mA
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		5.5			5.5		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		7.5			7.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V_{CC} = 5 V, T_A = 25°C		SN54BCT573		SN74BCT573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4		4		4		ns
t_{su}	Setup time, data before LE↓	1		2.5		1		ns
t_h	Hold time, data after LE↓	4		4		4		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54BCT573		SN74BCT573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	5	7.2	1	9.8	2	8.4	ns
t_{PHL}			2.8	5.9	8.2	1.5	10.3	2.8	9.6	
t_{PLH}	LE	Q	2.4	6.1	7.2	2	9.7	2.4	8.1	ns
t_{PHL}			2.9	5.2	7.1	2	8.8	2.9	7.8	
t_{PZH}	$\overline{OE}$	Q	3	6.2	8.5	2.5	11	3	10.4	ns
t_{PZL}			4.3	7.1	9.3	3.5	11.5	4.3	11	
t_{PHZ}	$\overline{OE}$	Q	2.2	3.9	5.6	1.5	7.2	2.2	6	ns
t_{PLZ}			1.7	3.6	5.2	1	7	1.7	6	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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SN74BCT573, Octal D-Type Transparent Latches

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54BCT573	SN74BCT573
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-15/64
No. of Outputs	8	8
Static Current		35
th (ns)		4
tpd max (ns)		9.6
tsu (ns)		1
Logic	True	True

FEATURES

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- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
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DESCRIPTION

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TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74bct573.pdf (73 KB,Rev.A) (Updated: 11/01/1991)

APPLICATION NOTES

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View Application Notes for Digital Logic

- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74BCT573DW	ACTIVE	SOP (DW) | 20	0 TO 70	View Contents	1KU | 1.40	25	N/A*	762 | 03 Oct	12 WKS			
								4839 | 04 Oct				
								>10k | 11 Oct				
SN74BCT573DWR	ACTIVE	SOP (DW) | 20	0 TO 70	View Contents	1KU | 1.43	2000	N/A*	601 | 25 Sep	12 WKS			
								4839 | 04 Oct				
								>10k | 11 Oct				
SN74BCT573N	ACTIVE	PDIP (N) | 20	0 TO 70	View Contents	1KU | 1.40	20	N/A*	3 | 23 Sep	12 WKS			
								2060 | 03 Oct				

								4839 | 07 Oct						
								>10k | 14 Oct						
								>10k | 21 Oct						
SN74BCT573NSR	ACTIVE	SOP (NS) | 20		View Contents	1KU | 1.40	2000	N/A*	>10k | 14 Oct	12 WKS					

Table Data Updated on: 9/26/2002