

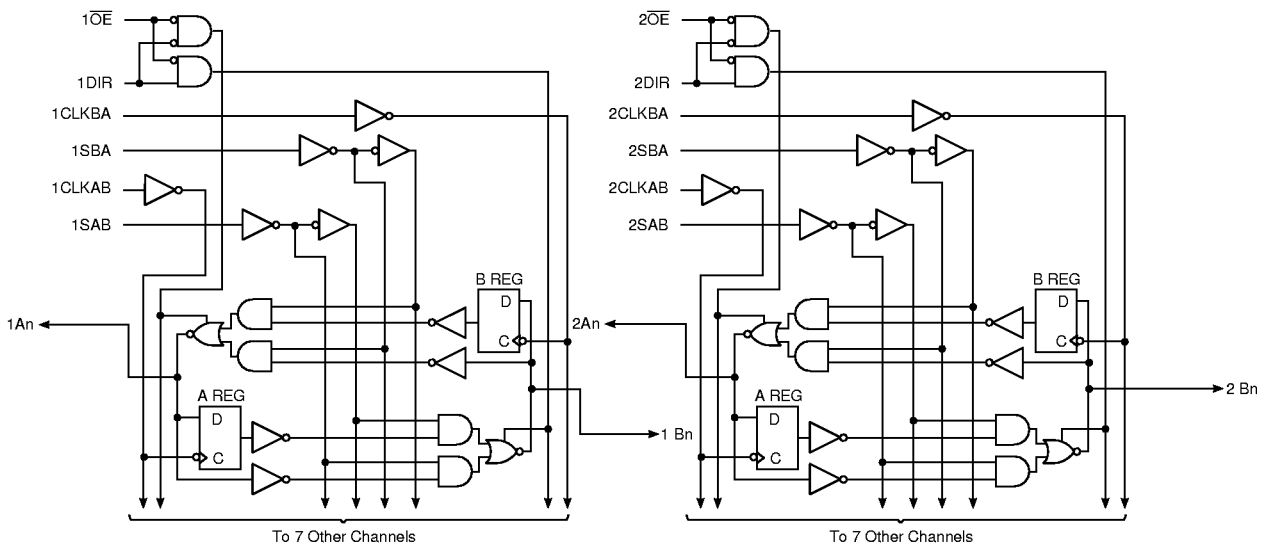
## FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- Bus Hold feature holds last active state during 3-state operation
- 10 $\mu$ A  $I_{CCQ}$  quiescent power supply current
- Hot insertable
- 2.0V–3.6V  $V_{CC}$  supply operation
- $\pm 24$ mA balanced output drive
- Power down high impedance inputs and outputs
- $t_{PD} = 5.7$ ns max.
- Input hysteresis for noise immunity
- Meets or exceeds JEDEC Standard 36 specifications
- Multiple power and ground pins for low noise
- Operating temperature range:  
 –40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:  
 Human body model > 2000V  
 Machine model > 200V
- Packages available:  
 56-pin TSSOP  
 56-pin SSOP

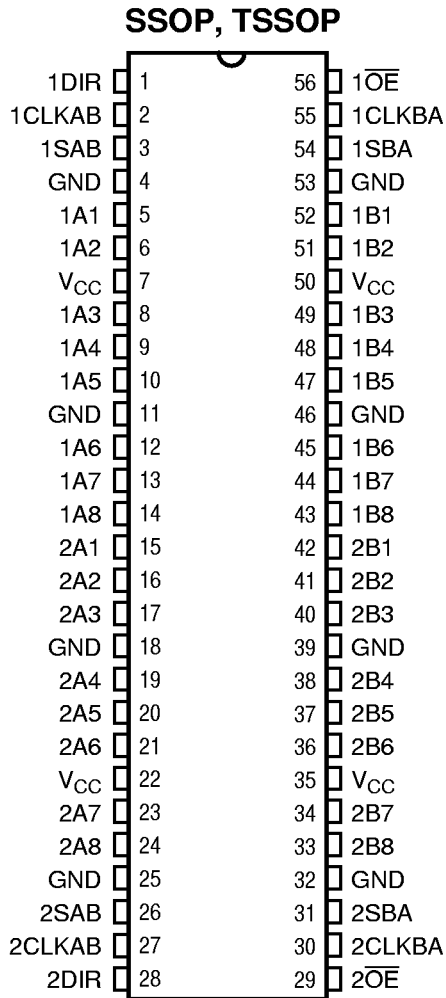
## DESCRIPTION

The LVCH16646A is a 16-bit bus registered transceiver with three-state outputs that is ideal for driving address and data buses. The LVCH16646A is organized for transmission of data between A bus and B bus either directly or from the internal storage registers. The QS74LVCH16646A provides Bus Hold circuitry on the data inputs to retain the last active state during 3-state operation, eliminating the need for external pull-up resistors. The 3.3V LVC family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end advanced workstation applications. 5V tolerant inputs and outputs allow this LVC product to be used in mixed 5V and 3.3V applications. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. To accommodate hot-plug or live insertion applications, this product is designed not to load an active bus when  $V_{CC}$  is removed. However, during power up or power down sequence,  $\overline{OE}$  should be tied to  $V_{CC}$  to ensure high-impedance state on the outputs.

**Figure 1. Functional Block Diagram**



**Figure 2. Pin Configuration**  
(All Pins Top View)



**Table 1. Pin Description**

Name	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Inputs
xSAB, xSBA	Output Source Select Inputs
xDIR, xOE	Output Enable Inputs

**Table 2. Function Table**

Inputs						Data I/O <sup>(1)</sup>		Operation or Function
xOE	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
H	X	H or L	H or L	x	x	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

**Notes:**

- The data output functions may be enabled or disabled by various signals at the xOE or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
↑ = LOW-to-HIGH Transition

**Table 3. Absolute Maximum Ratings**

Supply Voltage to Ground .....	-0.5V to 7.0V
DC Output Voltage $V_{OUT}$	
Outputs HIGH-Z .....	-0.5V to 7.0V
Outputs Active .....	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage $V_{IN}$ .....	-0.5V to 7.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-50mA
DC Output Diode Current	
$V_O < 0$ .....	-50mA
$V_O > V_{CC}$ .....	50mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ ) .....	$\pm 50mA$
DC Supply Current per Supply Pin .....	$\pm 100mA$
DC Ground Current per Ground Pin .....	$\pm 100mA$
$T_{STG}$ Storage Temperature .....	-65°C to 150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

**Table 4. Recommended Operating Conditions**

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	Supply Voltage, Operating	2.0	3.6	V	
	Supply Voltage, Data Retention Only	1.5	3.6		
$V_{IH}$	Input HIGH Voltage	$V_{OL} = 2.7$ to $3.6V$	2.0	—	V
$V_{IL}$	Input LOW Voltage	$V_{CC} = 2.7$ to $3.6V$	—	0.8	V
$V_{IN}$	Input Voltage	0	5.5	V	
$V_{OUT}$	Output Voltage in Active State	0	$V_{CC}$	V	
	Output Voltage in "OFF" State	0	5.5		
$I_{OH}$	Output Current HIGH	$V_{CC} = 3.0$ – $3.6V$	—	-24	mA
		$V_{CC} = 2.7V$		-12	
$I_{OL}$	Output Current LOW	$V_{CC} = 3.0$ – $3.6V$	—	24	mA
		$V_{CC} = 2.7V$	—	12	
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V	
$T_A$	Operating Free Air Temperature	-40	85	°C	

**Table 5. DC Electrical Characteristics Over Operating Range**

Industrial Temperature Range,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 2.7\text{V}, I_{OH} = -100\mu\text{A}$ $V_{CC} = 2.7\text{V}, I_{OH} = -12\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OH} = -12\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OH} = -24\text{mA}$	$V_{CC} - 0.2$ 2.2 2.4 2.2	— — — —	— — — —	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = 2.7\text{V}, I_{OL} = 100\mu\text{A}$ $V_{CC} = 2.7\text{V}, I_{OL} = 12\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OL} = 24\text{mA}$	— — —	— — —	0.2 0.4 0.55	V
$V_{IK}$	Input Clamp Voltage	$V_{CC} = 2.7\text{V}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
$I_I$	Input Leakage Current	$V_I = 0\text{V}, V_I = 5.5\text{V}, V_{CC} = 3.6\text{V}$	—	—	$\pm 1.0$	$\mu\text{A}$
$ I_{BH} $	Bus Hold Inputs Overdrive Current <sup>(2,3)</sup>	$V_{CC} = 3.6\text{V}, V_{IN} = 0\text{V}$ or $V_{IN} = V_{CC}$	—	—	50	$\mu\text{A}$
		$V_{CC} = 3.6\text{V}, 0.8\text{V} < V_{IN} < 2.0\text{V}$	—	—	500 <sup>(4)</sup>	
$I_{BHH}$ $I_{BHL}$	Bus Hold Input Sustaining Current	$V_{CC} = 3\text{V}$	$V_{IN} = 2.0\text{V}$	-75	—	$\mu\text{A}$
			$V_{IN} = 0.8\text{V}$	75	—	
$I_{OZ}$	High-Z I/O Leakage	$V_O = 0\text{V}, V_O = 5.5\text{V},$ $V_I = V_{IH}$ or $V_{IL}, V_{CC} = 3.6\text{V}$	—	—	$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	Power Off Leakage	$V_{CC} = 0\text{V}, V_I$ or $V_O = 5.5\text{V}$	—	—	10	$\mu\text{A}$
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}, V_{IN} = V_{CC}$ or GND	—	0.1	10	$\mu\text{A}$
$\Delta I_{CC}$	Quiescent Power Supply Current per Control Inputs at TTL HIGH	$V_{CC} = 3.6\text{V}, V_{IN} = V_{CC} - 0.6\text{V}^{(5)}$	—	2.0	3.0	$\mu\text{A}$
	Quiescent Power Supply Current per Bus Hold Inputs at TTL HIGH	$V_{CC} = 3.6\text{V}, V_{IN} = V_{CC} - 0.6\text{V}^{(5)}$	—	75	500	$\mu\text{A}$

**Notes:**

1. Typical values are at  $V_{CC} = 3.3\text{V}$  and  $T_A = 25^{\circ}\text{C}$ .
2. These parameters are guaranteed by characterization, but not production tested.
3. Pins with Bus Hold are identified in the pin description.
4. An external driver must provide at least  $|I_{BH}|$  during transition to guarantee that the Bus Hold input will change state.
5. Per TTL driven input. All other inputs at  $V_{CC}$  or GND.

**Table 6. Dynamic Switching Characteristics**

Symbol	Parameter	Test Conditions		Typ <sup>(1)</sup>	Unit
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50pF, V <sub>CC</sub> = 3.3V	V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	0.8	V
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 50pF, V <sub>CC</sub> = 3.3V	V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	0.8	V
C <sub>PD</sub>	Power Dissipation	C <sub>L</sub> = 50pF, f = 10MHz, V <sub>CC</sub> = 3.3 ±0.3V	Output Enable	35	pF
			Output Disable	6	

**Note:**

1. Typical values are at V<sub>CC</sub> = 3.3V, 25°C ambient.

**Table 7. Capacitance<sup>(1)</sup>**

Symbol	Pins	Conditions	Typ	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V, V <sub>OUT</sub> = 0V, f = 1MHz	7.0	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>IN</sub> = 0V, V <sub>OUT</sub> = 0V, f = 1MHz	8.0	pF

**Note:**

1. Capacitance is characterized but not production tested.

**Table 8. Switching Characteristics Over Operating Range**

Industrial Temperature Range, T<sub>A</sub> = -40°C to 85°C.

C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.

Symbol	Description <sup>(1)</sup>	V <sub>CC</sub> = 3.3 ±0.3V		V <sub>CC</sub> = 2.7V <sup>(2)</sup>		Unit
		Min	Max	Min	Max	
t <sub>MAX</sub>	Clock Pulse Frequency <sup>(2)</sup>	150	—	150	—	MHz
t <sub>PD</sub>	Propagation Delay xAX to xYx	2.0	5.7	2.0	6.8	ns
	Propogation Delay Clock to Bus	2.0	6.7	2.0	7.9	
	Propogation Delay xSAB or xSBA to Bus	2.0	7.7	2.0	9.2	
t <sub>EN</sub>	Output Enable Time xDIR or xOE to Bus	2.0	6.9	2.0	8.5	ns
t <sub>DIS</sub>	Output Disable Time <sup>(2)</sup> xDIR or xOE to Bus	2.0	6.9	2.0	7.7	ns
t <sub>SU</sub>	Setup Time HIGH or LOW Bus to Clock	2.9	—	3.2	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW Bus to Clock	0.3	—	0.0	—	ns
t <sub>W</sub>	Clock Pulse Width <sup>(2)</sup> LOW or HIGH	3.3	—	3.3	—	ns
t <sub>SK(O)</sub>	Output Skew <sup>(3)</sup>	—	0.5	—	—	ns

**Notes:**

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit

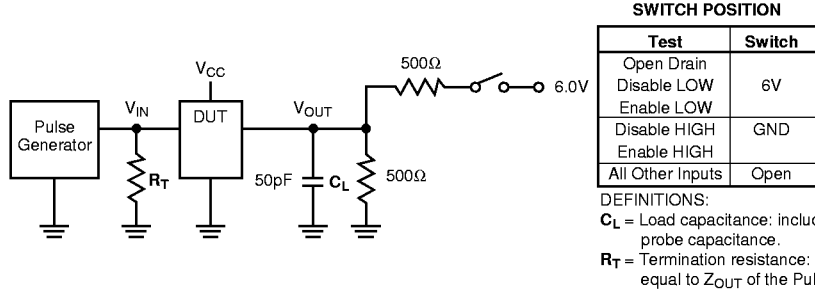


Figure 4. Setup, Hold, and Release Timing

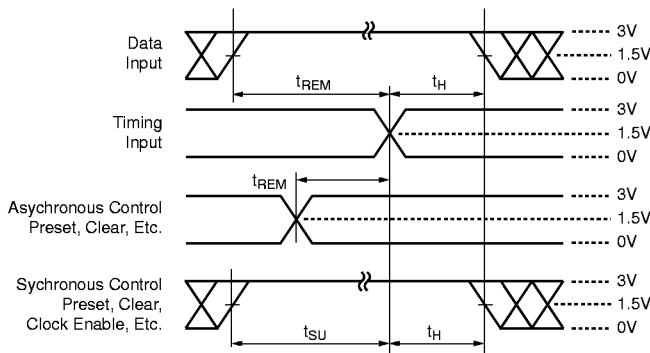


Figure 6. Pulse Width

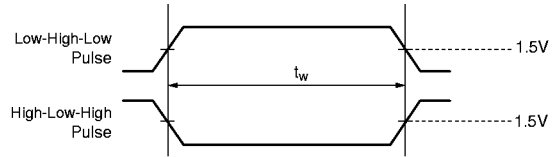


Figure 5. Enable and Disable Timing

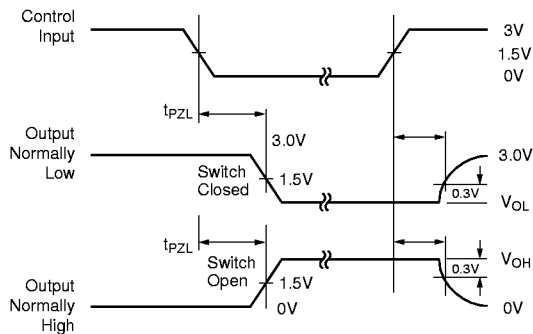
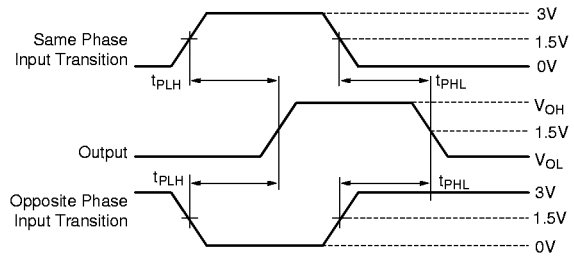


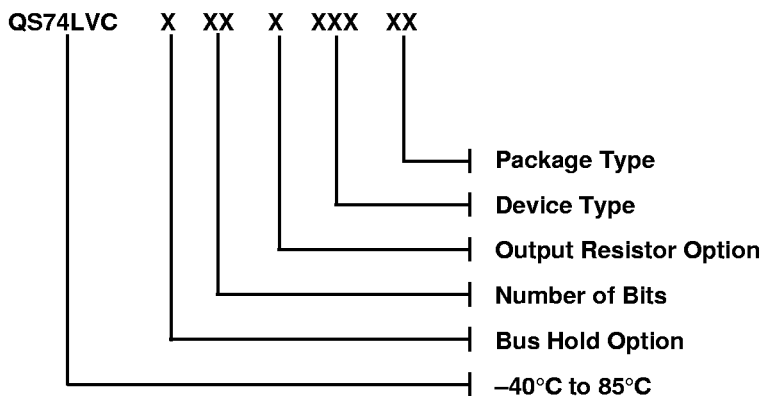
Figure 7. Propagation Delay



Notes:

1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  
 $Z_{OUT} \leq 50\Omega$ ;  $t_F, t_R \leq 2.5ns$ .

**ORDERING INFORMATION**



**Bus Hold Option:**  
H – with Bus Hold

**Number of Bits:**  
16 – 16-Bit

**Output Resistor Option:**  
Blank – No Output Resistor

**Device Type:**  
646

**Package Type:**  
PV – SSOP, 300 mil  
PA – TSSOP, 240 mil