CMOS Octal Latches

82C82
0408 39 82C83

Features/Benefits

- Full 8-bit parallel latching buffer
- Compatible with TTL bipolar 8282 and 8283
- Low power consumption
- Wide commercial operating supply and temperature ranges — 4.5 V to 5.5 V; -40°C to +85°C
- High output drive capability (I_{OL} = 32 mA)

57 ORIG
3129 003124 MMI

Description

The 82C82/82C83 Octal Latches are CMOS devices with three-state output buffers available in 20-pin packages. The three-state outputs are non-inverting on the 82C82 and inverting on the 82C83. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. Data is presented to the data output pins by activating the $\overline{OE}$ input line. High speed and industrial configuration make 82C82/82C83 compatible with 8086, 8088, 8089, 80186, and 80C86 microprocessors.

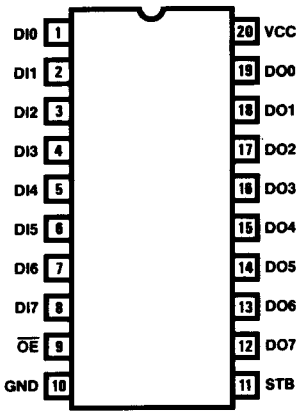
Ordering Information

PART NO.	PKG.	TEMP.	POLARITY	POWER
82C82C	N, J	Com	Non-invert	CMOS
82C82M	J*, W*, L	Mil		
82C83C	N, J	Com	Invert	CMOS
82C83M	J*, W*, L	Mil		

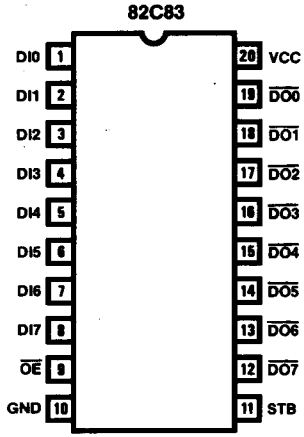
* Contact Factory

Pin Configurations

82C82

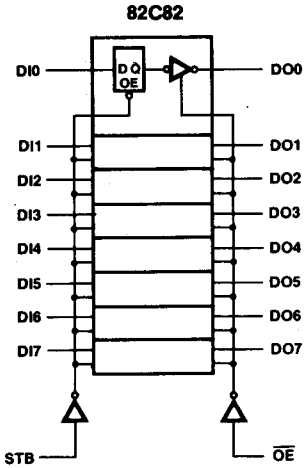


82C83

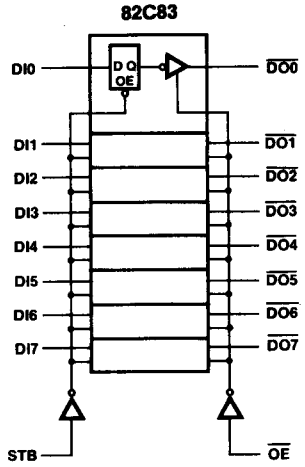


Functional Diagrams

82C82



82C83



TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories MMI

Absolute Maximum Ratings

Supply voltage ..... 8 V
Operating voltage ..... 4 V to 7 V
Input voltage ..... GND -2 V to 6.5 V
Output voltage ..... GND -0.5 to V_{CC} 0.5 V
Storage temperature ..... -65°C to +150°C
Maximum power dissipation ..... 1 W

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
T_A	Operating free-air temperature	-55		125	0		75	C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TESTING CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	LOW-level input voltage				0.8			0.8	V
V_{IH}	HIGH-level input voltage		2			2			V
I_{IL}	Input leakage current	$0 < V_{IN} < V_{CC}$	-1.0		1.0	-1.0		1.0	μA
V_{OH}	HIGH-level output voltage	I_{OH} = -8 mA, V_{CC} = min	3.8			3.8			V
V_{OL}	LOW-level output voltage	I_{OH} = 32 mA, V_{CC} = min			0.45			0.45	V
		I_{OH} = 8 mA, V_{CC} = min			0.40			0.40	
I_O	Output leakage current	$0V < V_O < V_{CC}$ OE = V_{CC} - 0.5 V	-10		10	-10		10	V
I_{CC}	Supply current	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open			10			10	μA
C_{IN}	Input capacitance	Freq. = 1 MHz T_A = 25°C V_{IN} = V_{CC} or GND		5			5		pF
C_{OUT}	Output capacitance			15			15		pF

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TESTING CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{IVOV}	Input to output delay	See note			35			35	ns
t_{SHOV}	STB to output delay				45			45	ns
t_{EHOZ}	Output disable time				35			35	ns
t_{ELOV}	Output enable time				50			50	ns
t_{IVSL}	Input to STB setup time		0			0			ns
t_{SLIX}	Input to STB hold time		25			25			ns
t_{SHSL}	STB high time		25			25			ns
t_{IRRF}	Input/output rise time/ fall time	Between 0.8 V to 2.0 V			20			20	ns

Note: See waveforms and test load circuit on next page.

Pin Names/82C82

DI0-DI7	Data Input Pins
DO0-DO7	Data Output Pins
STB	Active High Strobe Input
$\overline{OE}$	Active Low Output Enable

Pin Names/82C83

DI0-DI7	Data Input Pins
$\overline{DO0}$-$\overline{DO7}$	Iverted Data Output Pins
STB	Active High Strobe Input
$\overline{OE}$	Active Low Output Enable

Truth Table 82C82

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	L
H	L	H	H
↓	L	X	*

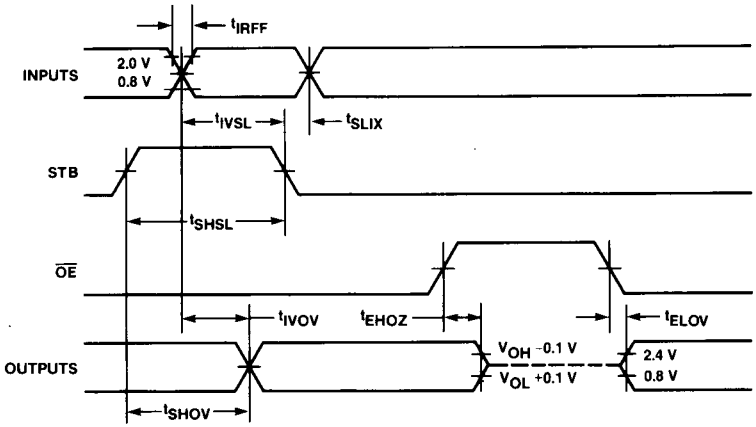
H = Logic one
L = Logic zero
X = Don't care

Truth Table 82C83

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	H
H	L	H	L
↓	L	X	*

Hi Z = High impedance
↓ = Negative transition
* = Latched to value of last data

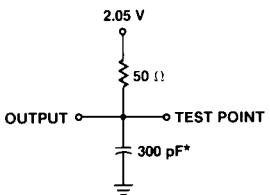
Waveforms



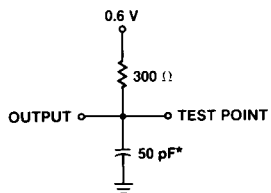
All timing measurements are made at 1.5 V unless otherwise noted.

Note: Input test signals must switch between V_{IL} - 0.4 V and V_{IH} + 0.4 V

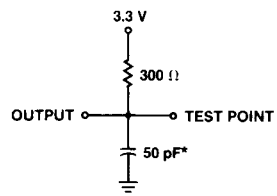
A.C. Test Circuit Specifications



TIVOV, TSHOV, TELOV
Load Circuits



TEHOZ
OUTPUT HIGH DISABLE
Load Circuit

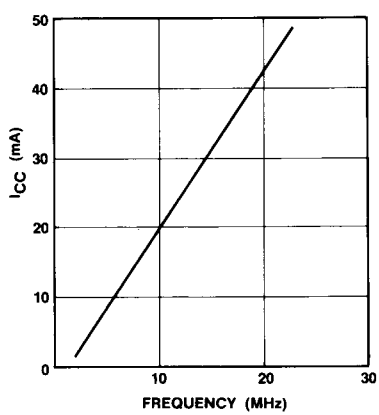


TEHOZ
OUTPUT LOW DISABLE
Load Circuit

* INCLUDES JIG AND STRAY CAPACITANCE

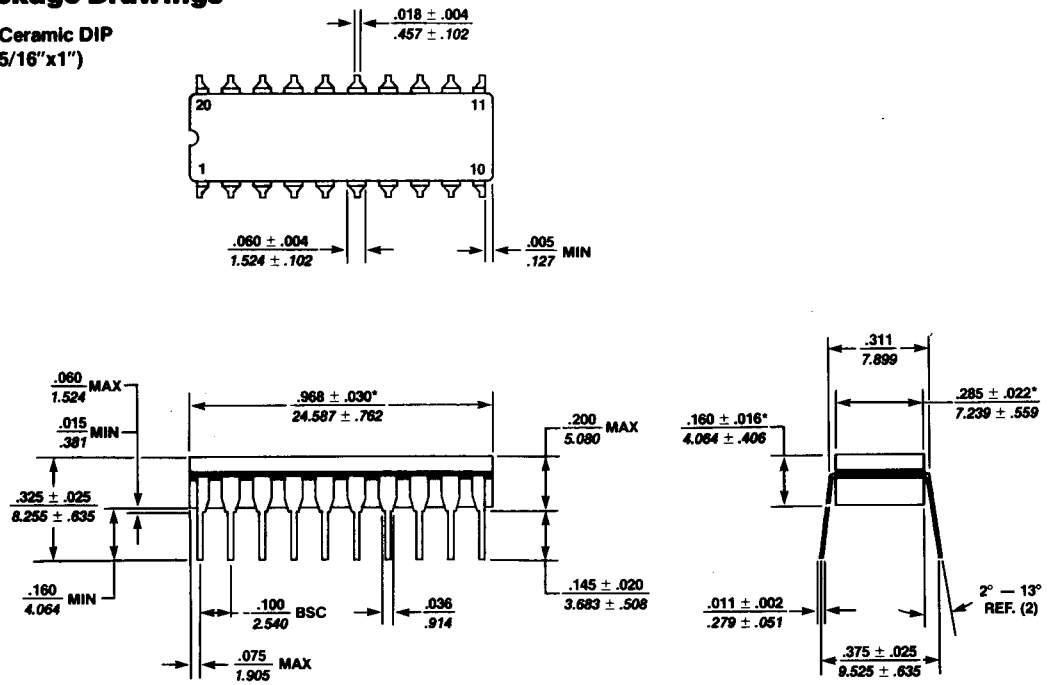
Typical ICC vs. Frequency

82C82/3

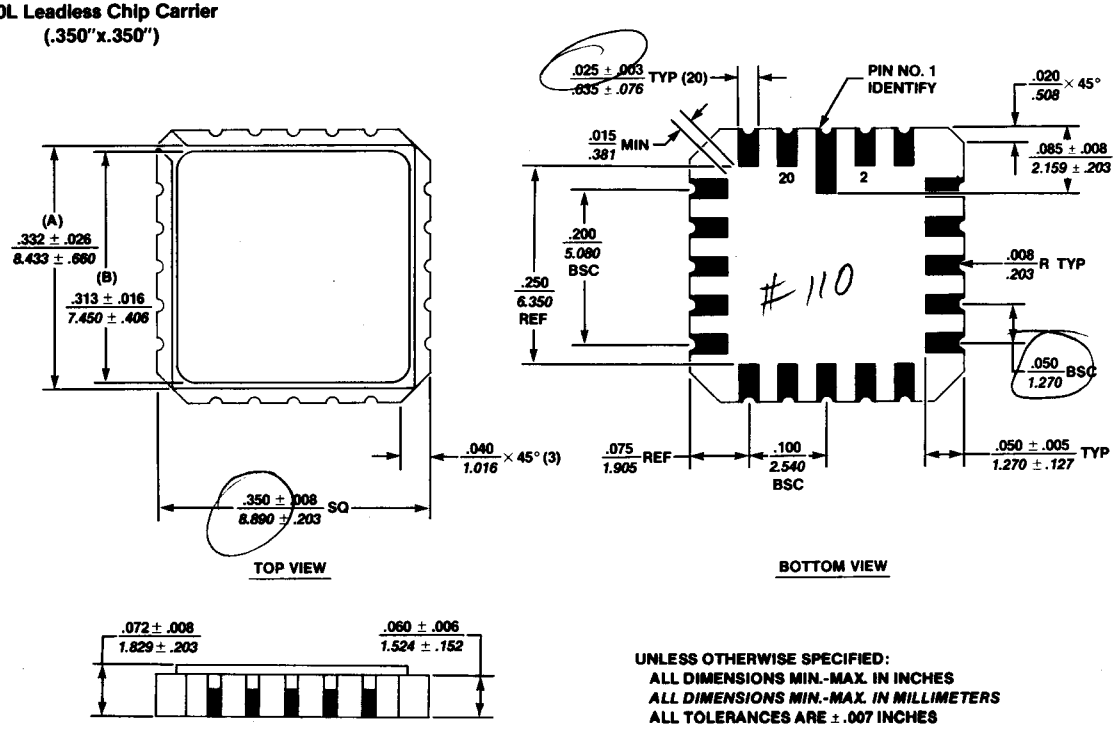


Package Drawings

20J Ceramic DIP (5/16"x1")



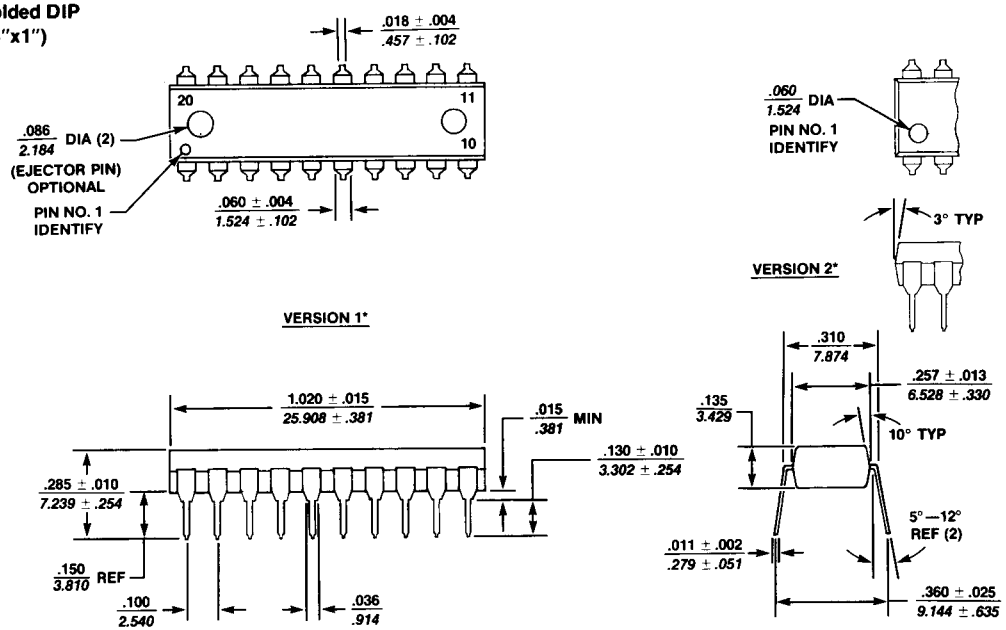
20L Leadless Chip Carrier (.350"x.350")



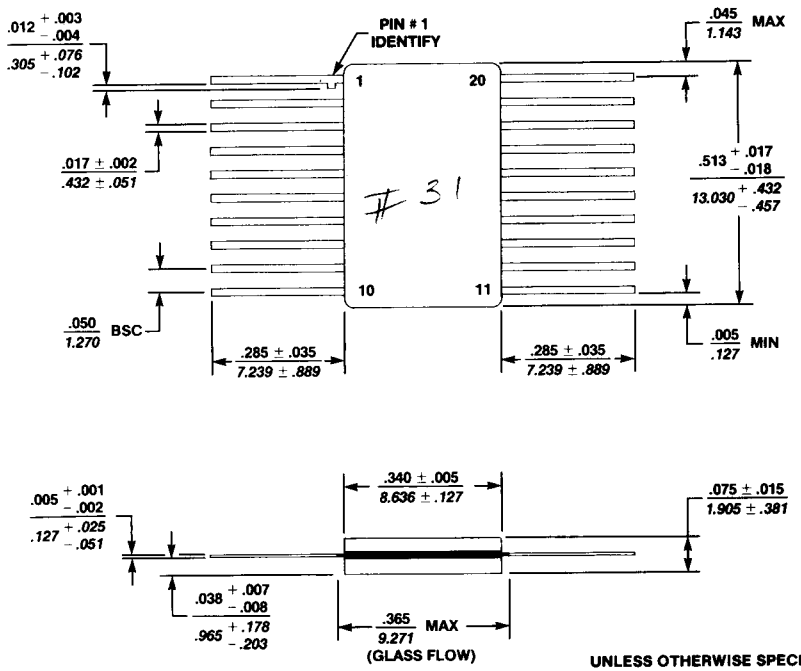
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Package Drawings

20N Molded DIP
(1/4"x1")



20W-3 Cerpack
(11/32"x17/32")



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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
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Monolithic MMI Memories

Americas
Monolithic Memories, Inc.
2175 Mission College Blvd.
Santa Clara, CA 95054-1592
Phone (408) 970-9700
TWX (910) 338-2374
TWX (910) 338-2376
Fax (408) 980-0675
Fax (408) 727-6549

France
Monolithic Memories France S.A.R.L.
Silic 463
F 94613 Rungis Cedex
France
Phone 1-6860818
Telex 202146
Fax 1-6876825

Japan
Monolithic Memories Japan KK
5-17-9 Shinjuku-Ku
Shinjuku
Tokyo 160
Japan
Phone 81-3-207-3131
Telex 232-3390 MMIKKJ
Fax 81-3-207-3130

United Kingdom
Monolithic Memories, Ltd.
Monolithic House
1 Queens Road
Farnborough, Hants
England GU146DJ
Phone 0252-517431
Telex 858051 MONO UKG
Fax (0252) 521041

Singapore
Monolithic Memories Singapore Pte., Ltd.
19 Kepple Road 11-06
Jit Poh Building
Singapore 0208
Phone 65-2257544
Telex RS55650 MMI RS
Fax 2246113

Germany
Monolithic Memories, GmbH
Mauerkircherstr 4
D 8000 Munich 80
West Germany
Phone 89-984961
Telex 524385
Fax 89-983162

Printed in U.S.A.

December 85