

# CMOS Octal Latches

82C82  
82C83

040839

## Features/Benefits

- Full 8-bit parallel latching buffer
- Compatible with TTL bipolar 8282 and 8283
- Low power consumption
- Wide commercial operating supply and temperature ranges — 4.5 V to 5.5 V; -40° C to +85° C
- High output drive capability ( $I_{OL} = 32 \text{ mA}$ )

57  
3124

003124

ORIC  
MMI

## Ordering Information

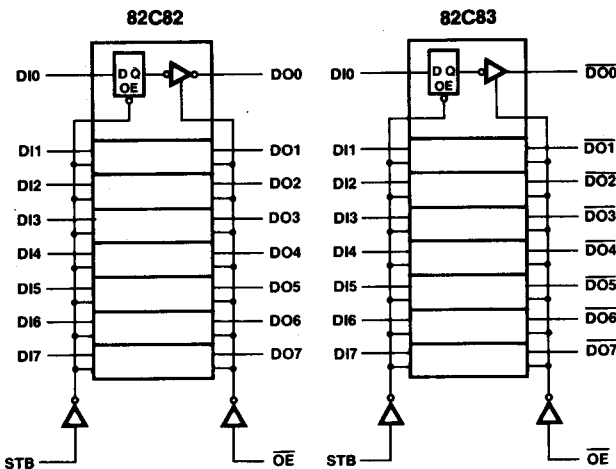
PART NO.	PKG.	TEMP.	POLARITY	POWER
82C82C	N, J	Com	Non-invert	CMOS
82C82M	J*, W*, L	Mil		
82C83C	N, J	Com	Invert	CMOS
82C83M	J*, W*, L	Mil		

\* Contact Factory

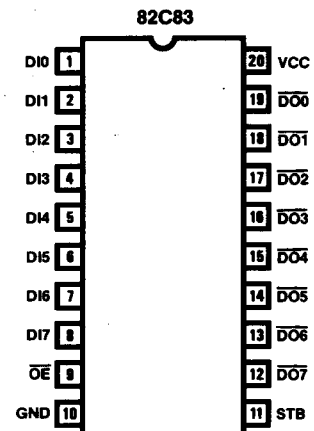
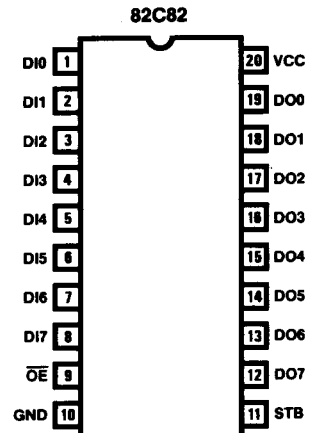
## Description

The 82C82/82C83 Octal Latches are CMOS devices with three-state output buffers available in 20-pin packages. The three-state outputs are non-inverting on the 82C82 and inverting on the 82C83. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. Data is presented to the data output pins by activating the  $\overline{OE}$  input line. High speed and industrial configuration make 82C82/82C83 compatible with 8086, 8088, 8089, 80186, and 80C86 microprocessors.

## Functional Diagrams



## Pin Configurations



**Absolute Maximum Ratings**

Supply voltage .....	8 V
Operating voltage .....	4 V to 7 V
Input voltage .....	GND -2 V to 6.5 V
Output voltage .....	GND -0.5 to V <sub>CC</sub> 0.5 V
Storage temperature .....	-65°C to +150°C
Maximum power dissipation .....	1 W

**Operating Conditions**

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
T <sub>A</sub>	Operating free-air temperature	-55		125	0		75	C

**Electrical Characteristics** Over Operating Conditions

SYMBOL	PARAMETER	TESTING CONDITIONS	MILITARY		COMMERCIAL		UNIT	
			MIN	TYP	MAX	MIN		TYP
V <sub>IL</sub>	LOW-level input voltage				0.8	0.8	V	
V <sub>IH</sub>	HIGH-level input voltage		2		2		V	
I <sub>IL</sub>	Input leakage current	0 < V <sub>IN</sub> < V <sub>CC</sub>	-1.0		1.0	-1.0	1.0	μA
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = -8 mA, V <sub>CC</sub> = min	3.8		3.8		V	
V <sub>OL</sub>	LOW-level output voltage	I <sub>OH</sub> = 32 mA, V <sub>CC</sub> = min			0.45		0.45	V
		I <sub>OH</sub> = 8 mA, V <sub>CC</sub> = min			0.40		0.40	
I <sub>O</sub>	Output leakage current	0V < V <sub>O</sub> < V <sub>CC</sub> OE = V <sub>CC</sub> - 0.5 V	-10		10	-10	10	V
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = V <sub>CC</sub> or GND Outputs open			10		10	μA
C <sub>IN</sub>	Input capacitance	Freq. = 1 MHz T <sub>A</sub> = 25°C V <sub>IN</sub> = V <sub>CC</sub> or GND		5		5		pF
C <sub>OUT</sub>	Output capacitance			15		15		pF

**Switching Characteristics** Over Operating Conditions

SYMBOL	PARAMETER	TESTING CONDITIONS	MILITARY		COMMERCIAL		UNIT	
			MIN	TYP	MAX	MIN		TYP
t <sub>IQOV</sub>	Input to output delay	See note			35		35	ns
t <sub>SHOV</sub>	STB to output delay				45		45	ns
t <sub>EHOZ</sub>	Output disable time				35		35	ns
t <sub>ELOV</sub>	Output enable time				50		50	ns
t <sub>IQSL</sub>	Input to STB setup time		0		0			ns
t <sub>SLIX</sub>	Input to STB hold time		25		25			ns
t <sub>SHSL</sub>	STB high time		25		25			ns
t <sub>IRRF</sub>	Input/output rise time/ fall time	Between 0.8 V to 2.0 V			20		20	ns

Note: See waveforms and test load circuit on next page.

**Pin Names/82C82**

DI0-DI7	Data Input Pins
DO0-DO7	Data Output Pins
STB	Active High Strobe Input
$\overline{OE}$	Active Low Output Enable

**Pin Names/82C83**

DI0-DI7	Data Input Pins
$\overline{DO0-DO7}$	Inverted Data Output Pins
STB	Active High Strobe Input
$\overline{OE}$	Active Low Output Enable

**Truth Table 82C82**

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	L
H	L	H	H
↓	L	X	*

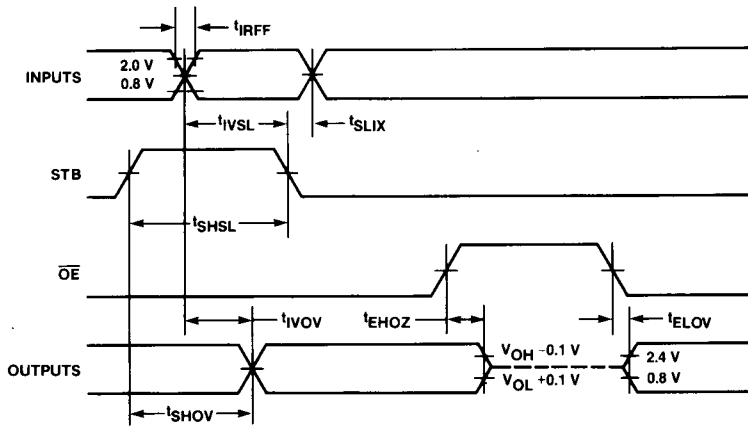
H = Logic one  
 L = Logic zero  
 X = Don't care

**Truth Table 82C83**

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	H
H	L	H	L
↓	L	X	*

Hi Z = High impedance  
 ↓ = Negative transition  
 \* = Latched to value of last data

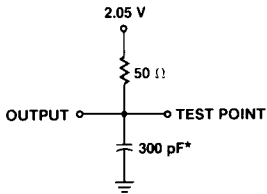
Waveforms



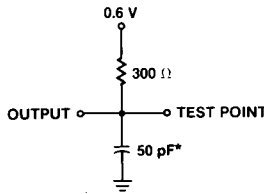
All timing measurements are made at 1.5 V unless otherwise noted.

Note: Input test signals must switch between  $V_{IL} - 0.4 V$  and  $V_{IH} + 0.4 V$

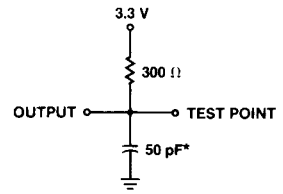
A.C. Test Circuit Specifications



TIVOV, TSHOV, TELOV  
Load Circuits



TEHOZ  
OUTPUT HIGH DISABLE  
Load Circuit

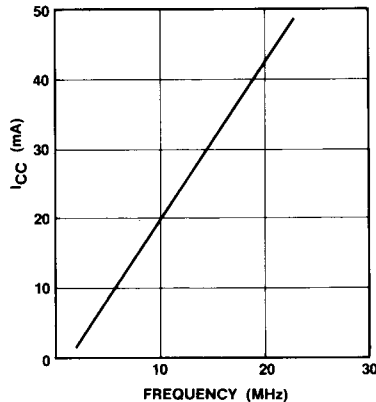


TEHOZ  
OUTPUT LOW DISABLE  
Load Circuit

\* INCLUDES JIG AND STRAY CAPACITANCE

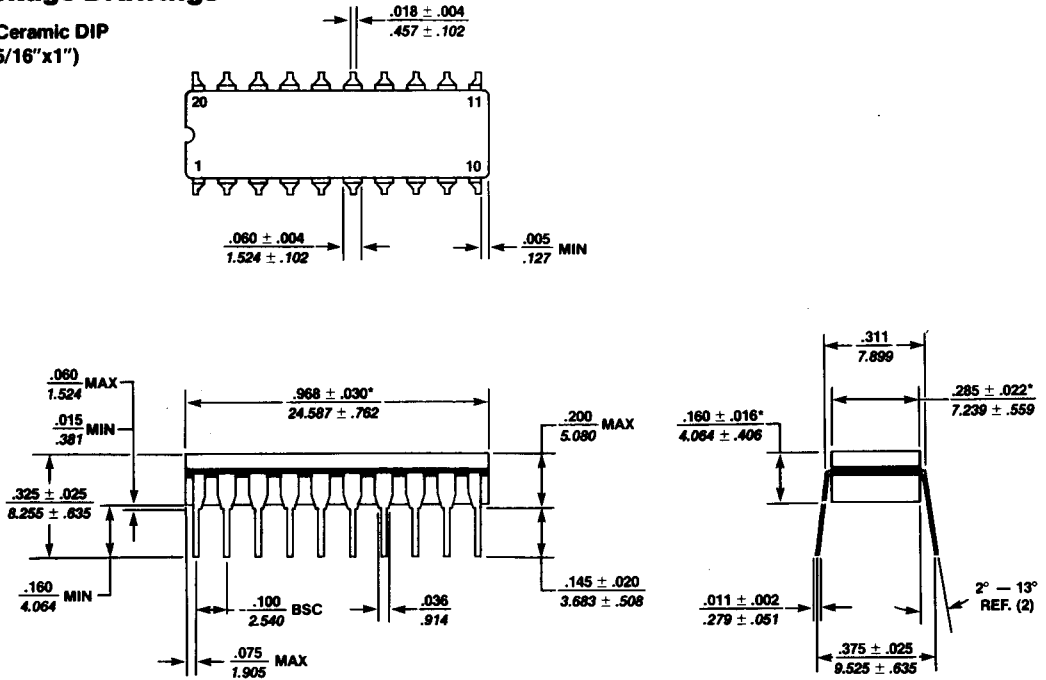
Typical  $I_{CC}$  vs. Frequency

82C82/3

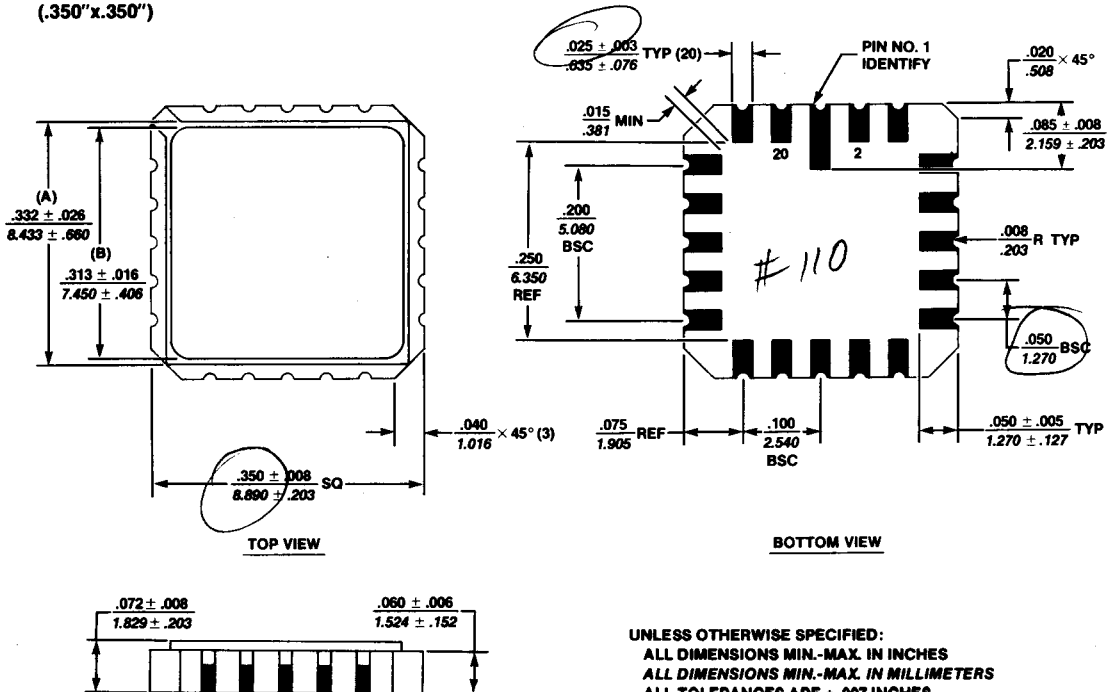


Package Drawings

20J Ceramic DIP  
(5/16"x1")



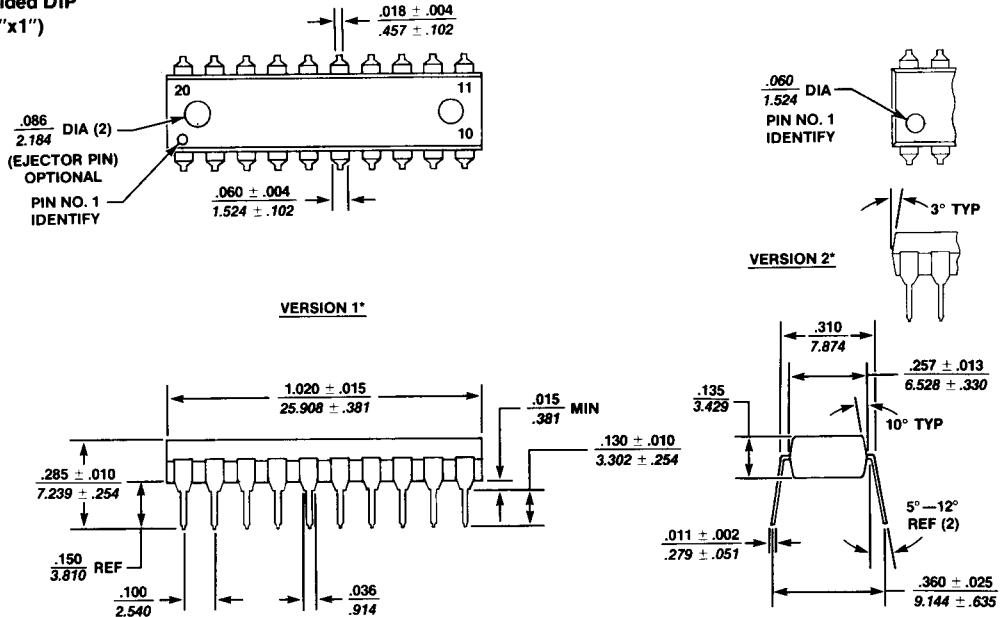
20L Leadless Chip Carrier  
(.350"x.350")



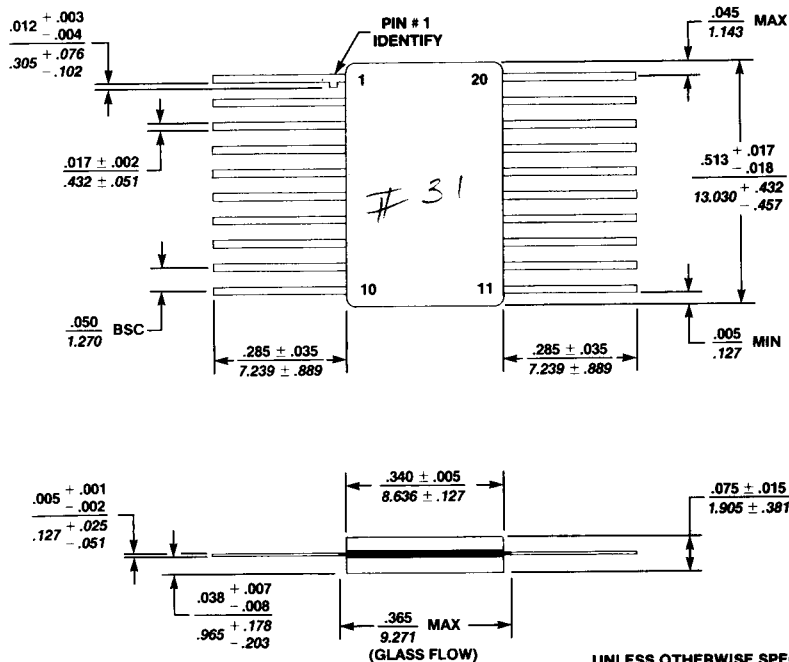
UNLESS OTHERWISE SPECIFIED:  
ALL DIMENSIONS MIN.-MAX. IN INCHES  
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS  
ALL TOLERANCES ARE ± .007 INCHES

Package Drawings

20N Molded DIP  
(1/4"x1")



20W-3 Cerpack  
(11/32"x17/32")



UNLESS OTHERWISE SPECIFIED:  
ALL DIMENSIONS MIN.-MAX. IN INCHES  
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS  
ALL TOLERANCES ARE  $\pm .007$  INCHES

# Monolithic Memories

## Americas

### **Monolithic Memories, Inc.**

2175 Mission College Blvd.  
Santa Clara, CA 95054-1592  
Phone (408) 970-9700  
TWX (910) 338-2374  
TWX (910) 338-2376  
Fax (408) 980-0675  
Fax (408) 727-6549

## United Kingdom

### **Monolithic Memories, Ltd.**

Monolithic House  
1 Queens Road  
Farnborough, Hants  
England GU146DJ  
Phone 0252-517431  
Telex 858051 MONO UKG  
Fax (0252) 521041

## France

### **Monolithic Memories France S.A.R.L.**

Silic 463  
F 94613 Rungis Cedex  
France  
Phone 1-6860818  
Telex 202146  
Fax 1-6876825

## Singapore

### **Monolithic Memories Singapore Pte., Ltd.**

19 Kepple Road 11-06  
Jit Poh Building  
Singapore 0208  
Phone 65-2257544  
Telex RS55650 MMI RS  
Fax 2246113

## Japan

### **Monolithic Memories Japan KK**

5-17-9 Shinjuku-Ku  
Shinjuku  
Tokyo 160  
Japan  
Phone 81-3-207-3131  
Telex 232-3390 MMIKKJ  
Fax 81-3-207-3130

## Germany

### **Monolithic Memories, GmbH**

Mauerkircherstr 4  
D 8000 Munich 80  
West Germany  
Phone 89-984961  
Telex 524385  
Fax 89-983162

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