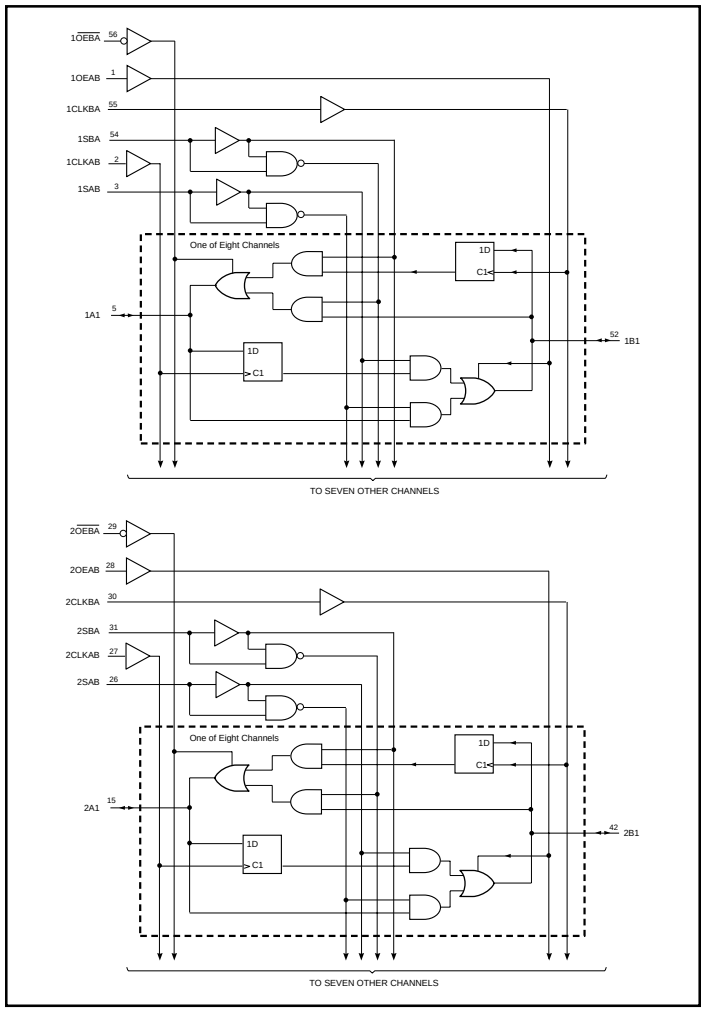
PI74AVC+16652

2.5V 16-Bit Bus Transceiver and Register with 3-State Outputs

Product Features

- PI74AVC+16652 is designed for low-voltage operation, V_{CC} = 1.65V to 3.6V
- True ±24mA Balanced Drive @ 3.3V
- I_{OFF} supports partial power-down operation
- 3.6V I/O Tolerant Inputs and Outputs
- All outputs contain a patented DDC (Dynamic DriveControl) circuit that reduces noise without degrading propagation delay.
- Industrial operation: –40°C to +85°C
- Available Packages:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 173 mil wide plastic TVSOP (K)

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74AVC+ series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading speed.

The PI74AVC+16652 is a 16-bit bus transceiver and register designed for low 1.65V to 3.6V V_{CC} operation. It consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary Output Enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. Select Control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Circuitry used for Select Control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

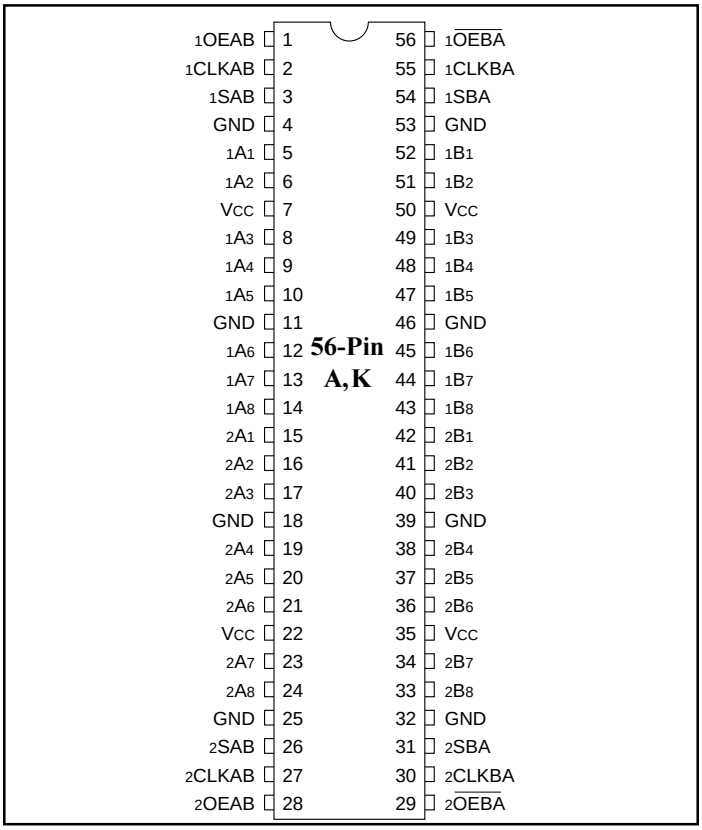
Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the Select Control or Output Enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-lops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are in the high-impedance state, each set of bus lines remains at its last level configuration.

To ensure the high-impedance state during power up or power down, $\overline{OEBA}$ should be tied to V_{CC} through a pull-up resistor and OEAB should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sinking current sourcing capability of the driver.

Product Pin Description

Pin Name	Description
OEAB	Output Enable Inputs (Active HIGH)
$\overline{\text{OEBA}}$	Output Enable Inputs (Active LOW)
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Select Control Inputs
xAx	Data Register A Inputs, Data Register B Outputs
xBx	Data Register B Inputs, Data Register A Outputs
GND	Ground
V_{CC}	Power

Pin Configuration



Truth Table[1]

Inputs						Data I/O*		Operation or Function
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1 - A8	B1 - B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	-	-	X	X	Input	Input	Store A and B data
X	H	-	H or L	X	X	Input	Unspecified**	Store A, hold B
H	H	-	-	X**	X	Input	Output	Store A in both registers
L	X	H or L	-	X	X	Unspecified**	Input	Hold A, store B
L	L	-	-	X	X**	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

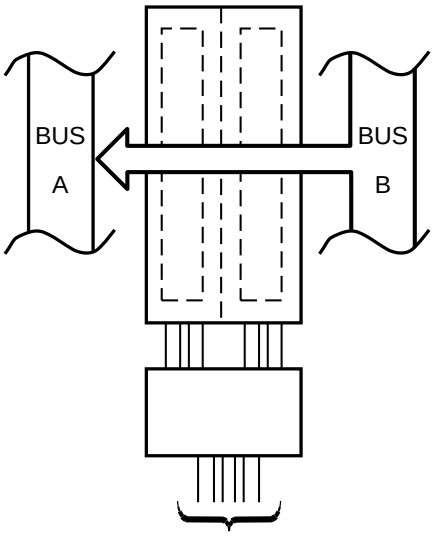
Notes:

1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, ↑ = LOW-to-HIGH Transition

* The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

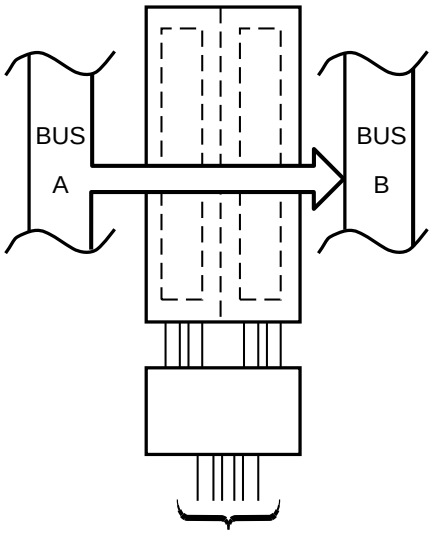
** Select control = L; clocks can occur simultaneously. Select control = H; to load both registers, clocks must be staggered.

REAL-TIME TRANSFER
BUS B to A



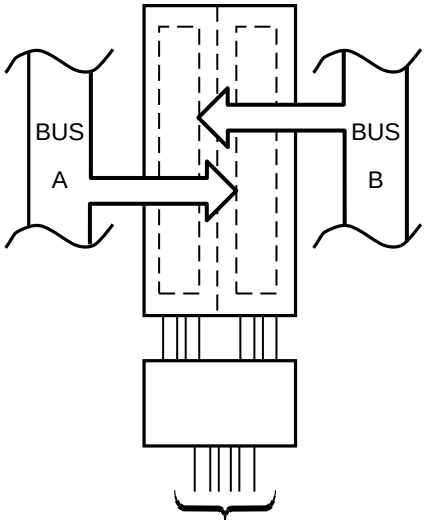
OEAB	$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS A to B



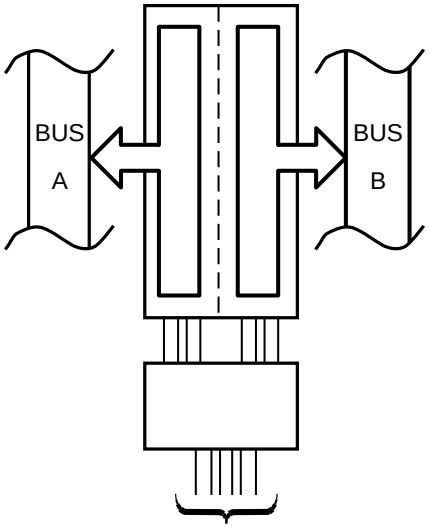
OEAB	$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

STORAGE FROM
A,B, or A and B



OEAB	$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED
DATA to A and/or B



OEAB	$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

Note:
1. Cannot transfer data to A bus and B bus simultaneously.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, V_{CC} ..... –0.5V to +4.6V
Input voltage range, V_I ..... –0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, V_O[1] ..... –0.5V to +4.6V
Voltage range applied to any output in the high or low state, V_O[1,2] ..... –0.5V to V_{CC} +0.5V
Input clamp current, I_{IK} (V_I <0) ..... –50mA
Output clamp current, I_{OK} (V_O <0) ..... –50mA
Continuous output current, I_O ..... ±50mA
Continuous current through each V_{CC} or GND ..... ±100mA
Package thermal impedance, q_{JA}[3]: package A ..... 64°C/W
package K ..... 48°C/W
Storage Temperature range, T_{stg} ..... –65°C to 150°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:
1. Input & output negative-voltage ratings may be exceeded if the input and output curent rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if theoutput current rating is observed.
3. package thermal impedance is calculated in accordance with JESD51.

Recommended Operating Conditions[1]

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
V_{IH} High-level Input Voltage	V_{CC} = 1.2V	V_{CC}		
	V_{CC} = 1.65V to 1.95V	0.65 x V_{CC}		
	V_{CC} = 2.3V to 2.7V	1.7		
	V_{CC} = 3V to 3.6V	2		
V_{IL} Low-level Input Voltage	V_{CC} = 1.2V		Gnd	
	V_{CC} = 1.65V to 1.95V		0.35 x V_{CC}	
	V_{CC} = 2.3V to 2.7V		0.7	
	V_{CC} = 3V to 3.6V		0.8	
V_I Input Voltage		0	3.6	
V_O Output Voltage	Active State	0	V_{CC}	
	3-State	0	3.6	
I_{OH} High-level output current	V_{CC} = 1.65V to 1.95V		– 6	mA
	V_{CC} = 2.3V to 2.7V		– 12	
	V_{CC} = 3V to 3.6V		– 24	
I_{OL} Low-level output current	V_{CC} = 1.65V to 1.95V		6	
	V_{CC} = 2.3V to 2.7V		12	
	V_{CC} = 3V to 3.6V		24	
$\Delta t\Delta v$ Input transition rise or fall rate	V_{CC} = 1.65V to 3.6V		5	ns/V
T_A Operating free-air temperature		–40	85	°C

Note:
1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

DC Electrical Characteristics (Over Operating Range, $T_A = –40°C$ to $+85°C$)

Parameters		Test Conditions[1]	V_{CC}	Min.	Max.	Units
V_{OH}		$I_{OH} = –100\mu A$	1.65V to 3.6V	$V_{CC} –0.2V$		V
		$I_{OH} = –6mA$ $V_{IH} = 1.07V$	1.65V	1.2		
		$I_{OH} = –12mA$ $V_{IH} = 1.7V$	2.3V	1.75		
		$I_{OH} = –24mA$ $V_{IH} = 2V$	3V	2.0		
V_{OL}		$I_{OL} = 100\mu A$	1.65V to 3.6V		0.2	
		$I_{OL} = 6mA$ $V_{IH} = 0.57V$	1.65V		0.45	
		$I_{OL} = 12mA$ $V_{IH} = 0.7V$	2.3V		0.55	
		$I_{OL} = 24mA$ $V_{IH} = 0.8V$	3V		0.8	
I_I	Control Inputs	$V_I = V_{CC}$ or GND	3.6V		±2.5	µA
I_{OFF}		V_I or $V_O = 3.6V$	0		±10	
I_{OZ}		$V_I = V_{CC}$ or GND	3.6V		±10	
I_{CC}		$V_O = V_{CC}$ or GND $I_O = 0$	3.6V		40	
C_I	Control Inputs	$V_I = V_{CC}$ or GND	2.5V		4	pF
			3.3V		4	
	Data Inputs		2.5V		6	
			3.3V		6	
C_O	Outputs	$V_O = V_{CC}$ or GND	2.5V		8	
			3.3V		8	

Note:
1. Typical values are measured at $T_A = 25°C$.

Timing Requirements

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

	V_{CC} = 1.2V		V_{CC} = 1.5V ±0.1V		V_{CC} = 1.8V ±0.15V		V_{CC} = 2.5V ±0.2V		V_{CC} = 3.3V ±0.3V		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{clock} Clock Frequency						150		250		350	MHz
t_w Pulse duration, CLKAB or CLKBA high or low					3.3		1.0		1.4		ns
t_{su} Setup time, A before CLKAB↑, or B before CLKBA↑	1.0		1.0		1.0		0.9		0.8		
t_h Hold time, A after CLKAB↑, or B after CLKBA↑	1.3		1.0		0.9		0.9		0.8		

Switching Characteristics

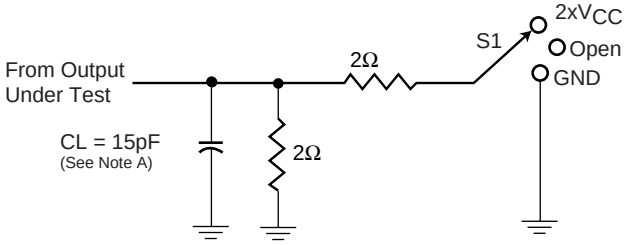
(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

Parameters	From (Input)	To (Output)	V_{CC} = 1.2V	V_{CC} = 1.5V ±0.1V		V_{CC} = 1.8V ±0.15V		V_{CC} = 2.5V ±0.2V		V_{CC} = 3.3V ±0.3V		Units
			Typical	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{max}						150		250		350		MHz
t_{pd}	A or B	B or A	5.0	1.9	4.2	1.5	3.6	1.2	3.2	0.9	2.6	ns
	CLKAB or CLKBA	A or B	5.5	2.0	4.0	1.9	3.8	1.3	3.5	1.0	3.2	
	SAB or SBA	B or A	4.8	2.4	4.1	2.0	4.0	1.7	3.8	1.4	3.1	
t_{en}	OE or $\overline{OE}$	A or B	4.5	1.8	3.6	1.5	3.5	1.4	3.0	1.0	2.5	
t_{dis}			5.5	2.0	4.0	1.8	4.0	1.4	3.7	1.1	3.2	

Operating Characteristics, T_A = 25°C

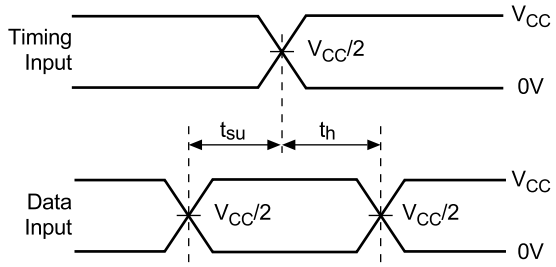
Parameters		Test Conditions	V_{CC} = 1.8V ±0.15V	V_{CC} = 2.5V ±0.2V	V_{CC} = 3.3V ±0.3V	Units
			Typical	Typical	Typical	
C_{pd} Power Dissipation Capacitance	Outputs Enabled	C_L = 0pF, f = 10 MHz	30	35	40	pF
	Outputs Disabled		12	15	20	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.2V and 1.5V ± 0.1V

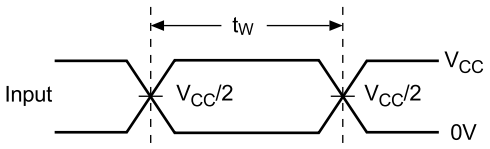


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

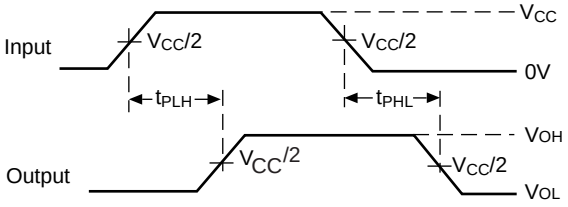
Load Circuit



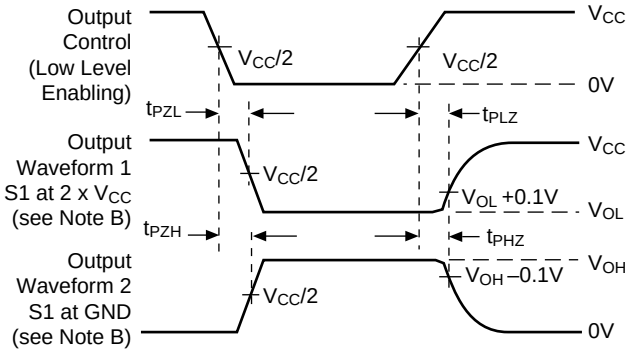
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



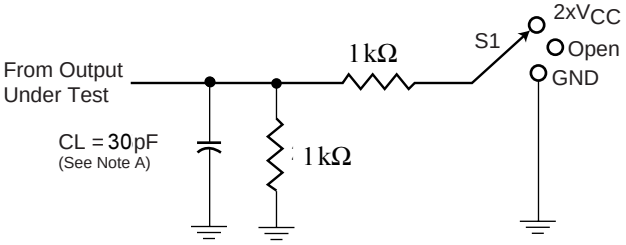
Voltage Waveforms
Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

Notes:

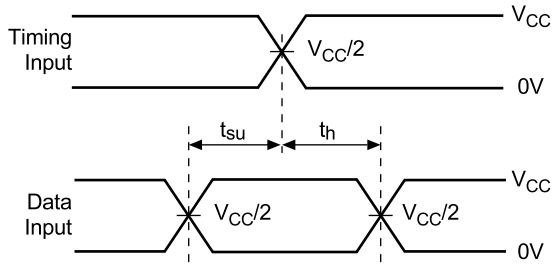
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8V ±0.15V

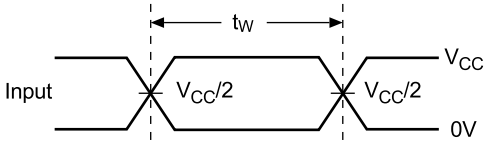


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

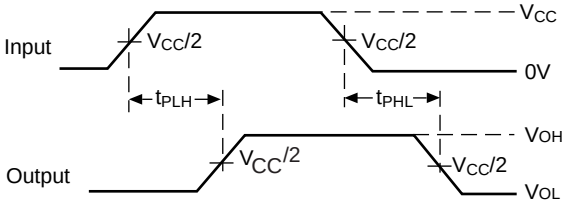
Load Circuit



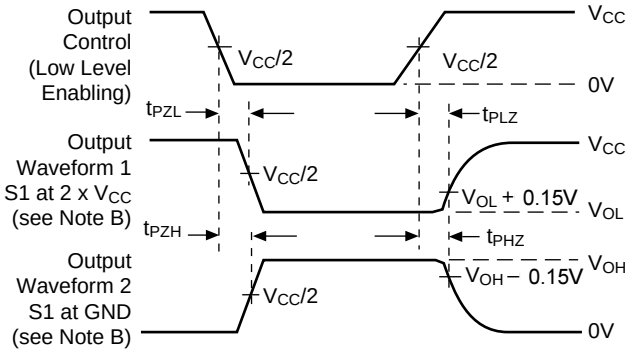
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



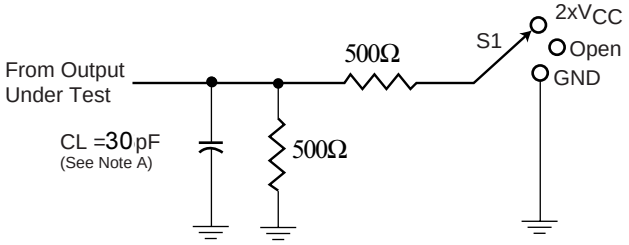
Voltage Waveforms
Enable and Disable Times

Figure 2. Load Circuit and Voltage Waveforms

Notes:

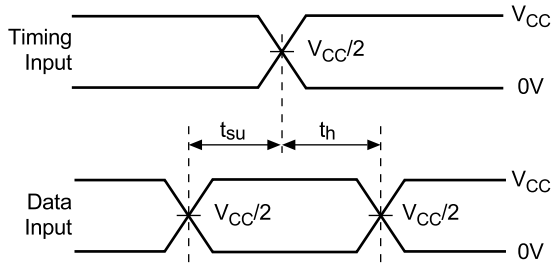
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5V ±0.2V

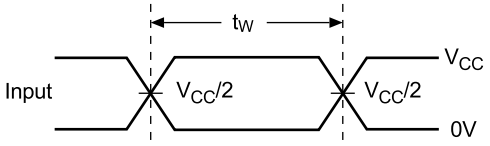


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

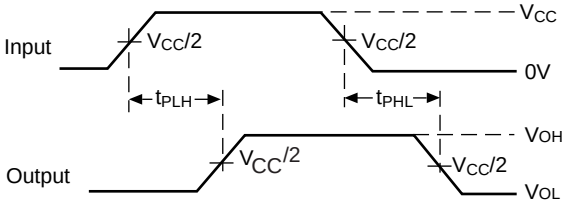
Load Circuit



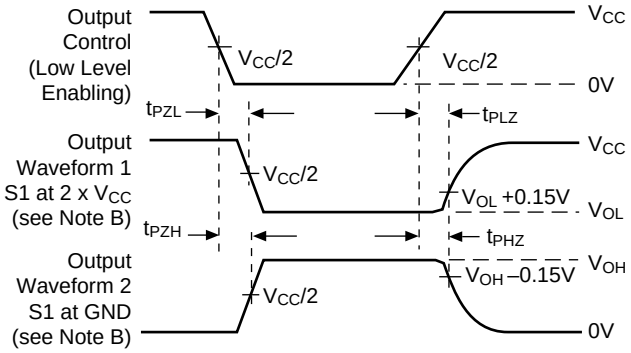
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 3. Load Circuit and Voltage Waveforms

Notes:

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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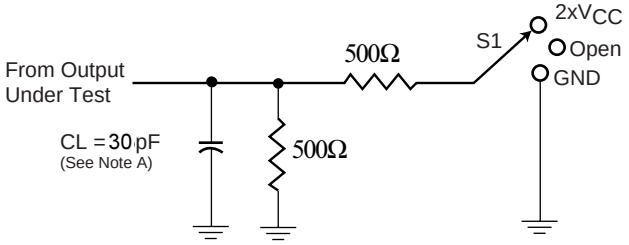
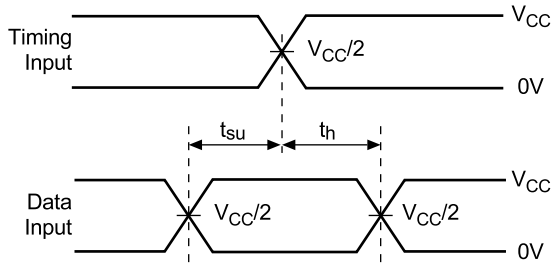
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3V ±0.3V

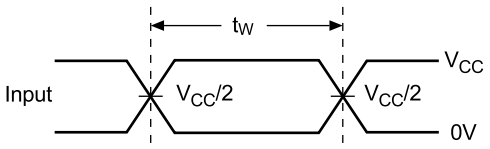


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

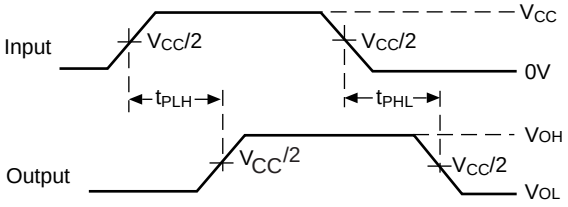
Load Circuit



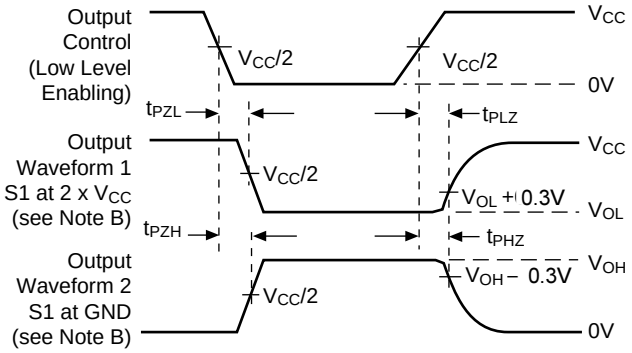
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



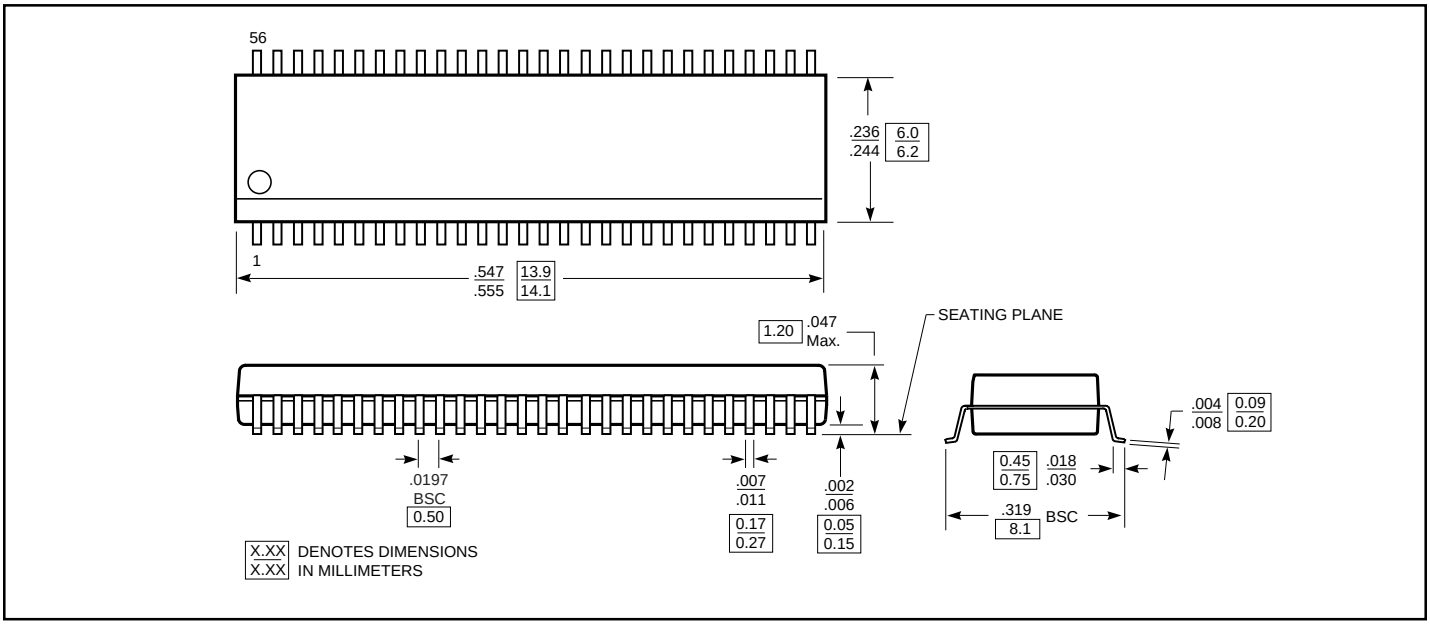
Voltage Waveforms
Enable and Disable Times

Figure 4. Load Circuit and Voltage Waveforms

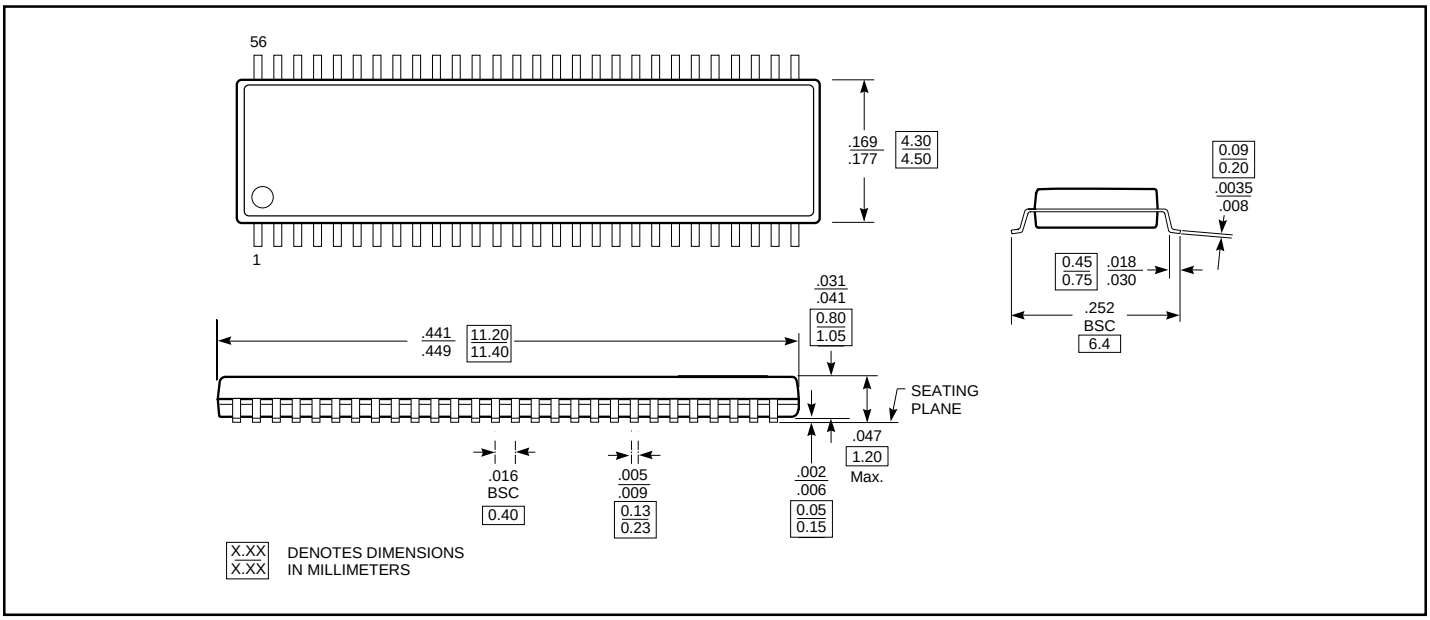
Notes:

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}
F. t_{PZL} and t_{PZH} are the same as t_{en}
G. t_{PLH} and t_{PHL} are the same as t_{pd}

56-Pin TSSOP (A) Package



56-Pin TVSOP (K) Package



Ordering Information

Ordering Data	Description
PI74AVC+16652A	56-pin, 240 mil wide plastic TSSOP
PI74AVC+16652K	56-pin, 173 mil wide plastic TVSOP