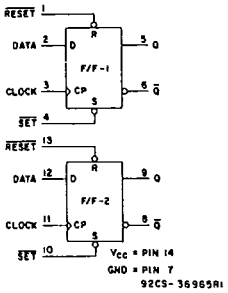
File Number **1476**

CD54/74HC74
CD54/74HCT74

T-46-07-08

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual D Flip-Flop with Set and Reset

Positive-Edge Trigger

Type Features:

- *Hysteresis on clock inputs for improved noise immunity and increased input Rise and Fall times.*
- *Asynchronous Set and Reset*
- *Complementary Outputs*
- *Buffered Inputs*
- *Typical f_{max} = 50 MHz @ V_{CC} = 5V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC74 and CD54/74HCT74 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL Loads.

This flip-flop has independent DATA, $\overline{SET}$, $\overline{RESET}$ and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC74 and CD54HCT74 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC74 and CD74HCT74 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

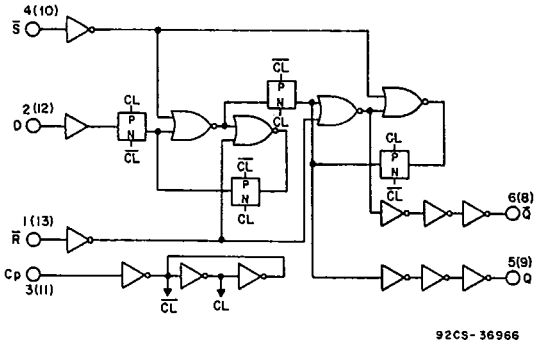


Fig. 1 — Logic Diagram

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to + 85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
⌐ = Transition from Low to High level

NOTES: Q0 = the level of Q before the indicated input conditions were established.
*This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

CD54/74HC74
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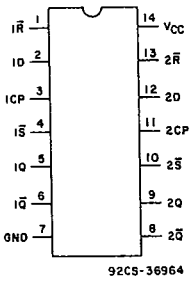
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5\ V < V_o < V_{CC} + 0.5V$) ..... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f•			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.
•Applicable for all inputs except clock.



92CS-36964

TERMINAL ASSIGNMENT

CD54/74HC74
CD54/74HCT74

STATIC ELECTRICAL CHARACTERISTICS

T-46-07-08

CHARACTERISTIC	CD74HC74/CD54HC74										CD74HCT74/CD54HCT74									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
* TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CL} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	4	—	40	—	80	V_{CC} or Gnd	5.5	—	—	4	—	40	—	80	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D	0.5
$\overline{R}$	0.5
CP	0.7
$\overline{S}$	0.75

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r,t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay	t_{PLH} t_{PHL}				
CP to Q, $\overline{Q}$ (Fig. 2)			14	14	
$\overline{R}$ to Q, $\overline{Q}$ (Fig. 3)		15	17	17	ns
$\overline{S}$ to Q, $\overline{Q}$ (Fig. 3)			17	17	
CP Frequency	f_{MAX}	15	50	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	25	30	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Data to CP Set-up Time (Fig. 4)	t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time (Fig. 4)	t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	
		4.5	3	—	3	—	3	—	3	—	3	—	3	—	
		6	3	—	—	—	3	—	—	—	3	—	—	—	
Removal Time $\overline{R}$, $\overline{S}$ to CP (Fig. 3)	t_{REM}	2	30	—	—	—	40	—	—	—	45	—	—	—	
		4.5	6	—	6	—	8	—	8	—	9	—	9	—	
		6	5	—	—	—	7	—	—	—	8	—	—	—	
Pulse Width $\overline{R}$, $\overline{S}$ (Figs. 2, 3)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Pulse Width CP (Figs. 2, 3)	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	18	—	20	—	23	—	24	—	27	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
CP Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	MHz
		6	35	—	—	—	29	—	—	—	23	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r,t_f = 6 ns)

CHARACTERISTIC		V_{CC} (V)	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay, CP to Q, $\overline{Q}$ (Fig. 2)	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	
		6	—	30	—	—	—	37	—	—	—	45	—	—	
$\overline{R}$, $\overline{S}$ to Q, $\overline{Q}$ (Fig. 3)	t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	
	t_{PLH}	4.5	—	40	—	40	—	50	—	50	—	60	—	60	
		6	—	34	—	—	—	43	—	—	—	51	—	—	
Transition Times (Fig. 5)	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

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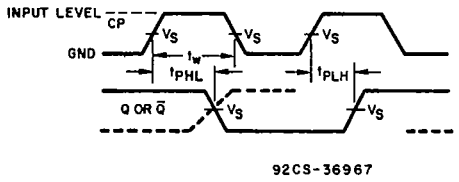

Fig. 2 — Clock pre-requisite and propagation delays.

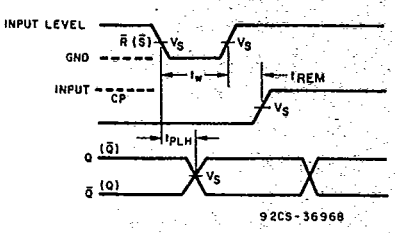

Fig. 3 — $\overline{Reset}$ or $\overline{Set}$ pre-requisite and propagation delays

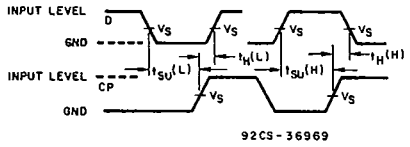

Fig. 4 — Data pre-requisite times.

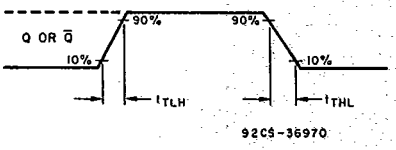

Fig. 5 — Output transition times.

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V