

SN54HCT564, SN74HCT564 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D2804, MARCH 1984 - REVISED SEPTEMBER 1987

- Inputs are TTL-Voltage Compatible
- High-Current 3-State Output Drive Bus-Lines Directly or Up to 15 LSTTL Loads
- Bus-Structured Pinout
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit registers feature three-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight-bit edge-triggered D-type flip-flops enter data on the low-to-high transition of the clock.

An output-control (\overline{OC}) input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

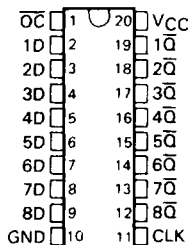
The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54HCT564 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT564 is characterized for operation from -40°C to 85°C .

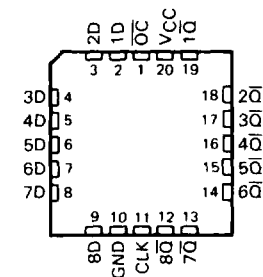
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
\overline{OC}	CLK	D	\overline{Q}
L	↑	H	L
L	↑	L	H
L	L	X	\overline{Q}_0
H	X	X	Z

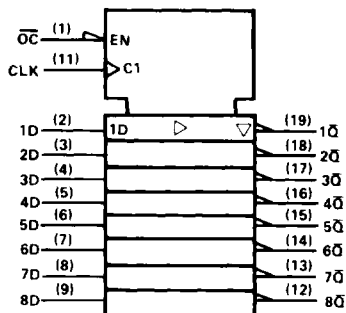
SN54HCT564 . . . J PACKAGE
SN74HCT564 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT564 . . . FK PACKAGE
(TOP VIEW)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

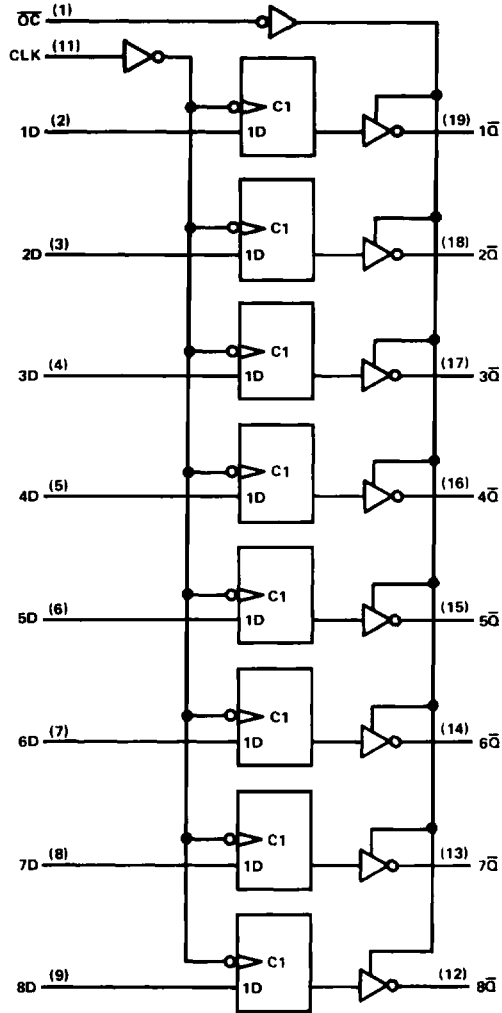

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HCT564			SN74HCT564			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			0			V
V_I	Input voltage	0			V_{CC}			V
V_O	Output voltage	0			V_{CC}			V
t_t	Input transition (rise and fall) times	0			500			ns
T_A	Operating free-air temperature	-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT564		SN74HCT564		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20$ μA	4.5 V	4.4	4.499		4.4		4.4	V	
	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -6$ mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20$ μA	4.5 V		0.001	0.1			0.1	V	
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 6$ mA	4.5 V		0.17	0.26			0.33		
I_I	$V_I = V_{CC}$ or 0	5.5 V		± 0.1	± 100			± 1000	nA	
I_{OZ}	$V_O = V_{CC}$ or 0	5.5 V		± 0.01	± 0.5			± 10	μA	
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V			8			160	μA	
ΔI_{CC}^\dagger	One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4			3	2.9	mA
C_i		4.5 to 5.5 V		3	10			10	10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

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OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		SN54HCT564		SN74HCT564		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock} Clock frequency	4.5 V	0	31	21		25		MHz
	5.5 V	0	36	23		28		
t _w Pulse duration, CLK high or low	4.5 V	16		24		20		ns
	5.5 V	14		22		18		
t _{su} Setup time, data before CLK†	4.5 V	20		30		25		ns
	5.5 V	17		27		23		
t _h Hold time, data after CLK†	4.5 V	5		5		5		ns
	5.5 V	5		5		5		

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT564		SN74HCT564		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f _{max}			4.5 V	31	36		21		25		MHz	
			5.5 V	36	40		23		28			
t _{pd}	CLK	Any \bar{Q}	4.5 V		18	36		54		45		ns
			5.5 V		16	32		48		41		
t _{en}	\bar{OC}	Any \bar{Q}	4.5 V		14	30		45		38		ns
			5.5 V		10	27		41		34		
t _{dis}	\bar{OC}	Any \bar{Q}	4.5 V		22	30		45		38		ns
			5.5 V		20	27		41		34		
t _t		Any \bar{Q}	4.5 V		10	12		18		15		ns
			5.5 V		9	11		16		14		

C _{pd}	Power dissipation capacitance per flip-flop	No load, T _A = 25°C	93 pF typ
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT564		SN74HCT564		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{pd}	CLK	Any \bar{Q}	4.5 V		38	53		80		66		ns
			5.5 V		36	47		71		60		
t _{en}	\bar{OC}	Any \bar{Q}	4.5 V		30	47		71		59		ns
			5.5 V		27	39		59		49		
t _t		Any \bar{Q}	4.5 V		18	42		63		53		ns
			5.5 V		16	38		57		48		

Note 1: Load circuits and voltage waveforms are shown in Section 1.