Integrated Device Technology, Inc.

# 3.3V CMOS 16-BIT REGISTER

**IDT74ALVCH16374**
**IDT74ALVCH162374**
**IDT74ALVC16374**
**ADVANCE INFORMATION**

## FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **Typical tsk(o) (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP, 19.6 mil pitch TSSOP, and 15.7 mil pitch TVSOP packages
  - Extended commercial range of -40°C to +85°C
  - VCC = 3.3V ±0.3V, Normal Range
  - VCC = 2.7V to 3.6V, Extended Range
  - VCC = 2.5V ±0.2V
  - CMOS power levels (0.4µW typ. static)
  - Rail-to-Rail output swing for increased noise margin
- **Features for ALVCH16374 and ALVC16374:**
  - High Drive Outputs: ±24mA
  - Suitable for heavy loads
- **Features for ALVCH162374:**
  - Light Balanced Output Driver: ±12mA
  - Minimal switching noise

## DESCRIPTION:

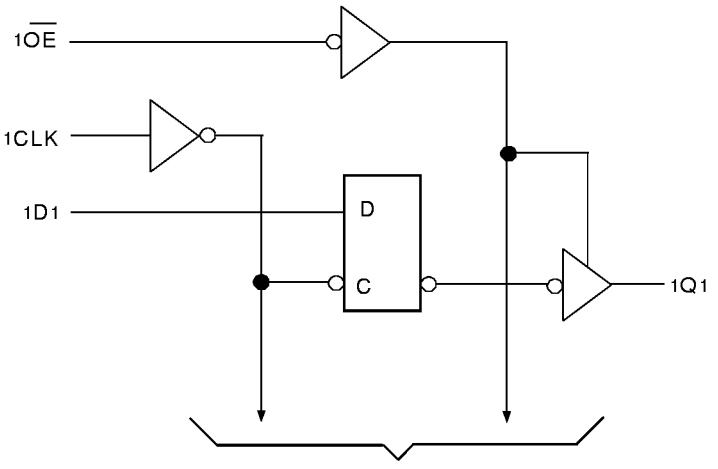
The ALVCH16374 16-bit edge-triggered D-type registers are built using advanced dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable (xOE) and clock (xCLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The ALVCH16x374 have "bus-hold" which retains the input's last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistor.

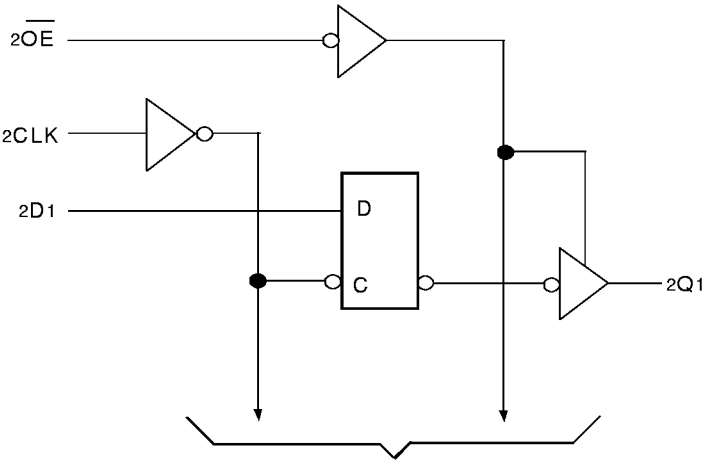
The ALVCH16374/ALVC16374 have been designed with a ±24mA output driver. These drivers are capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH162374 has series resistors in the device output structure which will significantly reduce line noise when used whith light loads. This driver has been designed to drive ±12mA at the designated threshold levels.

## FUNCTIONAL BLOCK DIAGRAM




4218 drw 01

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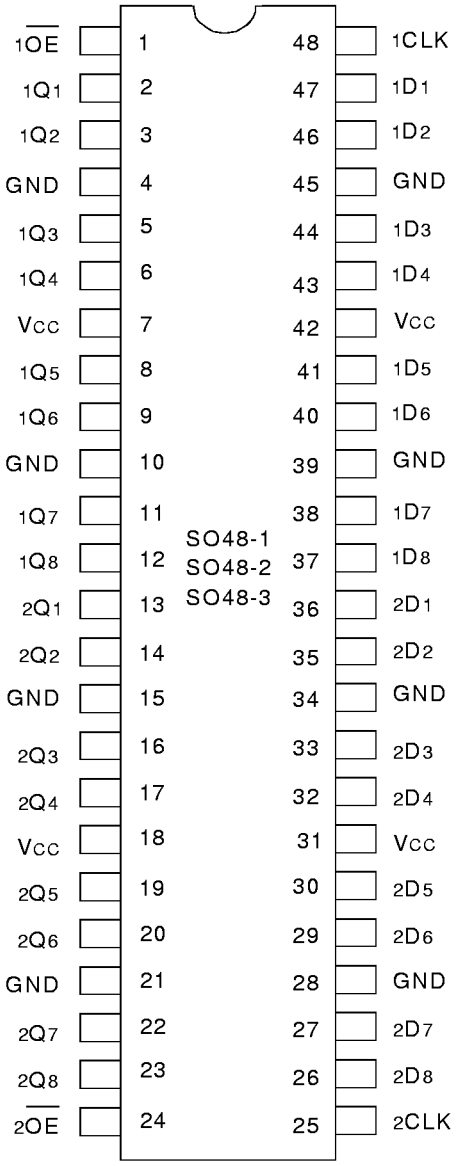
## PIN CONFIGURATIONS

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**SSOP/ TSSOP/TVSOP TOP VIEW**

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| xDx | Data Inputs(1) |
| xCLK | Clock Inputs |
| xQx | 3-State Outputs. |
| $x\overline{OE}$ | 3-State Output Enable Input (Active LOW) |

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**NOTE:**
1. On ALVCH these pins have "Bus-hold". All other pins are standard inputs outputs or I/Os. On ALVC no pins have "Bus-hold".

## ABSOLUTE MAXIMUM RATING(1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +4.6 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$ +0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | –60 to +60 | mA |
| $I_{IK}$ $I_{OK}$ | Continuous Clamp Current, $V_I < 0$ or $V_O < 0$ | –50 | mA |
| $I_{CC}$ $I_{SS}$ | Continuous Current through each $V_{CC}$ or GND | ±100 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{CC}$ terminals.
3. All terminals except $V_{CC}$.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5.0 | 7.0 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 7.0 | 9.0 | pF |
| $C_{I/O}$ | I/O Port Capacitance | $V_{IN}$ = 0V | 7.0 | 9.0 | pF |

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**NOTE:**
1. As applicable to the device type.

## FUNCTION TABLE(1)

| Function | Inputs | | | Outputs |
|---|---|---|---|---|
| | xDx | xCLK | $x\overline{OE}$ | xQx |
| Hi-Z | X | L | H | Z |
| | X | H | H | Z |
| Load Register | L | ↑ | L | L |
| | H | ↑ | L | H |
| | L | ↑ | H | Z |
| | H | ↑ | H | Z |

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**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: $T_A$ = –40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7 V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = 3.6V | $V_I$ = $V_{CC}$ | — | — | ±1 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = 3.6V | $V_I$ = GND | — | — | ±1 | |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = 3.6V | $V_O$ = $V_{CC}$ | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State Output pins) | | $V_O$ = GND | — | — | ±1 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = –18mA | | — | 0.7 | –1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V<br>$V_{IN}$ = GND or $V_{CC}$ | | — | 0.1 | 40 | µA |

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## BUS-HOLD CHARACTERISTICS FOR ALVCH16x374

| Symbol | Parameter(2) | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 3.0V | $V_I$ = 2.0V | –75 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.8V | 75 | — | — | |
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 2.3V | $V_I$ = 1.7V | –45 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.7V | 45 | — | — | |
| $I_{BHHO}$ | Bus-Hold Input Overdrive Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 3.6V | — | — | ±500 | µA |
| $I_{BHLO}$ | | | | | | | |

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**NOTES:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.
2. Pins with Bus-hold are identified in the pin description.

## OUTPUT DRIVE CHARACTERISTICS FOR ALVCH16374 AND ALVC16374

| Symbol | Parameter | Test Conditions[1] | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = –0.1mA | $V_{CC}$–0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = –6mA | 2 | — | |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = –12mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | | 2.2 | — | |
| | | $V_{CC}$ = 3.0V | | 2.4 | — | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = –24mA | 2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 6mA | — | 0.4 | |
| | | | $I_{OL}$ = 12mA | — | 0.7 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 12mA | — | 0.4 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 24mA | — | 0.55 | |

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## OUTPUT DRIVE CHARACTERISTICS FOR ALVCH162374

| Symbol | Parameter | Test Conditions[1] | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = –0.1mA | $V_{CC}$–0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = –4mA | 1.9 | — | |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = –6mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | $I_{OH}$ = –8mA | 2 | — | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = –6mA | 2.4 | — | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = –12mA | 2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 4mA | — | 0.4 | |
| | | | $I_{OL}$ = 6mA | — | 0.55 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 8mA | — | 0.6 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 12mA | — | 0.8 | |

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**NOTE:**

1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ =–40°C to +85°C.

## SWITCHING CHARACTERISTICS FOR ALVCH16374 AND ALVC16374[1]

| Symbol | Parameter | $V_{CC}$ = 2.5V ±0.2V | | $V_{CC}$ = 2.7V | | $V_{CC}$ = 3.3V ±0.3V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{MAX}$ | xCLK Frequency | 0 | 150 | 0 | 150 | 0 | 150 | MHz |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay xCLK to xQx | 1 | 5.9 | 1 | 4.9 | 1 | 4.2 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time | 1 | 6.7 | 1 | 5.9 | 1 | 4.8 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time | 1.7 | 5.5 | 1 | 4.7 | 1.2 | 4.3 | ns |
| $t_{SU}$ | Set-up Time HIGH or LOW xDx to xCLK | 2.1 | — | 2.2 | — | 1.9 | — | ns |
| $t_H$ | Hold Time HIGH or LOW xDx after xCLK | 0.6 | — | 0.5 | — | 0.5 | — | ns |
| $t_W$ | xCLK Pulse Width HIGH or LOW | 3.3 | — | 3.3 | — | 3.3 | — | ns |
| $t_{SK(o)}$ | Output Skew[2] | 0 | 500 | 0 | 500 | 0 | 500 | ps |

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## SWITCHING CHARACTERISTICS FOR ALVCH162374[1]

| Symbol | Parameter | $V_{CC}$ = 2.5V ±0.2V | | $V_{CC}$ = 2.7V | | $V_{CC}$ = 3.3V ±0.3V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{MAX}$ | xCLK Frequency | 0 | | 0 | | 0 | | MHz |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay xCLK to xQx | 1 | | 1 | | 1 | | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time | 1 | | 1 | | 1 | | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time | 1 | | 1 | | 1.2 | | ns |
| $t_{SU}$ | Set-up Time HIGH or LOW xDx to xCLK | | — | | — | | — | ns |
| $t_H$ | Hold Time HIGH or LOW xDx after xCLK | | — | | — | | — | ns |
| $t_W$ | xCLK Pulse Width HIGH or LOW | | — | | — | | — | ns |
| $t_{SK(o)}$ | Output Skew[2] | 0 | 500 | 0 | 500 | 0 | 500 | ps |

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**NOTES:**
1. See test circuits and waveforms. $T_A$ = –40°C to +85°C.
2. Skew between any two outputs of the same package switching in the same direction.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Standard Inputs HIGH | $V_{CC}$ = Max. | $V_{IN} = V_{CC} - 0.6V$[3] | — | 2.0 | 30 | µA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Bus-hold Inputs HIGH | $V_{CC}$ = Max. | $V_{IN} = V_{CC} - 0.6V$[3] | — | 162 | 325 | µA |
| $I_{CCD}$ | Dynamic Power Supply Current[4,5] | $V_{CC}$ = Max.<br>Outputs Open<br>x$\overline{OE}$ = GND<br>50% Duty Cycle<br>One Input Toggling | $V_{IN} = V_{CC}$<br>$V_{IN}$ = GND | — | 50 | 75 | µA/<br>MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>Outputs Open<br>$f_{CP}$ = 10MHz<br>50% Duty Cycle<br>x$\overline{OE}$ = GND<br>fi = 5MHz<br>50% Duty Cycle<br>One Bit Toggling | $V_{IN} = V_{CC}$<br>$V_{IN}$ = GND | — | 0.5 | 0.8 | mA |
| | | | $V_{IN} = V_{CC} - 0.6V$<br>$V_{IN}$ = GND | — | 0.5 | 0.8 | |
| | | $V_{CC}$ = Max.<br>Outputs Open<br>$f_{CP}$ = 10MHz<br>50% Duty Cycle<br>x$\overline{OE}$ = GND<br>fi = 2.5MHz<br>50% Duty Cycle<br>Sixteen Bits Toggling | $V_{IN} = V_{CC}$<br>$V_{IN}$ = GND | — | 2.5 | 3.8 | |
| | | | $V_{IN} = V_{CC} - 0.6V$<br>$V_{IN}$ = GND | — | 2.5 | 4.0 | |

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**NOTES:**

1. $V_{CC}$ (max.) = 3.6V
2. Typical values are at $V_{CC}$ = 3.3V, +25° C ambient.
3. Per TTL driven input; all other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. $C_{PD} = I_{CCD}/V_{CC}$
   $C_{PD}$ = Power Dissipation Capacitance
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current ($I_{CCL}$, $I_{CCH}$ and $I_{CCZ}$)
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $N_{CP}$ = Number of Clock Inputs at $f_{CP}$
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$

## TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

| Symbol | Vcc = 3.3V ±0.3V | Vcc = 2.7V | Vcc = 2.5V±0.2V | Unit |
|---|---|---|---|---|
| $V_{LOAD}$ | 6 | 6 | 4.6 | V |
| $V_{IH}$ | 2.7 | 2.7 | 2.3 | V |
| $V_T$ | 1.5 | 1.5 | $V_{CC}/2$ | V |
| $V_{LZ}$ | 300 | 300 | 150 | mV |
| $V_{HZ}$ | 300 | 300 | 150 | mV |
| $C_L$ | 50 | 50 | 30 | pF |

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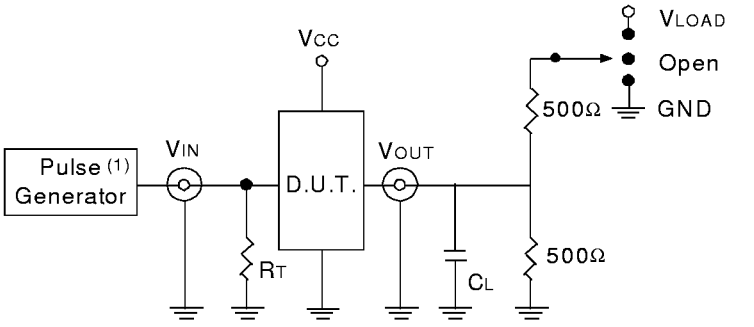
**DEFINITIONS:**

$C_L$= Load capacitance: includes jig and probe capacitance.

$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

## TEST CIRCUITS FOR ALL OUTPUTS




4218 drw 04

**NOTE:**

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other tests | Open |

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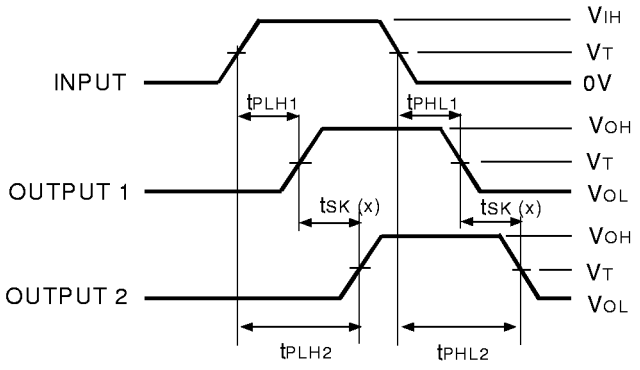
## OUTPUT SKEW - tSK (x)




$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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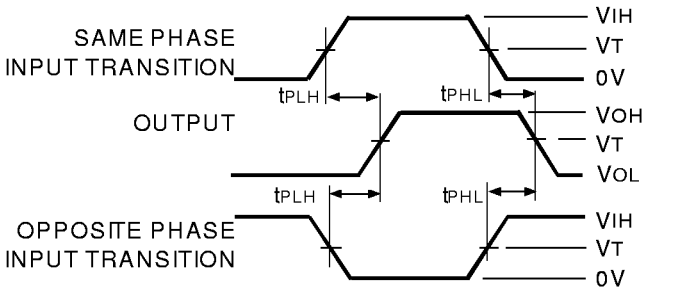
**NOTES:**

1. For tSK(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tSK(b) OUTPUT1 and OUTPUT2 are in the same bank.

## PROPAGATION DELAY

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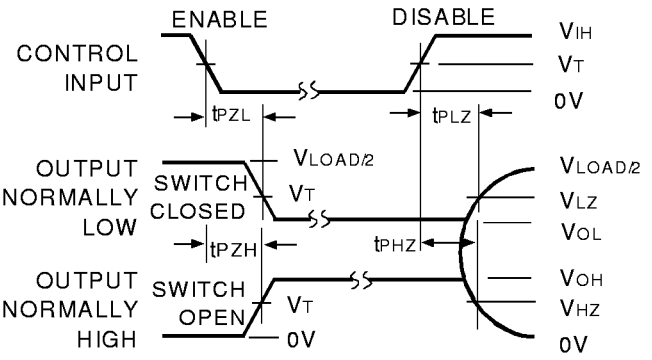
## ENABLE AND DISABLE TIMES




**NOTE:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

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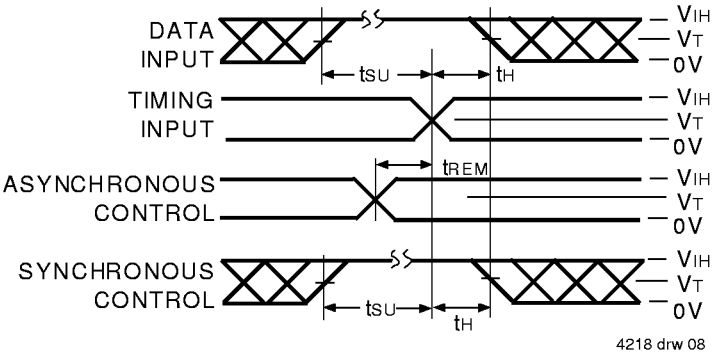
## SET-UP, HOLD AND RELEASE TIMES

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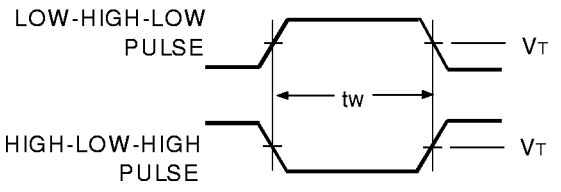
## PULSE WIDTH

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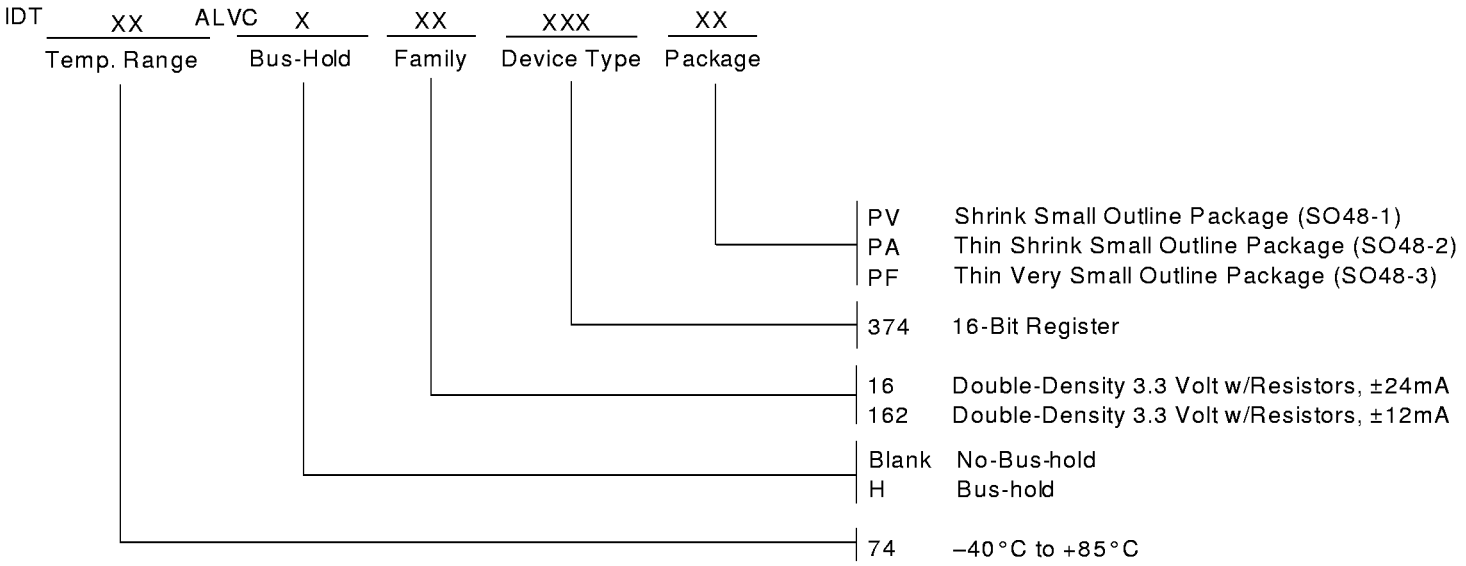
## ORDERING INFORMATION

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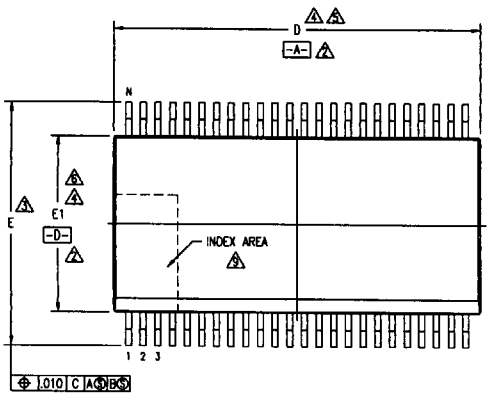
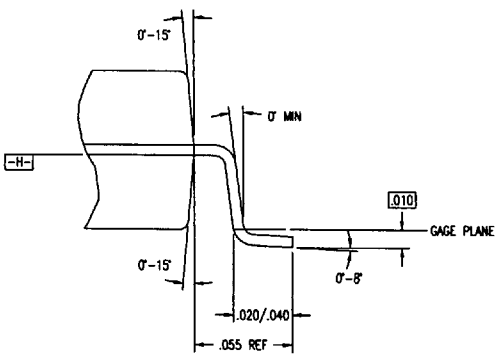
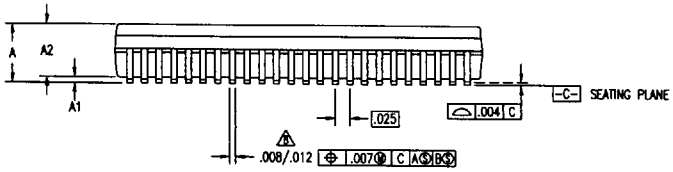
## SSOP

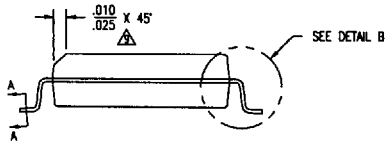
| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 17893 | 00 | INITIAL RELEASE | 07/15/90 | A. FUNCELL |
| 22377 | 01 | REMOVE CHAMFER FROM PACKAGE | 04/15/92 | T. VU |
| 27492 | 02 | REDRAW TO JEDEC FORMAT | 02/01/95 | |

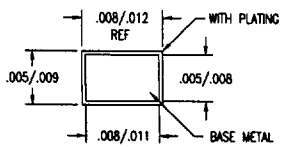



DETAIL B




SECTION A-A

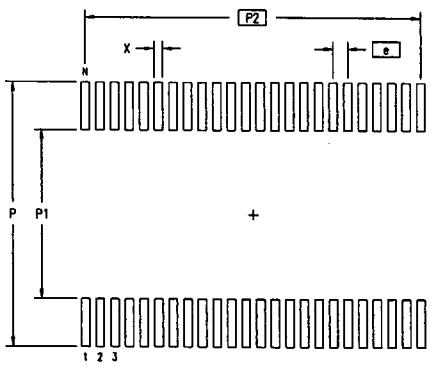
| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 | |
|---|---|---|---|
| DECIMAL XX± XXX± XXXX± | ANGULAR ± | | |
| APPROVALS | DATE | TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH | |
| DRAWN AA | 08/15/90 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4029 REV 02 |
| | | DO NOT SCALE DRAWING | |

## SSOP (Continued)

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 17893 | 00 | INITIAL RELEASE | 07/15/90 | A. FUNCELL |
| 22377 | 01 | REMOVE CHAMFER FROM PACKAGE | 04/15/92 | T. VU |
| 27492 | 02 | REDRAW TO JEDEC FORMAT | 02/01/95 | |

| DWG # | | S048-1 | | | DWG # | | S056-1 | | |
|---|---|---|---|---|---|---|---|---|---|
| SYMBOL | JEDEC VARIATION AA | | | NOTE | JEDEC VARIATION AB | | | NOTE |
| | MIN | NOM | MAX | | MIN | NOM | MAX | |
| A | .095 | .102 | .110 | | .095 | .102 | .110 | |
| A1 | .008 | .012 | .016 | | .008 | .012 | .016 | |
| A2 | .088 | .090 | .092 | | .088 | .090 | .092 | |
| D | .620 | .625 | .630 | 4,5 | .720 | .725 | .730 | 4,5 |
| E | .395 | .405 | .420 | 3 | .395 | .405 | .420 | 3 |
| E1 | .291 | .295 | .299 | 4,6 | .291 | .295 | .299 | 4,6 |
| N | 48 | | | | 56 | | | |

### LAND PATTERN DIMENSIONS




| | MIN | MAX | MIN | MAX |
|---|---|---|---|---|
| P | .450 | .458 | .450 | .458 |
| P1 | .282 | .290 | .282 | .290 |
| P2 | .575 BSC | | .675 BSC | |
| X | .010 | .018 | .010 | .018 |
| e | .025 BSC | | .025 BSC | |
| N | 48 | | 56 | |

### NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

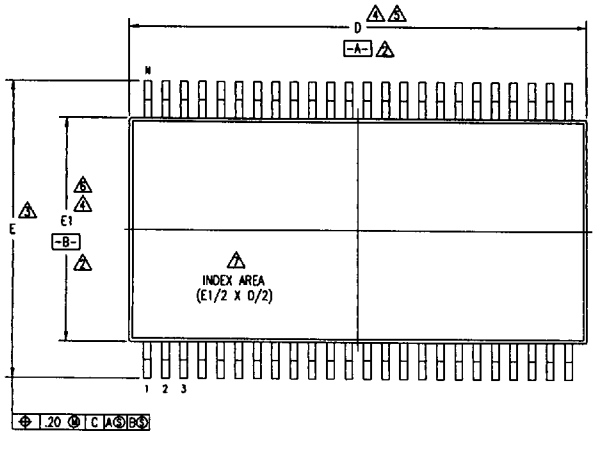
10 ALL DIMENSIONS ARE IN INCHES

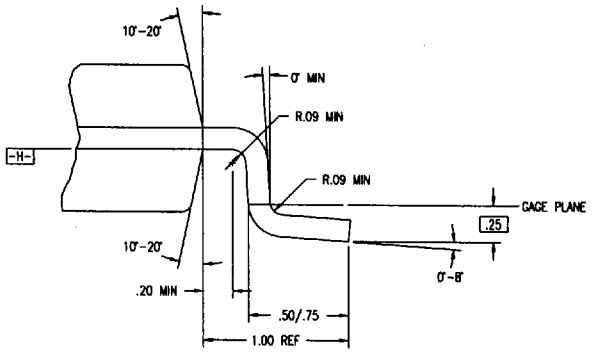
11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARATION AA & AB

| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. |
|---|---|---|
| DECIMAL XX± XXX± XXXX± | ANGULAR ± | 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 |
| APPROVALS | DATE | TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH |
| DRAWN AA | 05/15/90 | |
| CHECKED | | SIZE C DRAWING No. PSC-4029 REV 02 |
| | | DO NOT SCALE DRAWING |

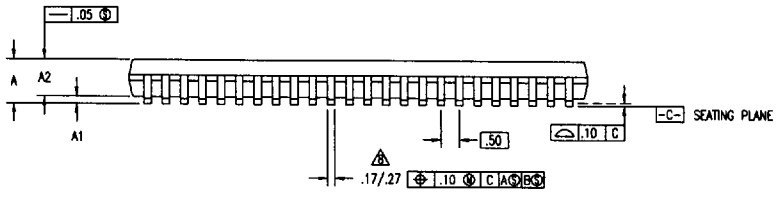
## TSSOP

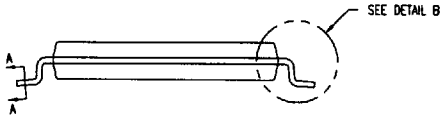
| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 23757 | 00 | INITIAL RELEASE | 02/15/93 | T. VU |
| 26315 | 01 | CHANGE DIMS A1 & A2 | 05/18/94 | DG |
| 25490 | 02 | CHANGE DIM A1 | 07/21/94 | T. VU |
| 27494 | 03 | REDRAW TO JEDEC FORMAT | 03/08/95 | |

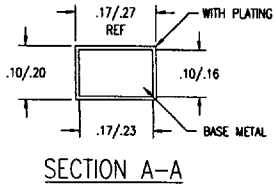



DETAIL B




SECTION A-A

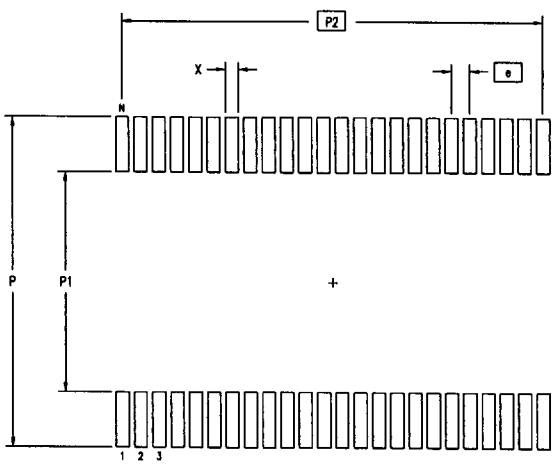
| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070 | |
| DECIMAL | ANGULAR | | |
| XX± | ± | | |
| XXX± | | | |
| XXXX± | | | |
| APPROVALS | DATE | TITLE | PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH |
| DRAWN dd | 01/15/93 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4039 REV 03 |
| | | DO NOT SCALE DRAWING | |

## TSSOP (Continued)

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| 23757 | 00 | INITIAL RELEASE | 02/15/93 | T. VU |
| 26315 | 01 | CHANGE DIMS A1 & A2 | 05/18/94 | DG |
| 26490 | 02 | CHANGE DIM A1 | 07/21/94 | T. VU |
| 27494 | 03 | REDRAW TO JEDEC FORMAT | 03/08/95 | |

| DWG # | | | S048-2 | | DWG # | | | S056-2 | |
|---|---|---|---|---|---|---|---|---|---|
| SYMBOL | JEDEC VARIATION ED | | | NOTE | JEDEC VARIATION EE | | | NOTE |
| | MIN | NOM | MAX | | MIN | NOM | MAX | |
| A | – | – | 1.10 | | – | – | 1.10 | |
| A1 | .05 | – | .15 | | .05 | – | .15 | |
| A2 | .85 | 1.00 | 1.05 | | .85 | 1.00 | 1.05 | |
| D | 12.40 | 12.50 | 12.60 | 4,5 | 13.90 | 14.00 | 14.10 | 4,5 |
| E | 7.95 | 8.10 | 8.25 | 3 | 7.95 | 8.10 | 8.25 | 3 |
| E1 | 6.00 | 6.10 | 6.20 | 4,6 | 6.00 | 6.10 | 6.20 | 4,6 |
| N | 48 | | | | 56 | | | |

### LAND PATTERN DIMENSIONS



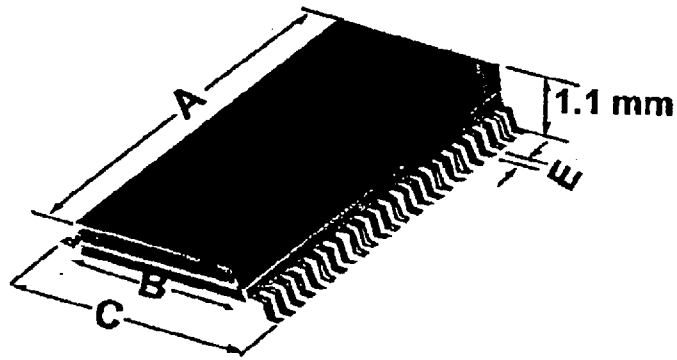

| | MIN | MAX | MIN | MAX |
|---|---|---|---|---|
| P | 8.90 | 9.10 | 8.90 | 9.10 |
| P1 | 5.90 | 6.10 | 5.90 | 6.10 |
| P2 | 11.50 BSC | | 13.50 BSC | |
| X | .30 | .40 | .30 | .40 |
| e | .50 BSC | | .50 BSC | |
| N | 48 | | 56 | |

### NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-
4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION ED & EE

| TOLERANCES UNLESS SPECIFIED | | Integrated Device Technology, Inc. |
|---|---|---|
| DECIMAL ANGULAR | | 2975 Stender Way, Santa Clara, CA 95054 |
| XX± ± | | PHONE: (408) 727-6116 |
| XXX± | | FAX: (408) 492-8674 TWX: 910-338-2070 |
| XXXX± | | |
| APPROVALS | DATE | TITLE PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH |
| DRAWN AA | 01/13/93 | |
| CHECKED | | SIZE C DRAWING No. PSC-4039 REV 03 |
| | | DO NOT SCALE DRAWING |

# TVSOP
# The Most Compact Double Density Package




| TVSOP Package | Typical Dimensions (in mm) | | | | Area (mm2) |
|---|---|---|---|---|---|
| | A | B | C | E | |
| 48 Pin | 9.80 | 4.40 | 6.40 | 0.40 | 63.00 |
| 56 Pin | 11.30 | 4.40 | 6.40 | 0.40 | 72.30 |
| 80 Pin | 17.00 | 6.10 | 8.10 | 0.40 | 137.80 |
| 100 Pin | 20.80 | 6.10 | 8.10 | 0.40 | 168.50 |

# Double Density Packaging

## 48-Pin


16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²


12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²


9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

## 56-Pin


18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²


14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²


11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

| TVSOP | Area ($mm^2$) | %Smaller Than SSOP | %Smaller Than TSSOP |
|---|---|---|---|
| 48 pin | 63.00 | 61.9 | 38.0 |
| 56 pin | 72.30 | 62.2 | 36.0 |