Integrated Device Technology, Inc.

3.3V CMOS SINGLE POSITIVE-NAND GATE WITH SCHMITT-TRIGGER INPUTS, 5 VOLT TOLERANT I/O

IDT74LVC1G132A
ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.65mm pitch PSOP package
- Extended commercial range of – 40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range
- Vcc = 1.65V to 3.6V, Extended Range
- Vcc = 2.5V ±0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC1G132A:

- High Output Drivers: ±24mA
- Reduced system switching noise

DESCRIPTION:

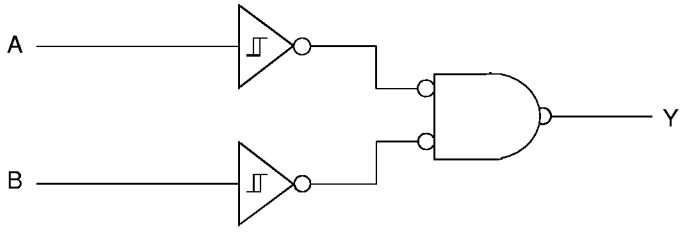
This single positive NAND gate is built using advanced dual metal CMOS technology. The LVC1G132A is designed for 1.65V to 3.6V Vcc operation and performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

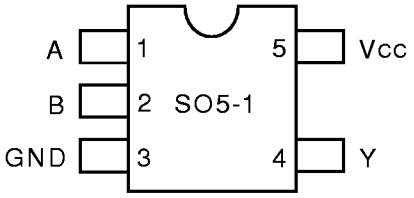
APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
A, B	Data Inputs
Y	Data Output

FUNCTION TABLE (1)

Inputs		Output
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't care

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to + 6.5	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +6.5	V
T_{STG}	Storage Temperature	– 65 to + 150	°C
I_{OUT}	DC Output Current	– 50 to + 50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

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NOTE:
1. As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = – 40°C To +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 1.65V to 1.95V		0.65 x V_{CC}	—	—	V
		V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 1.65V to 1.95V		—	—	0.35 x V_{CC}	
		V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
			3.6 ≤ Vin ≤ 5.5V (2)	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND		—	—	500	µA

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NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies to 3-state outputs in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 1.65V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 1.65V	I_{OH} = – 4mA	1.2	—	
		V_{CC} = 2.3V	I_{OH} = – 8mA	1.7	—	
		V_{CC} = 2.7V	I_{OH} = – 12mA	2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 1.65V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 1.65V	I_{OL} = 4mA	—	0.45	
		V_{CC} = 2.3V	I_{OL} = 8mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to +85°C.

HYSTERESIS CHARACTERISTICS

Parameter	Test Conditions	Vcc	Min.	Typ.	Max.	Unit
V_{T+} Positive-going threshold	Input Voltage, from V_{IL} to V_{IH}, in a linear ramp observing the output transition.	1.65V	—	—	—	V
		2.3V	—	—	—	
		2.7V	0.8‡	—	2	
		3V	0.8‡	—	2	
		3.6V	0.8‡	—	2	
V_{T-} Negative-going threshold	Input Voltage, from V_{IH} to V_{IL}, in a linear ramp observing the output transition.	1.65V	—	—	—	V
		2.3V	—	—	—	
		2.7V	0.4	—	1.4‡	
		3V	0.6	—	1.5‡	
		3.6V	0.8	—	1.8‡	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$\Delta V_{T\ min} = \lvert V_{T+\ min} - V_{T-\ max} \rvert$ $\Delta V_{T\ max} = \lvert V_{T+\ max} - V_{T-\ min} \rvert$	1.65V	—	—	—	V
		2.3V	—	—	—	
		2.7V	0.3	—	1.1	
		3V	0.3	—	1.2	
		3.6V	0.3	—	1.2	

‡ = Guaranteed by design.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	Vcc = 1.8V ± 0.15V Typical	Vcc = 2.5V ± 0.2V Typical	Vcc = 3.3V ± 0.3V Typical	Unit
C_{PD}	Power Dissipation Capacitance	C_L = 0pF, f = 10Mhz	—	—	—	pF

SWITCHING CHARACTERISTICS [1]

Symbol	Parameter	Vcc = 1.8V ± 0.15V		Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay A or B to Y	1	13.7	1	7.9	—	7.5	1	6.4	ns

NOTE:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.

TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	$Vcc^{(1)}$= 3.3V±0.3V	$Vcc^{(1)}$= 2.7V	$Vcc^{(2)}$= 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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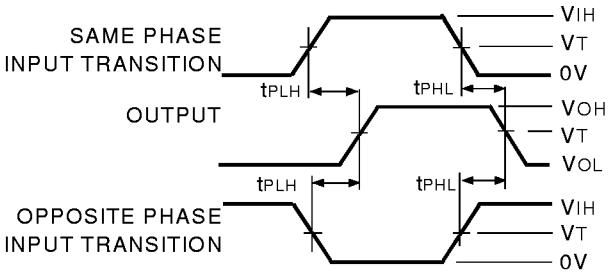
PROPAGATION DELAY



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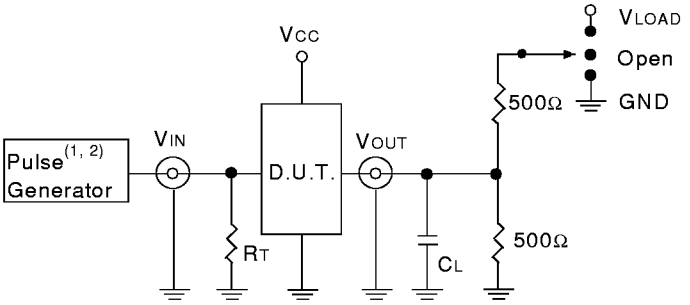
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION:

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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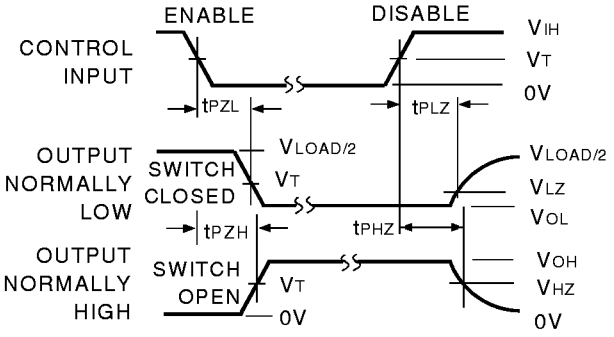
ENABLE AND DISABLE TIMES



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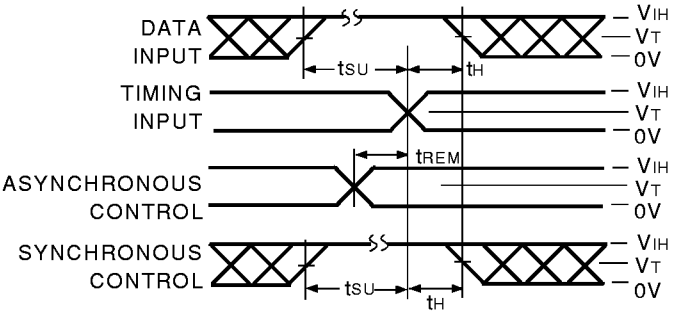
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD AND RELEASE TIMES



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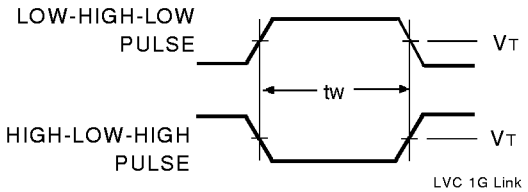
PULSE WIDTH



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1.8V ± 0.15V TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V_{CC} [1] = 1.8V ± 0.15V	Unit
V_{LOAD}	2 x Vcc	V
V_{IH}	Vcc	V
V_T	V_{CC} / 2	V
V_{LZ}	150	mV
V_{HZ}	150	mV
C_L	30	pF

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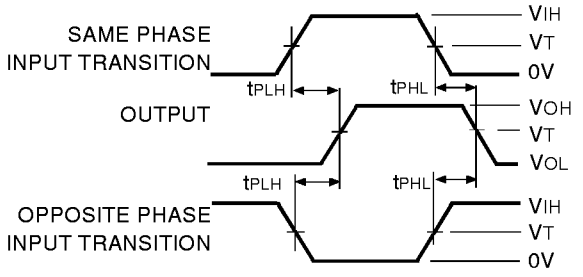
PROPAGATION DELAY



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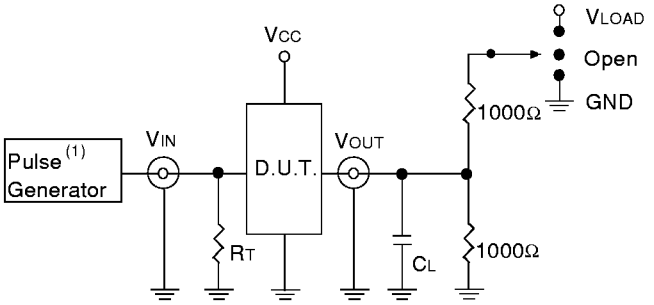
TEST CIRCUITS FOR ALL OUTPUTS



LVC 1G Link

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

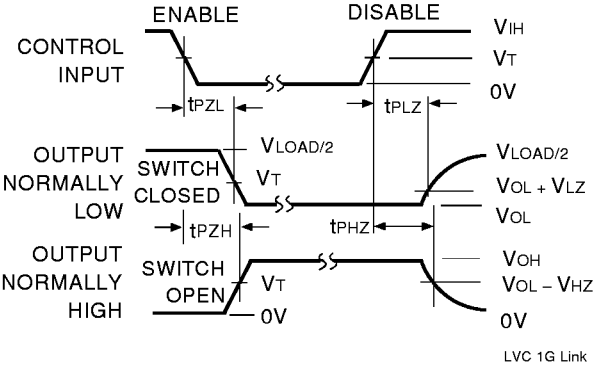
NOTE:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION:

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

LVC 1G Link

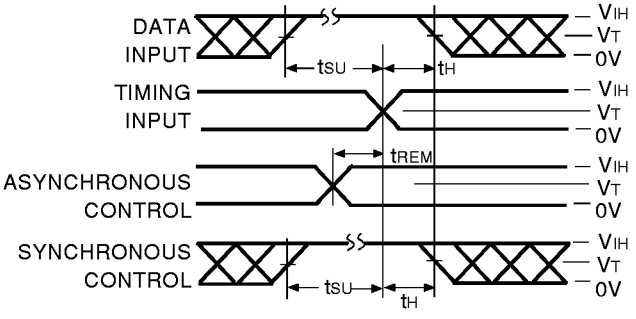
ENABLE AND DISABLE TIMES



LVC 1G Link

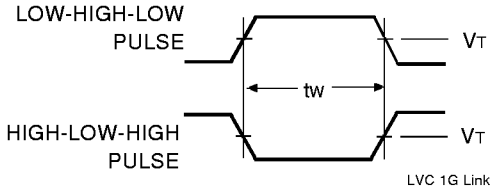
NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD AND RELEASE TIMES



LVC 1G Link

PULSE WIDTH



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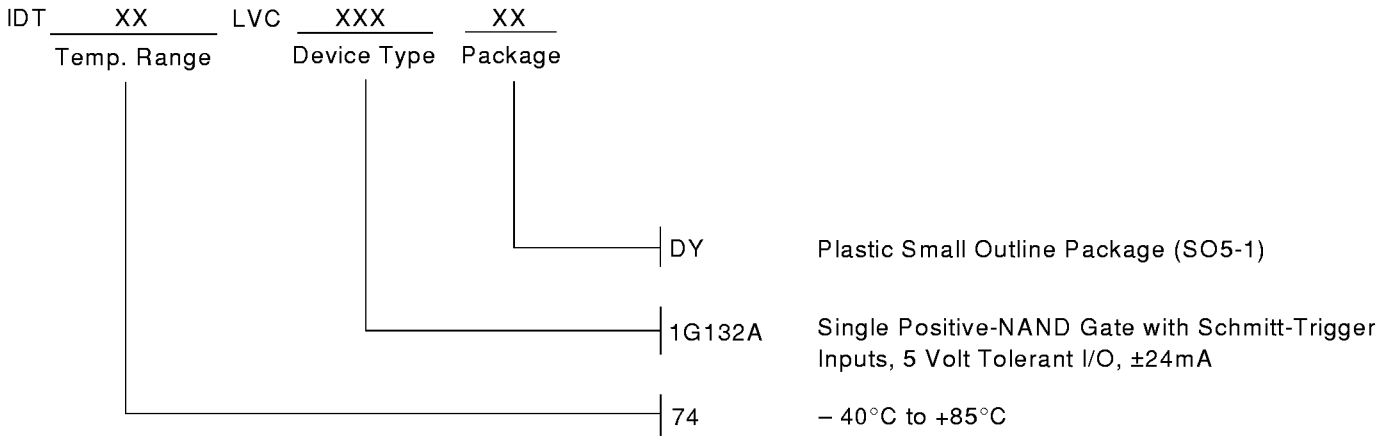
ORDERING INFORMATION



PICOGATE-LOGIC (DY) PACKAGES

Due to their small size, PicoGate-Logic packages require more complex symbolization guidelines. IDT's 5-pin PSOP (DY) packaged devices utilize a three-symbol name rule. The first symbol denotes device technology, the second symbol denotes device function, and the third symbol denotes a wafer fab/assembly site code for internal tracking.

EXAMPLES:

1. A PicoGate-Logic device with package code LR* is an IDT74LVCG179A.
2. A PicoGate-Logic device with package code GC* is an IDT74ALVC1G04.

PICOGATE-LOGIC (DY) PACKAGE SYMBOLIZATION GUIDELINES

TECHNOLOGY	CODE
ALVC	G
ALVCH	J
LVC	L
LVCH(1)	

FUNCTION	CODE
00	A
02	B
04	C
U04	D
06(1)	
07(1)	
08	E
14	F
32	G
79	R
86	H
125	M
126	N
132(1)	

NOTE:
1. Code to be determined.