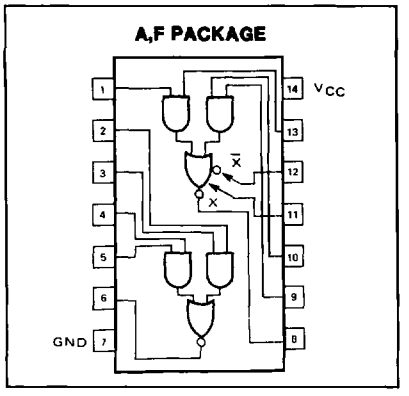
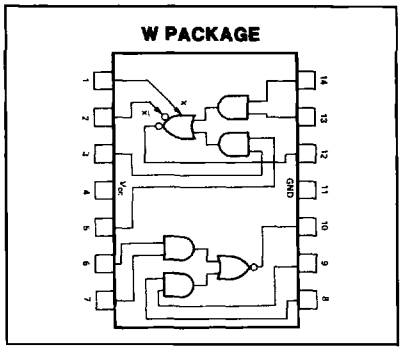
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE 54/7450

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W,	74H	A,F

PIN CONFIGURATION





SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°CC

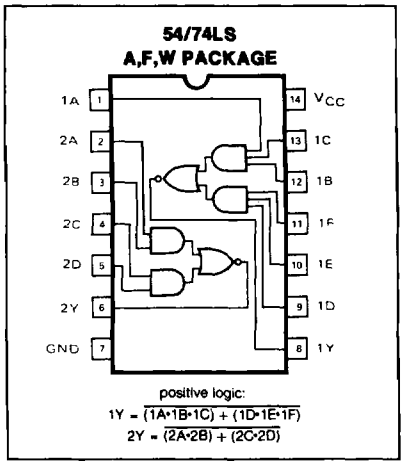
TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω Expander pins are open			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time							
t_{PLH} Low-to-high		13	22		6.8	11	ns
					C_X=15pF		
					11		
t_{PHL} High-to-low		8	15		6.2	11	ns
					C_X=15pF		
					7.4		

Load circuit and typical waveforms are shown at the front of section.

LOGIC

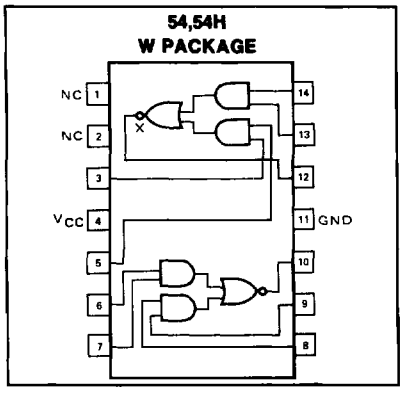
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE 54/7451

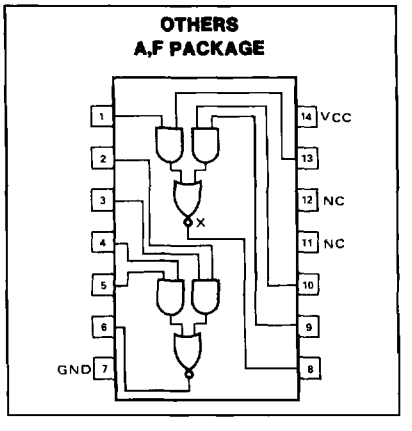
PIN CONFIGURATION



SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F





DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE 54/7451

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		13	22		6.8	11		9	15	2	3.5 (C_L=50pF) 5	5.5	ns
t_{PHL} High-to-low		8	15		6.2	11		9.5	15	2	3.5 (C_L=50pF) 5.5	5.5	ns

Make no external connection to X and $\bar{X}$ pins of the 54/7451 and the 54/74H51.
Load circuit and typical waveforms are shown at the front of section.

4-WIDE 2-2-2-3-INPUT AND-OR GATE 54/7452

SPEED/PACKAGE AVAILABILITY

54H F,W 74H A,F

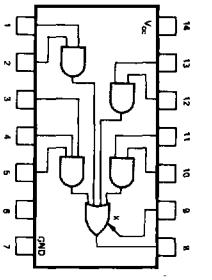
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74H C_L=25pF R_L=280Ω EXPANDER PIN IS OPEN			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		10.6 (C_X = 15pF) 14.8	15	ns
t_{PHL} High-to-low		9.2 (C_X = 15pF) 9.8	15	ns

Load circuit and typical waveforms are shown at the front of section.

PIN CONFIGURATION

A,F PACKAGE



W PACKAGE