DATA SHEET

CBT3384
10-bit bus switch with 5-bit output enables

Product specification
Supersedes data of 2000 Jan 28

2000 Nov 13

Philips
Semiconductors

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10-bit bus switch with 5-bit output enables CBT3384

FEATURES

- 5 Ω switch connection between two ports
- TTL compatible control input and output levels
- See CBTS3384 for CBT3384 with Schottky diode undershoot protection
- See CBTD3384 for CBT3384 with level shifting diodes
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

The CBT3384 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3384 device is organized as two 5-bit bus switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is LOW, the switch is on and port A is connected to B. When $\overline{OE}$ is HIGH, the switch is open and high-impedance state exists between the two ports.

The CBT3384 is characterized for operation from –40 °C to +85 °C.

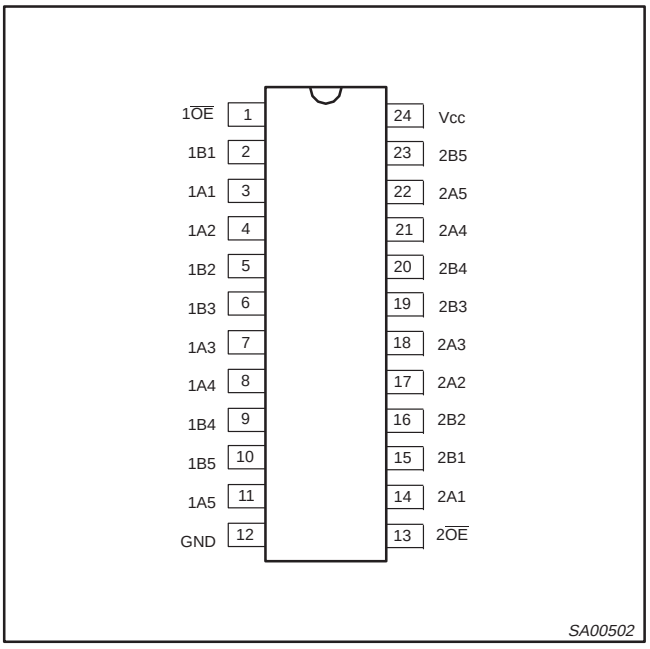
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50 pF; V_{CC} = 5 V	250	ps
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0 V or V_{CC}	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5 V	3	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
24-Pin Plastic SO	–40 °C to +85 °C	CBT3384 D	SOT137-1
24-Pin Plastic SSOP	–40 °C to +85 °C	CBT3384 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40 °C to +85 °C	CBT3384 PW DH	SOT355-1

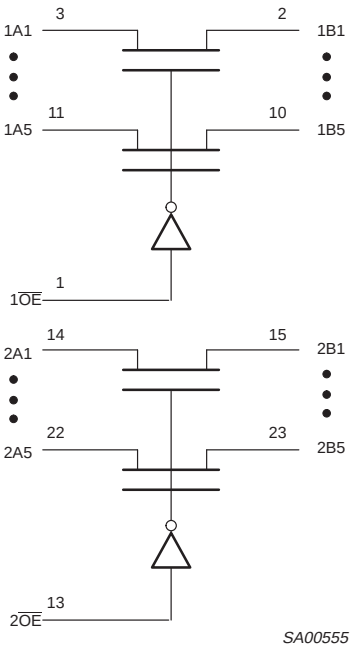
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{OE}$, $2\overline{OE}$	Output enables
3, 4, 7, 8, 11	1A1–1A5	Inputs
14, 17, 18, 21, 22	2A1–2A5	Inputs
2, 5, 6, 9, 10	1B1–1B5	Outputs
15, 16, 19, 20, 23	2B1–2B5	Outputs
12	GND	Ground (0 V)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
$1\overline{OE}$	**$2\overline{OE}$**	**1A, 1B**	**2A, 2B**
L	L	1A = 1B	2A= 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance “off” state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current		–50	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{SW}	DC output diode current	$V_O < 0$	±128	mA
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T_{amb} = –40°C to +85°C			
			Min	Typ[1]	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_I = –18 mA			–1.2	V
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V			±1	μA
I_{CC}	Quiescent supply current[2]	V_{CC} = 5.5 V; I_O = 0, V_I = V_{CC} or GND			3	μA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V, one input at 3.4 V, other inputs at V_{CC} or GND			2.5	mA
C_I	Control pins	V_I = 3.0 V or 0		4		pF
$C_{I(OFF)}$	Power-off leakage current	V_O = 3.0 V or 0, $\overline{OE}$ = V_{CC}		10		pF
r_{on}[3]	On-resistance	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA		5	7	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA		5	7	
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = –15 mA		10	15	
V_P	Pass voltage	V_I = V_{CC} = 5.0 V; I_O = –100 μA	3.4	3.6	3.9	V
I_{UCP}	Undershoot static current protection	V_{CC} = 5.0 V, I_B = 400 μA; $\overline{OE}$ = 5.0 V; $V_B \geq$ 3.0 V		8		mA

NOTES:
1. All typical values are at V_{CC} = 5 V, T_{amb} = 25°C
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

GND = 0 V; t_R; C_L = 50 pF

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
				V_{CC} = +5.0 V ±0.5 V		
				Min	Max	
t_{pd}	Propagation delay[1]	A or B	B or A		.25	ns
t_{en}	Output enable time to High and Low level	$\overline{OE}$	A or B	1.0	5.7	ns
t_{dis}	Output disable time from High and Low level	$\overline{OE}$	A or B	1.0	5.2	ns

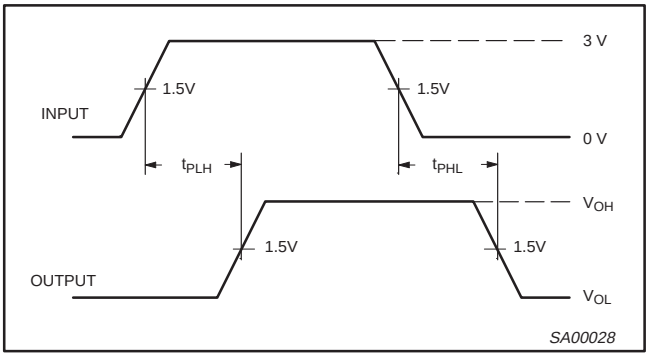
NOTE:
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on–state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

SYMBOL	PARAMETER DESCRIPTION	LIMITS			UNIT
		T_{amb} = –40 °C to +85 °C V_{CC} = 5 V, ±0.5 V			
		MIN.	MEAN	MAX.	
t_{pd}	Propagation delay (see Note 1)			250	ps
t_{PZH}	Output enable time to High level	1.6	3.4	5.6	ns
t_{PHZ}	Output enable time from High level	1.7	3.3	5.5	ns
t_{PZL}	Output enable time to Low level	2.3	4	6	ns
t_{PLZ}	Output enable time from Low level	2.5	4.5	6.6	ns

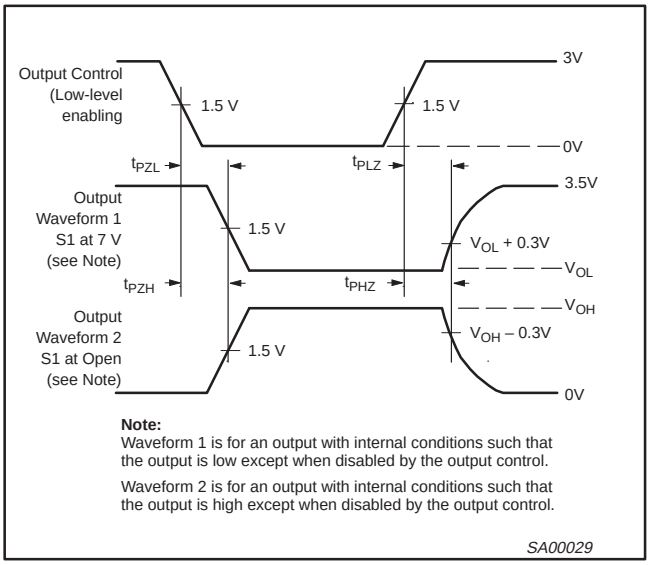
NOTE:
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance); at +25°C.

AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0 V

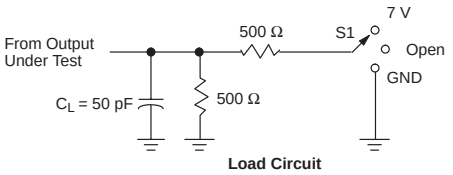


Waveform 1. Input (An) to Output (Yn) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

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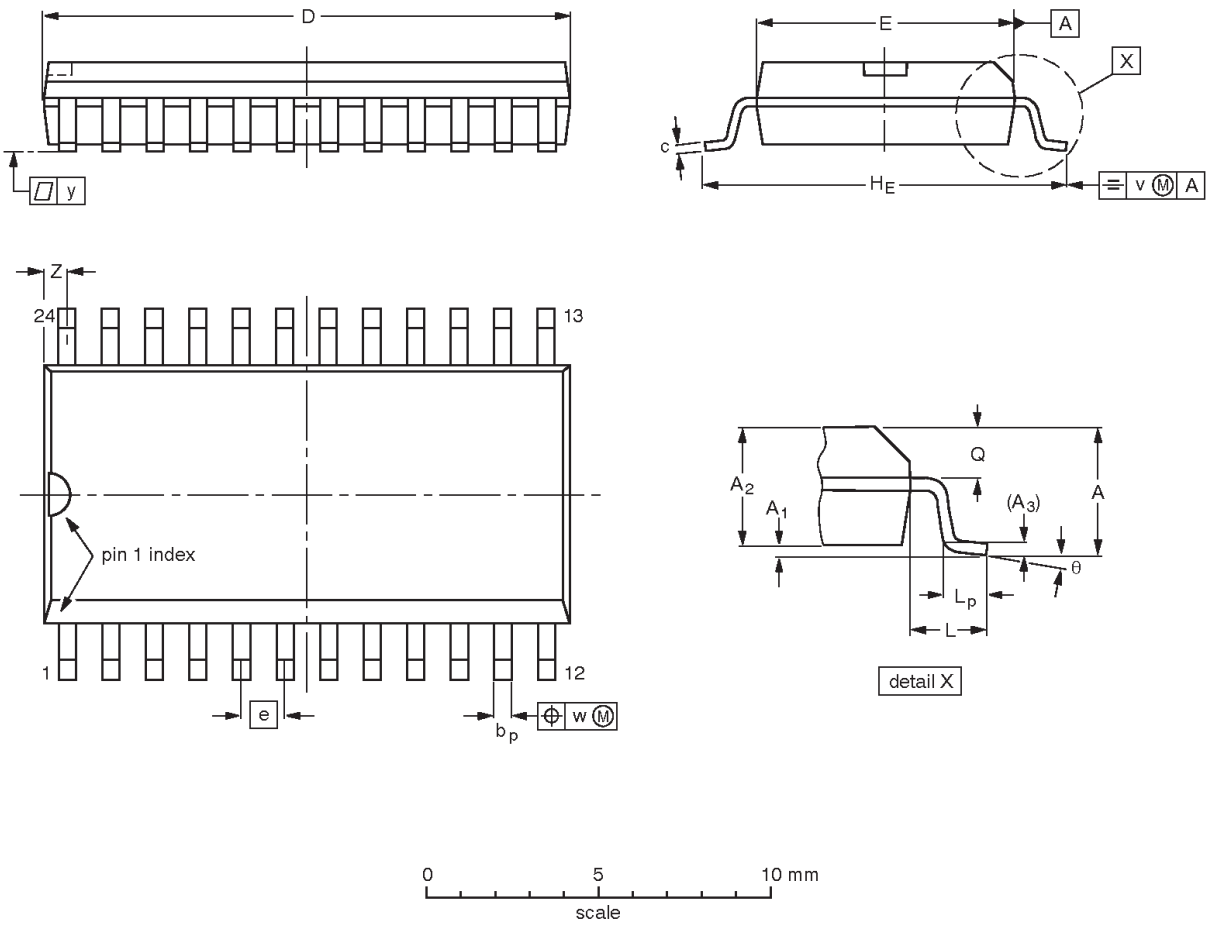
NOTES:

1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
2. The outputs are measured one at a time with one transition per measurement.

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

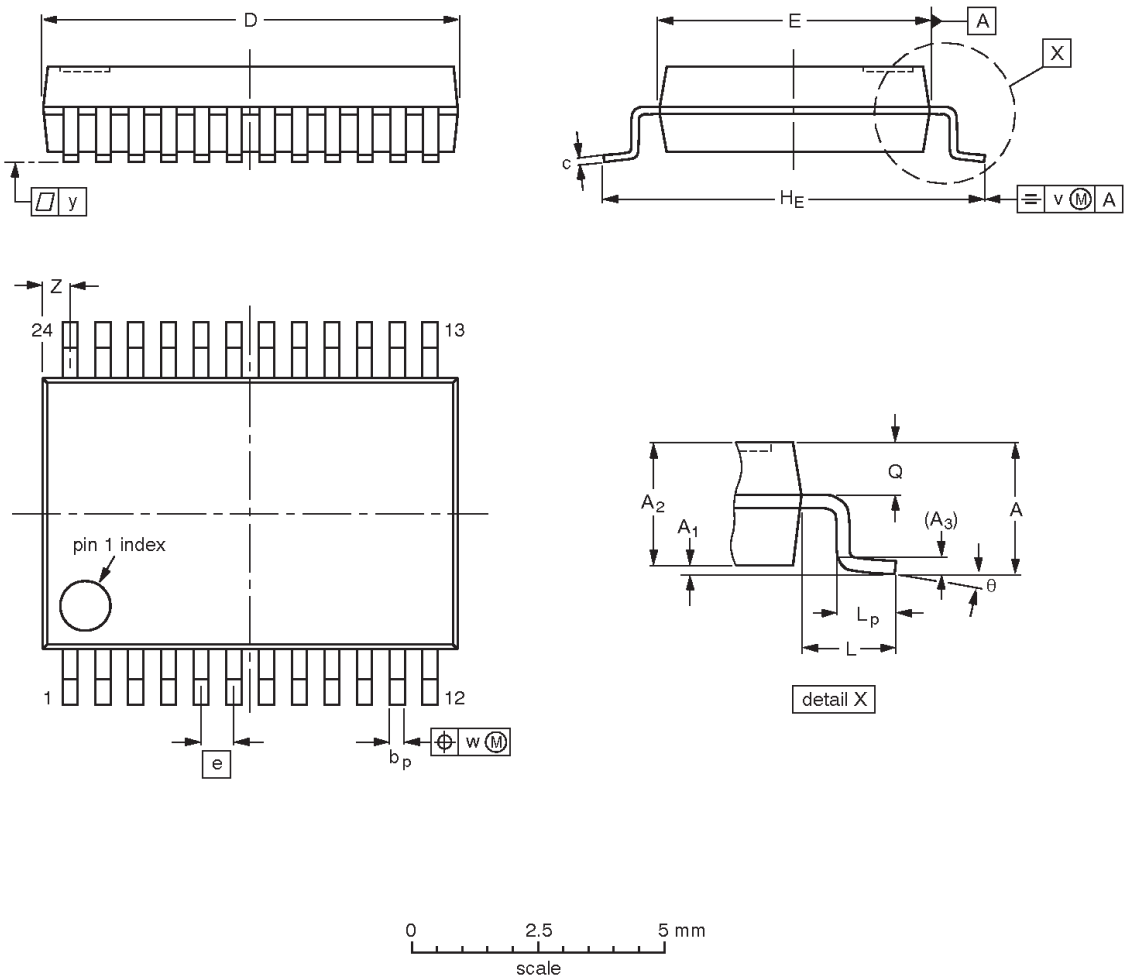
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013				~~97-05-22~~ 99-12-27

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

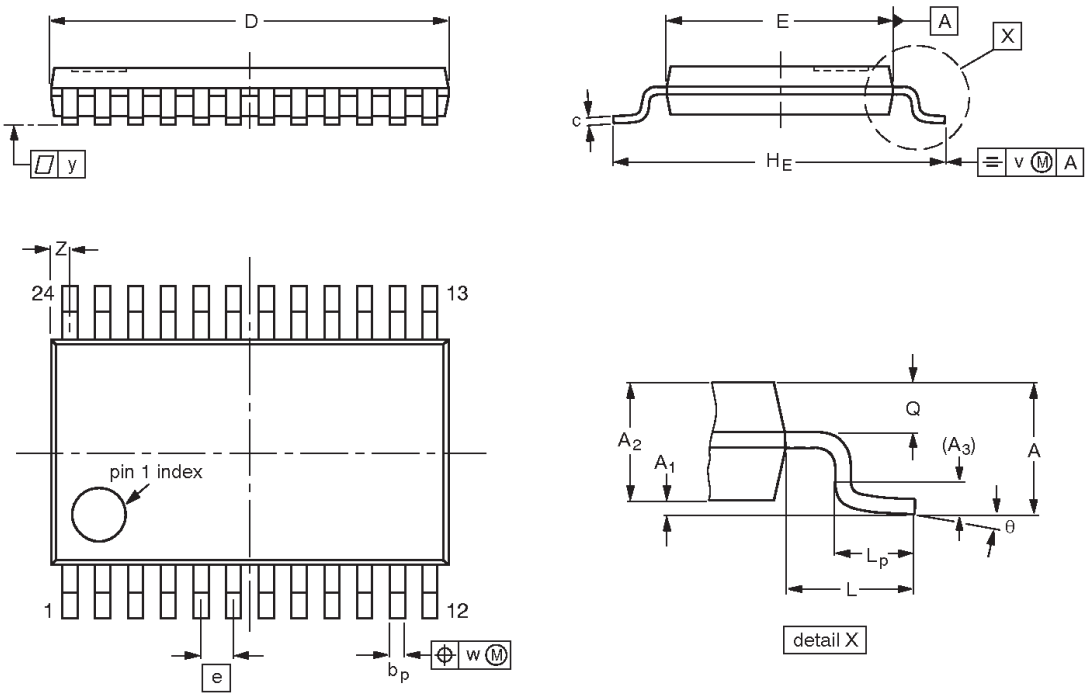
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

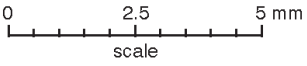
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150				~~95-02-04~~ 99-12-27

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~95-02-04~~ 99-12-27

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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