# Am25LS2518

Quad D Register with Standard and Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

- Low-Power Schottky version of the popular Am2918 and
- · Four standard totem-pole outputs

- · Four three-state outputs
- Four D-type flip-flops
- Second sourced by T. I. as the SN54/74LS388

#### **GENERAL DESCRIPTION**

The Am25LS2518 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

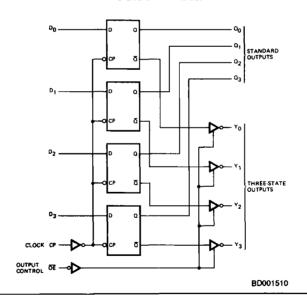
The same data as on the Q outputs is enabled at the threestate Y outputs when the "output control" (OE) input is LOW. When the OE input is HIGH, the Y outputs are in the high-impedance state.

The Am25LS2518 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25LS2518 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

### **BLOCK DIAGRAM**



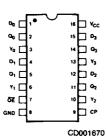
### **RELATED PRODUCTS**

Part No.	Description
Am25S18	Quad D Register
Am2918	Quad D Register
Am29LS18	Quad D Low Power Register
Am29LS2519	Quad D Low Power Register

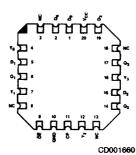
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## CONNECTION DIAGRAM Top View

D-16, P-16

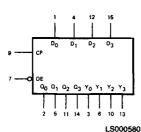


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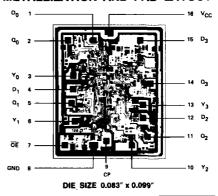


Note: Pin 1 is marked for orientation

### LOGIC SYMBOL

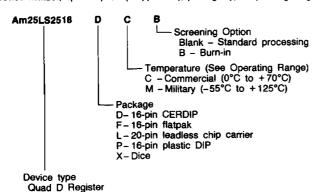


### **METALLIZATION AND PAD LAYOUT**



### **ORDERING INFORMATION**

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations						
Am25LS2518	PC DC, DM FM LC, LM XC, XM					

### Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

### 9

### PIN DESCRIPTION

Pin No.	Name	1/0	Description
	Di	1	The four data inputs to the register.
	Ci	0	The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.
	Yi	0	The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y <sub>i</sub> outputs to the high-impedance state.
9	CP	1	Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.
7	Œ	<u> </u>	Output Control. When the OE input is HIGH, the YI outputs are in the high-impedance state. When the OE input is LOW, the TRUE register data is present at the Yi outputs.

### TRUTH TABLE

	INPUTS		OUT	PUTS	
ŌĔ	CLOCK CP	D	a	Y	NOTES
н	L	×	NC	Z	-
H	н	X	NC	Z Z Z Z	-
H	f +	L	L	Z	_
H	1	н	H	Z	-
L	t	L	L	L	-
L	t	н	н	н	-
L	-	-	L	L	1
L	_	-	Н	н	1

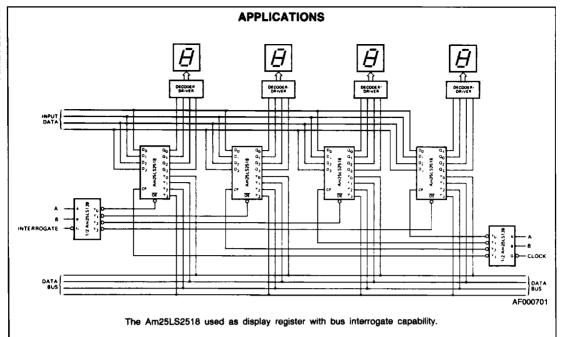
L - LOW

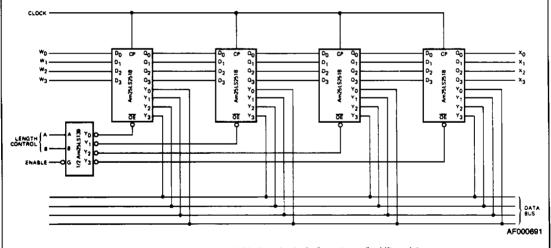
H = HIGH

NC = No change t = LOW-to-HIGH transition Z = High-Impedance

X = Don't care

Note: 1. When OE is LOW, the Y output will be in the same logic state as the Q output.





The Am25LS2518 as a variable length (1, 2, 3 or 4 word) shift register.

### **ABSOLUTE MAXIMUM RATINGS**

Storage Temperature65°C to +150°C
(Ambient) Temperature Under Bias55°C to +125°C
Supply Voltage to Ground Potential
Continuous0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State0.5V to +V <sub>CC</sub> max
DC Input Voltage0.5V to +7.0V
DC Output Current, Into Outputs
DC Input Current30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

### **OPERATING RANGES**

Commercial (C) Devices	
Temperature	0°C to +70°C
Supply Voltage	+4.75V to +5.25V
Military (M) Devices	
Temperature	55°C to +125°C
Supply Voltage	+4.5V to +5.5V
Operating ranges define those limit ality of the device is guaranteed.	's over which the function-

### DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)					Min	Typ (Note 1)	Max	Units
						MIL	2.5	3.4		
	1	Van - MIN	Q.	Q. <sub>IOH</sub> = -660μA		COM'L	2.7	3.4		Volts
VOH	Output HIGH Voltage	V <sub>CC</sub> = MIN V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$\Gamma_{\mathbf{v}}$	MIL, IC	MIL, IOH = -1.0mA		2.4	3.4		
		1	Y		Юн	= - 2.6mA	2.4	3.4		
		•		I <sub>OL</sub> = 4.0	mΑ				0.4	
VOL	VOL Output LOW Voltage	V <sub>CC</sub> = MIN V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		I <sub>OL</sub> = 8.0n	n <b>A</b>				0.45	Volts
		VIN - VIH OF VIL		I <sub>OL</sub> = 12mA				0.5		
V <sub>IH</sub>	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
		Guaranteed inner	Guaranteed input logical LOW MIL		L			0.7		
VIL	V <sub>IL</sub> Input LOW Level		voltage for all inputs. COM'L					0.8	Volts	
VI	Input Clamp Voltage	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18mA				·		-1.5	Volts	
lıL	Input LOW Current	VCC = MAX, VIN	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4V						-0.36	mA
IH	Input HIGH Current	VCC = MAX, VIN	- 2.7	٧					20	μΑ
lı	Input HIGH Current	VCC = MAX, VIN	<b>-</b> 7.0	<u> </u>					0.1	mA
	Off-State (High-Impedance)		V <sub>O</sub> = 0.4V					-20		
loz	Output Current	V <sub>CC</sub> = MAX		V <sub>O</sub> = 2.4V				20	μΑ	
Isc	Output Short Circuit Current (Note 3)	VCC = MAX				-15		-85	mA	
loc	Power Supply Current (Note 4)	V <sub>CC</sub> = MAX					17	28	mA	

- Notes: 1. Typical limits are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading.

  2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.

  3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

  4. I<sub>CC</sub> is measured with all inputs at 4.5V and all outputs open.

### SWITCHING CHARACTERISTICS (TA = +25°C, VCC = 5.0V)

<b>Parameters</b>	Description		Test Conditions	Min	Тур	Max	Unite
ФГН	Clock to Q <sub>i</sub>				18	27	
tens.			] [		18	27	ns
tplH		Otto a marin	1		18	27	
<sup>†</sup> PHL	Clock to Yi	(OE LOW)			18	27	ns
		LOW	C <sub>L</sub> = 15pF	18			
t <sub>pw</sub> Clock Pulse Width	HIGH	RL = 2.0kΩ	R <sub>L</sub> = 2.0kΩ 15			ns	
t <sub>s</sub>	Data			15			ns
th	Data		1	5.0			ns
<sup>t</sup> zH			Ī		7.0	11	
†ZL	OE to Yi				8	12	ns
thz			C <sub>L</sub> = 5.0pF		14	21	
1LZ	ŌE to Yi		R <sub>L</sub> = 2.0kΩ		12	18	ns
fmax	Maximum Clock Fro	equency (Note 1)		35	50		MHz

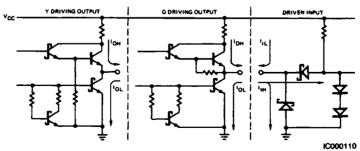
Note 1. Per industry convention, f<sub>max</sub> is the worst case value of the maximum device operating frequency with no constraints on t<sub>f</sub>, t<sub>f</sub>, pulse width or duty cycle.

### SWITCHING CHARACTERISTICS over operating range unless otherwise specified\*

			1 1	COMM	ERCIAL	MILI	TARY		
				Am25	L82518	Am25	LS2518		
Parameters	Parameters Description	Test Conditions	Min	Max	Min	Max	Units		
tplH	1				38		45		
t <sub>PHL</sub>	Clock to Qi		] [		38		45	ns	
tplH			1 [		35		40	ns	
t <sub>PHL</sub>	Clock to Yi (OE LOW)	XV)			35		40		
	Clock Pulse Width	LOW	C <sub>L</sub> = 50pF R <sub>L</sub> = 2.0kΩ	20		20		ns	
1 <sub>pw</sub>		HIGH		20		20			
t <sub>e</sub>	Deta	Philosophia Committee Comm	] [	15		15		ns	
th	Data		1 [	5.0		5.0		ns	
t <sub>ZH</sub>	1		1 [		15		17	]	
t <sub>ZL</sub>	OE to Yi				16		17	ns .	
ЧZ	OE to Yi		C: = 5 0nE	Ct = 5.00F		27		30	
<b>LZ</b>			C <sub>L</sub> = 5.0pF R <sub>L</sub> = 2.0kΩ		24		30	na	
fmex	Maximum Clock Freq	uency (Note 1)	1 Γ	30		25		MHz	

\*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

# Am25LS2518 LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.