Am9312
Eight-Input Multiplexer

01217

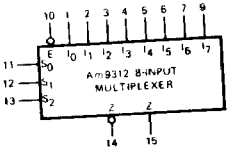
Distinctive Characteristics:

- 10 ns typical propagation delay
- Both true and complement outputs provided
- 100% reliability assurance testing in compliance with MIL-STD-883
- Can be used to generate any function of four variables

FUNCTIONAL DESCRIPTION

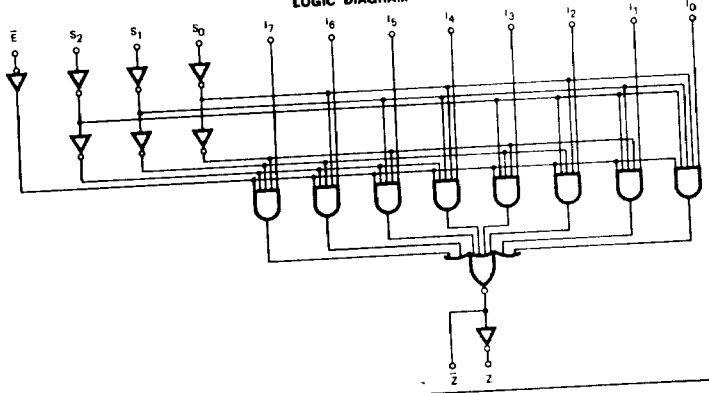
The Am9312 is a high-speed eight-input multiplexer or data selector. A three-bit select code, S_0, S_1, S_2, determines which one of the eight inputs, I_0 through I_7, will be routed through to the outputs. Both true and complement outputs are available; the complement output is slightly faster. An active LOW enable ($\overline{E}$) is provided. When the enable is HIGH, the two outputs go to their inactive levels, with the Z output LOW and the $\overline{Z}$ output HIGH. The device can also be used to generate any logic function of four variables.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



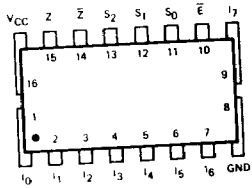
Am9312 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-pin Molded DIP	0°C to +75°C	U6M931259X
16-pin Hermetic DIP	0°C to +75°C	U7B931259X
16-pin Hermetic DIP	−55°C to +125°C	U7B9312 51X
16-pin Hermetic Flat Pak	−55°C to +125°C	U4L931251X
Dice	Note	UXX9312XXD

Revised Ordering Information
See Section 9

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125° temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM R GS (Above which the useful life may be impaired)

Storage Tempe	
Temperature (Ambient) Under Bias	−65°C to +15
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−55°C to + 12
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +7
DC Input Voltage	−0.5 V to +V_{CC} m
Output Current, Into Outputs	−0.5 V to +5.5
DC Input Current	30 m
	−30 mA to +5.0 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93125 0X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am93125 1X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−1.0	−1.6	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−35		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		27	44	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

(V_{CC} = 5.0 V, C_L = 15 pF (Refer to table for test conditions)

		Min	Typ	Max	Units
t_{pd}^+(ST)	Turn Off Delay—Select Input to TRUE Output	12	23	34	ns
t_{pd}^-(ST)	Turn On Delay—Select Input to TRUE Output	13	25	34	ns
t_{pd}^+(SF)	Turn Off Delay—Select Input to FALSE Output	9	18	24	ns
t_{pd}^-(SF)	Turn On Delay—Select Input to FALSE Output	9	18	26	ns
t_{pd}^+(DT)	Turn Off Delay—Data Input to TRUE Output	9	16	24	ns
t_{pd}^-(DT)	Turn On Delay—Data Input to TRUE Output	9	16	24	ns
t_{pd}^+(DF)	Turn Off Delay—Data Input to FALSE Output	3	9	14	ns
t_{pd}^-(DF)	Turn On Delay—Data Input to FALSE Output	4	10	16	ns
t_{pd}^+($\overline{ET}$)	Turn Off Delay—Enable Input to TRUE Output	11	23	30	ns
t_{pd}^-($\overline{ET}$)	Turn On Delay—Enable Input to TRUE Output	10	22	31	ns
t_{pd}^+($\overline{EF}$)	Turn Off Delay—Enable Input to FALSE Output	6	14	20	ns
t_{pd}^-($\overline{EF}$)	Turn On Delay—Enable Input to FALSE Output	6	16	23	ns

...ON OF TERMS

...SCRIPT TERMS:

...IGH, applying to a HIGH-signal level or when used with V_{CC} ...dicate HIGH V_{CC} value.

...put.

...OW, applying to a LOW signal level or when used with V_{CC} ...dicate LOW V_{CC} value.

...utput.

...CTIONAL TERMS:

...le Input ($\overline{E}$) Is active LOW to enable data selection from ... of eight data inputs. Enable input HIGH inhibits all data ...ce selection. Refer to Truth Table.

...Out The logic HIGH or LOW output drive capability in terms ...put Unit Loads.

...ata Inputs designates one of the eight multiplexer data inputs ..., 7.

...load One T^2L gate input load. In the HIGH state it is equal to ... at 2.4V and in the LOW state it is equal to −1.6mA at 0.4V.

...utput The logic TRUE output of the multiplexer.

...utput The complement of the Z output.

...RATIONAL TERMS:

Output HIGH current, forced out of output in V_{OH} test.

Output LOW current, forced into the output in V_{OL} test.

The current drawn by the device under a +5.0 V power supply with input and output terminals open.

...tive Current Current flowing out of the device.

...tive Current Current flowing into the device.

Minimum logic HIGH input voltage.

Maximum logic LOW input voltage.

Minimum logic HIGH output voltage with output HIGH current ...owing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level).

t_{pd+}**(ST)** The propagation delay from a Select Input signal transition to the corresponding TRUE output LOW-HIGH transition.

t_{pd-}**(ST)** The propagation delay from a Select Input signal transition to the corresponding TRUE output HIGH-LOW transition.

t_{pd+}**(SF)** The propagation delay from a Select Input signal transition to the corresponding FALSE output LOW-HIGH transition.

t_{pd-}**(SF)** The propagation delay from a Select Input signal transition to the corresponding FALSE output HIGH-LOW transition.

t_{pd+}**(DT)** The propagation delay from a Data Input signal transition to the TRUE output LOW-HIGH transition.

t_{pd-}**(DT)** The propagation delay from a Data Input signal transition to the TRUE output HIGH-LOW transition.

t_{pd+}**(DF)** The propagation delay from a Data Input signal transition to the FALSE output LOW-HIGH transition.

t_{pd-}**(DF)** The propagation delay from a Data Input signal transition to the FALSE output HIGH-LOW transition.

$t_{pd+}(\overline{ET})$ The propagation delay from an Enable Input signal transition to the TRUE output LOW-HIGH transition.

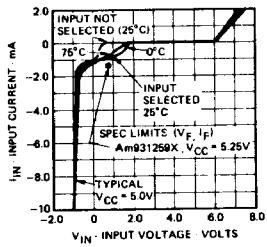
$t_{pd-}(\overline{ET})$ The propagation delay from an Enable Input signal transition to the TRUE output HIGH-LOW transition.

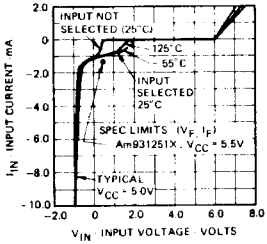
$t_{pd+}(\overline{EF})$ The propagation delay from an Enable Input signal transition to the FALSE output LOW-HIGH transition.

$t_{pd-}(\overline{EF})$ The propagation delay from an Enable Input signal transition to the FALSE output HIGH-LOW transition.

PERFORMANCE CURVES

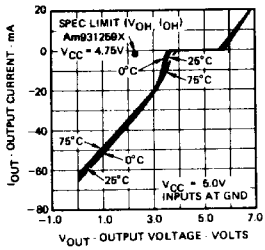
...put Characteristics

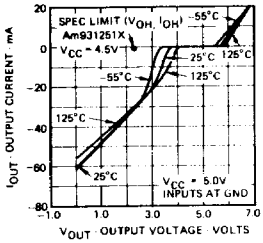




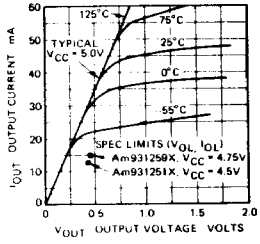
...utput Characteristics

HIGH





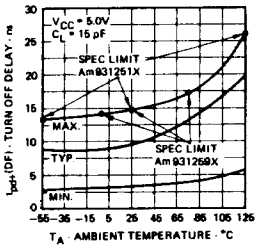
LOW



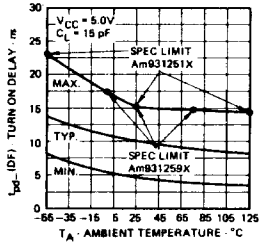
PERFORMANCE CURVES

Switching Characteristics

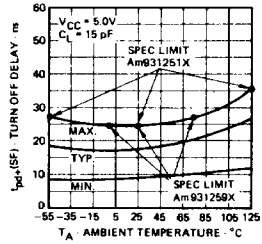
Turn Off Delay
Data Input to FALSE Output



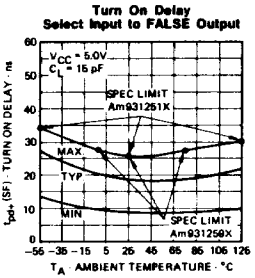
Turn On Delay
Data Input to FALSE Output



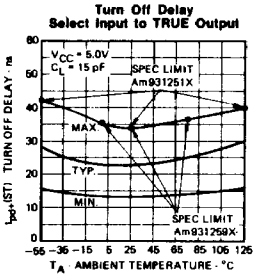
Turn Off Delay
Select Input to FALSE Output



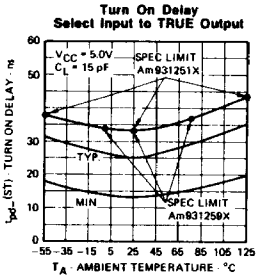
Turn On Delay
Select Input to FALSE Output



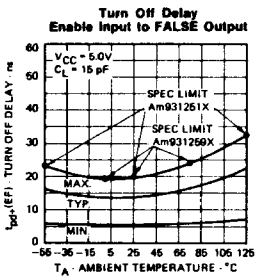
Turn Off Delay
Select Input to TRUE Output



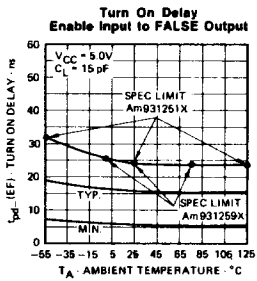
Turn On Delay
Select Input to TRUE Output



Turn Off Delay
Enable Input to FALSE Output



Turn On Delay
Enable Input to FALSE Output



MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TRUTH TABLE

Inputs											Outputs	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$(F) Z
H	X	X	X	X	X	X	X	X	X	X	X	H L
L	L	L	L	L	X	X	X	X	X	X	X	H L
L	L	L	L	H	X	X	X	X	X	X	X	L H
L	L	L	H	X	L	X	X	X	X	X	X	H L
L	L	L	H	X	H	X	X	X	X	X	X	L H
L	L	H	L	X	X	L	X	X	X	X	X	H L
L	L	H	L	X	X	H	X	X	X	X	X	L H
L	L	H	H	X	X	X	L	X	X	X	X	H L
L	L	H	H	X	X	X	H	X	X	X	X	L H
L	H	L	L	X	X	X	X	L	X	X	X	H L
L	H	L	L	X	X	X	X	H	X	X	X	L H
L	H	L	H	X	X	X	X	X	L	X	X	H L
L	H	L	H	X	X	X	X	X	H	X	X	L H
L	H	H	L	X	X	X	X	X	X	L	X	H L
L	H	H	L	X	X	X	X	X	X	H	X	L H
L	H	H	H	X	X	X	X	X	X	X	L	H L
L	H	H	H	X	X	X	X	X	X	X	H	L H

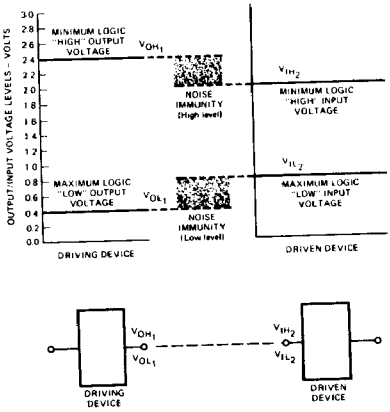
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care

Am9312 LOADING RULES

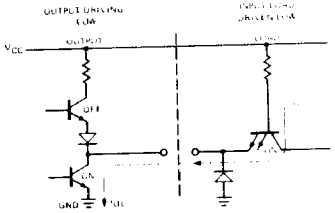
Input/Output	Pin No.s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
I_0	1	1	—	—
I_1	2	1	—	—
I_2	3	1	—	—
I_3	4	1	—	—
I_4	5	1	—	—
I_5	6	1	—	—
I_6	7	1	—	—
GND	8	—	—	—
I_7	9	1	—	—
$\overline{E}$	10	1	—	—
S_0	11	1	—	—
S_1	12	1	—	—
S_2	13	1	—	—
$\overline{Z}$	14	—	20	10
Z	15	—	20	10
V_{CC}	16	—	—	—

INPUT/OUTPUT INTERFACE CONDITIONS

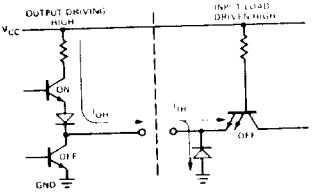
Voltage Interface Conditions — LOW & HIGH



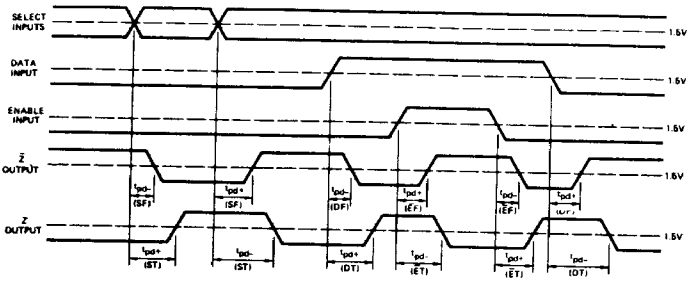
Current Interface Conditions — LOW



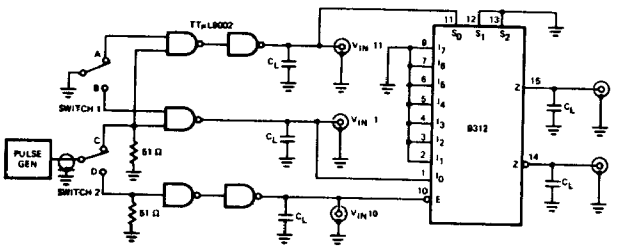
Current Interface Conditions — HIGH



SWITCHING TIME WAVEFORMS



SWITCHING TIME TEST CIRCUIT

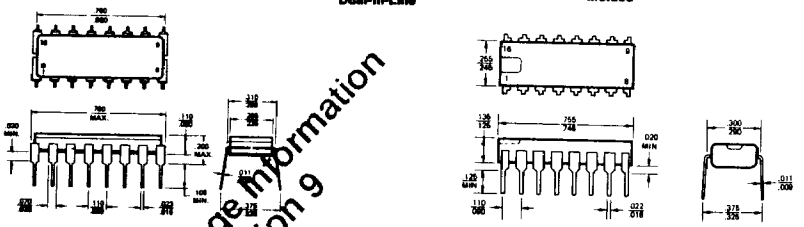


Switching Measurement Connection Table

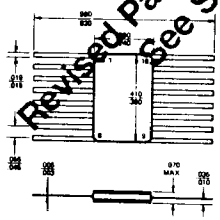
	$t_{pd}\pm$(DT) $t_{pd}\pm$(DF)	$t_{pd}\pm$(ST) $t_{pd}\pm$(SF)	$t_{pd}\pm(\overline{ET})$ $t_{pd}\pm(\overline{EF})$
Switch 1	A	B	B
Switch 2	C	C	D

PHYSICAL DIMENSIONS

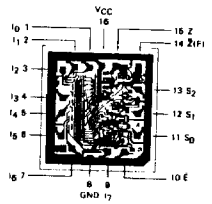
Hermetic — **Dual-In-Line** — **Molded**



Flat Package



Metallization and Pad Layout



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TELEX: 34-6306

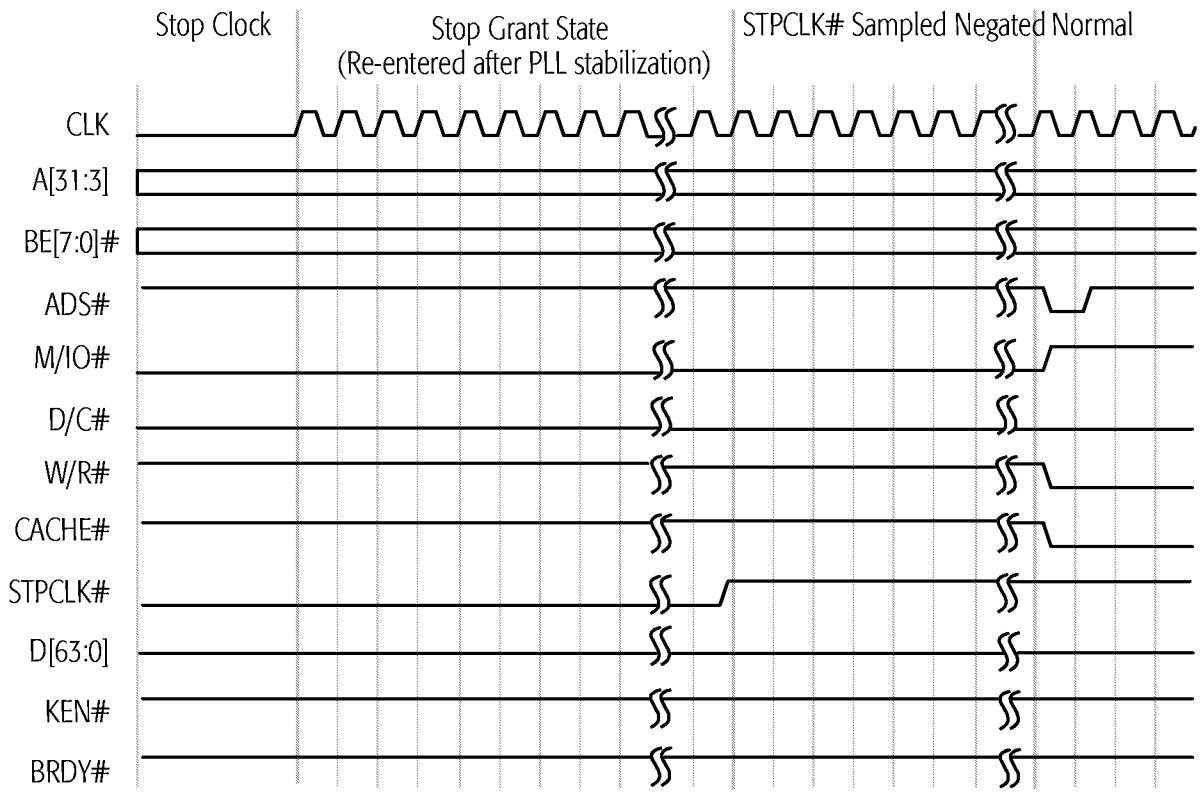

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

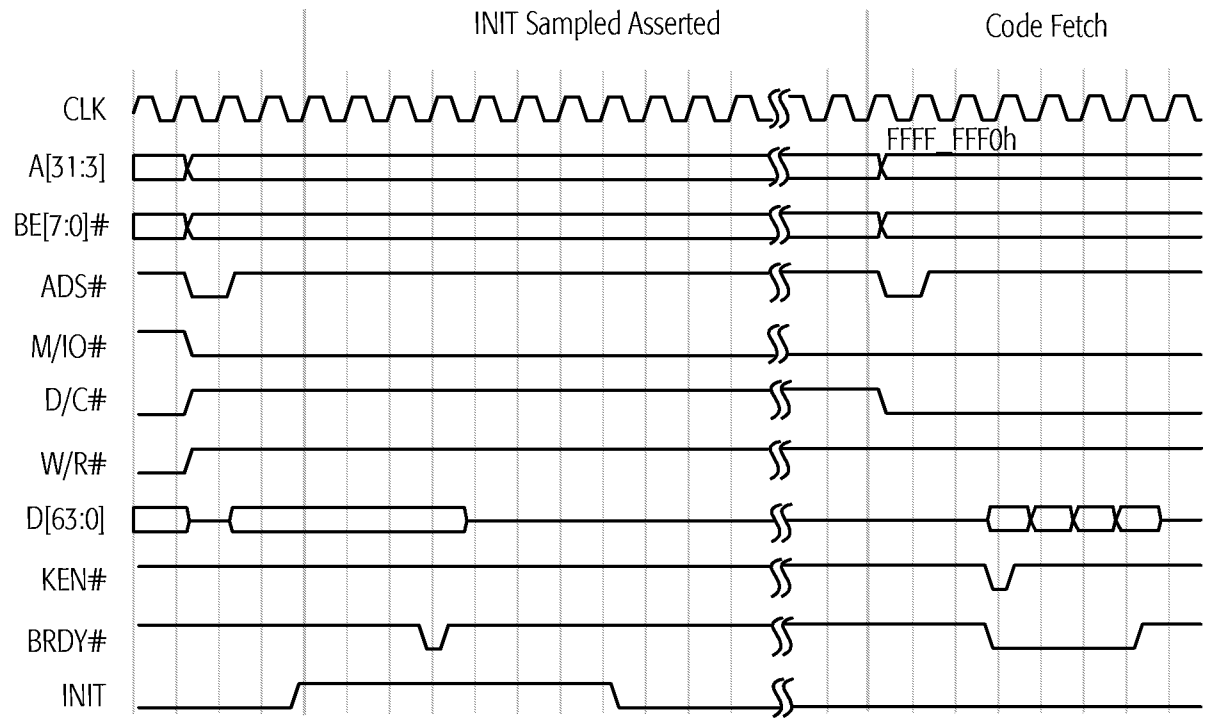

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.