# LOW SKEW, 1-TO-4 DIFFERENTIAL-TO-LVDS FANOUT BUFFER W/INTERNAL TERMINATION

ICS889833

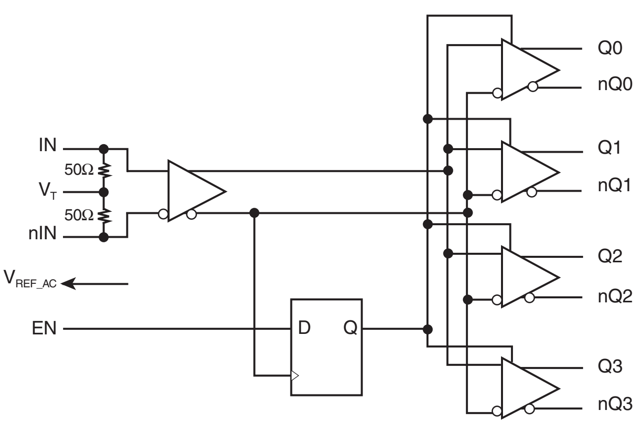
## General Description

The ICS889833 is a high speed 1-to-4 Differential-to-LVDS Fanout Buffer w/Internal Termination and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. The ICS889833 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and $V_{REF\_AC}$ pin allow other differential signal families such as LVPECL, LVDS, and CML to be easily interfaced to the input with minimal use of external components. The device also has an output enable pin which may be useful for system test and debug purposes. The ICS889833 is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

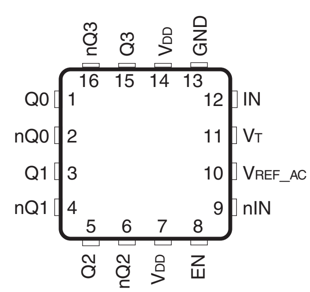
## Features

- Four differential LVDS outputs
- IN, nIN input pair can accept the following differential input levels: LVPECL, LVDS, CML
- Output frequency: >2GHz
- Cycle-to-cycle jitter, RMS: 0.2ps (maximum)
- Additive phase jitter, RMS: 0.04ps (typical)
- Total jitter: 10ps (maximum)
- Output skew: 40ps (maximum)
- Part-to-part skew: 200ps (maximum)
- Propagation delay: 520ps (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## Block Diagram




## Pin Assignment




**ICS889833**
**16-Lead VFQFN**
3mm x 3mm x 0.95 package body
**K Package**
Top View

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2 | Q0, nQ0 | Output | | Differential output pair. Normally terminated with 100Ω across the pair. Unused outputs must be terminated with 100Ω across the pin (Q0/nQ0). LVDS interface levels. |
| 3, 4 | Q1, nQ1 | Output | | Differential output pair. Normally terminated with 100Ω across the pair. Unused outputs must be terminated with 100Ω across the pin (Q1/nQ1). LVDS interface levels. |
| 5, 6 | Q2, nQ2 | Output | | Differential output pair. Normally terminated with 100Ω across the pair. Unused outputs must be terminated with 100Ω across the pin (Q2/nQ2). LVDS interface levels. |
| 7, 14 | $V_{DD}$ | Power | | Positive supply pins. |
| 8 | EN | Input | Pullup | Synchronizing output enable pin. When LOW, enables/disables outputs. When HIGH, enables outputs when left open. Internally connected to a 37kΩ pull-up resistor. LVTTL / LVCMOS interface levels. |
| 9 | nIN | Input | | Inverting differential LVPECL clock input. $R_T$ = 50Ω termination to $V_T$. |
| 10 | $V_{REF\_AC}$ | Output | | Reference voltage for AC-coupled applications. Equal to $V_{DD}$ - 1.4V (approx.). Maximum sink/source current is 0.5mA. |
| 11 | $V_T$ | Input | | Input termination center-tap. Each side of the differential input pair terminates to a $V_T$ pin. The $V_T$ pins provide a center-tap to a termination network for maximum interface flexibility. |
| 12 | IN | Input | | Non-inverting LVPECL differential clock input. $R_T$ = 50Ω termination to $V_T$. |
| 13 | GND | Power | | Power supply ground. |
| 14, 15 | Q3, nQ3 | Output | | Differential output pair. Normally terminated with 100Ω across the pair. Unused outputs must be terminated with 100Ω across the pin (Q3nQ3). LVDS interface levels. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $R_{PULLUP}$ | Input Pullup Resistor | | | 37 | | kΩ |

**TABLE 3. CONTROL INPUT FUNCTION TABLE**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| IN | nIN | EN | Q0:Q3 | nQ0:nQ3 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| X | X | 0 | 0 (NOTE 1) | 1 (NOTE 1) |

NOTE 1: On the next negative transition of the input signal (IN).

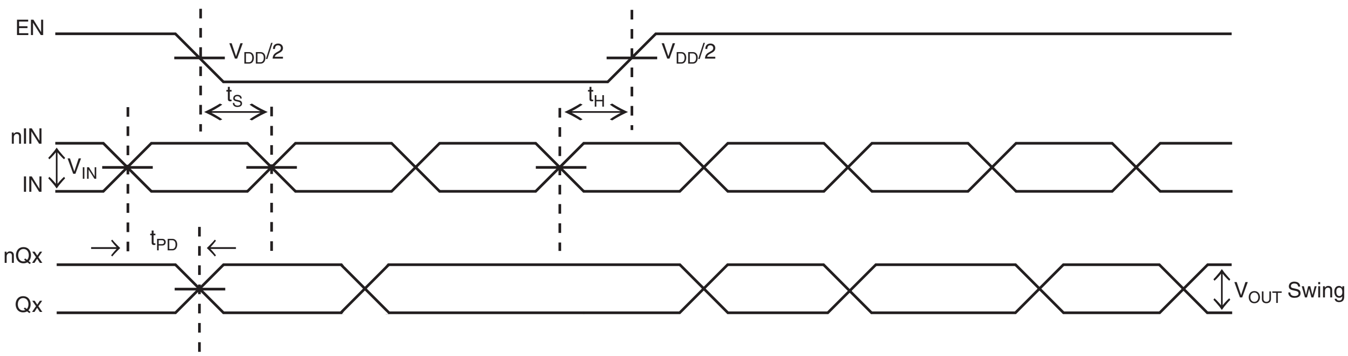



**FIGURE 1. EN TIMING DIAGRAM**

## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5 V |
| Outputs, $I_O$ (LVDS) | |
| Continuous Current | 10mA |
| Surge Current | 15mA |
| Input Current, IN, nIN | ±50mA |
| $V_T$ Current, $I_{VT}$ | ±100mA |
| Input Sink/Source, $I_{REF\_AC}$ | ±0.5mA |
| Operating Temperature Range, TA | -40°C to +85°C |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |
| Package Thermal Impedance, $\theta_{JA}$ (Junction-to-Ambient) | 90.2°C/W (0 lfpm) |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**Table 4A. Power Supply DC Characteristics,** $V_{DD}$ = 3.3V±0.3V; TA = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| $I_{DD}$ | Power Supply Current | | | | 100 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{DD}$ = 3.3V±0.3V; TA = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | $V_{DD} = V_{IN}$ = 3.6V | -125 | | 30 | µA |
| $I_{IL}$ | Input Low Current | $V_{DD}$ = 3.6V, $V_{IN}$ = 0V | | | -300 | µA |

NOTE: Specs are design targets unless otherwise noted.

**Table 4C. DC Characteristics,** $V_{DD}$ = 3.3V±0.3V; TA = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $R_{DIFF\_IN}$ | Differential Input Resistance | (IN, nIN) | | 80 | 100 | 120 | Ω |
| $R_{IN}$ | Input Resistance | | IN-to-VT | 40 | 50 | 60 | Ω |
| $V_{IH}$ | Input High Voltage | (IN, nIN) | | 1.2 | | $V_{DD}$ | V |
| $V_{IL}$ | Input Low Voltage | (IN, nIN) | | 0 | | $V_{DD}$ - 0.15 | V |
| $V_{IN}$ | Input Voltage Swing | | | 0.15 | | 1.7 | V |
| $V_{DIFF\_IN}$ | Differential Input Voltage Swing | | | 0.3 | | | V |
| $V_{REF\_AC}$ | Bias Voltage | | | $V_{DD}$ - 1.45 | $V_{DD}$ - 1.35 | $V_{DD}$ - 1.25 | V |

**Table 4C. LVDS DC Characteristics,** $V_{DD}$ = 3.3V±0.3V; TA = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 250 | 325 | | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | 500 | 650 | | V |
| $V_{OS}$ | Offset Voltage | | 1.15 | 1.35 | 1.55 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

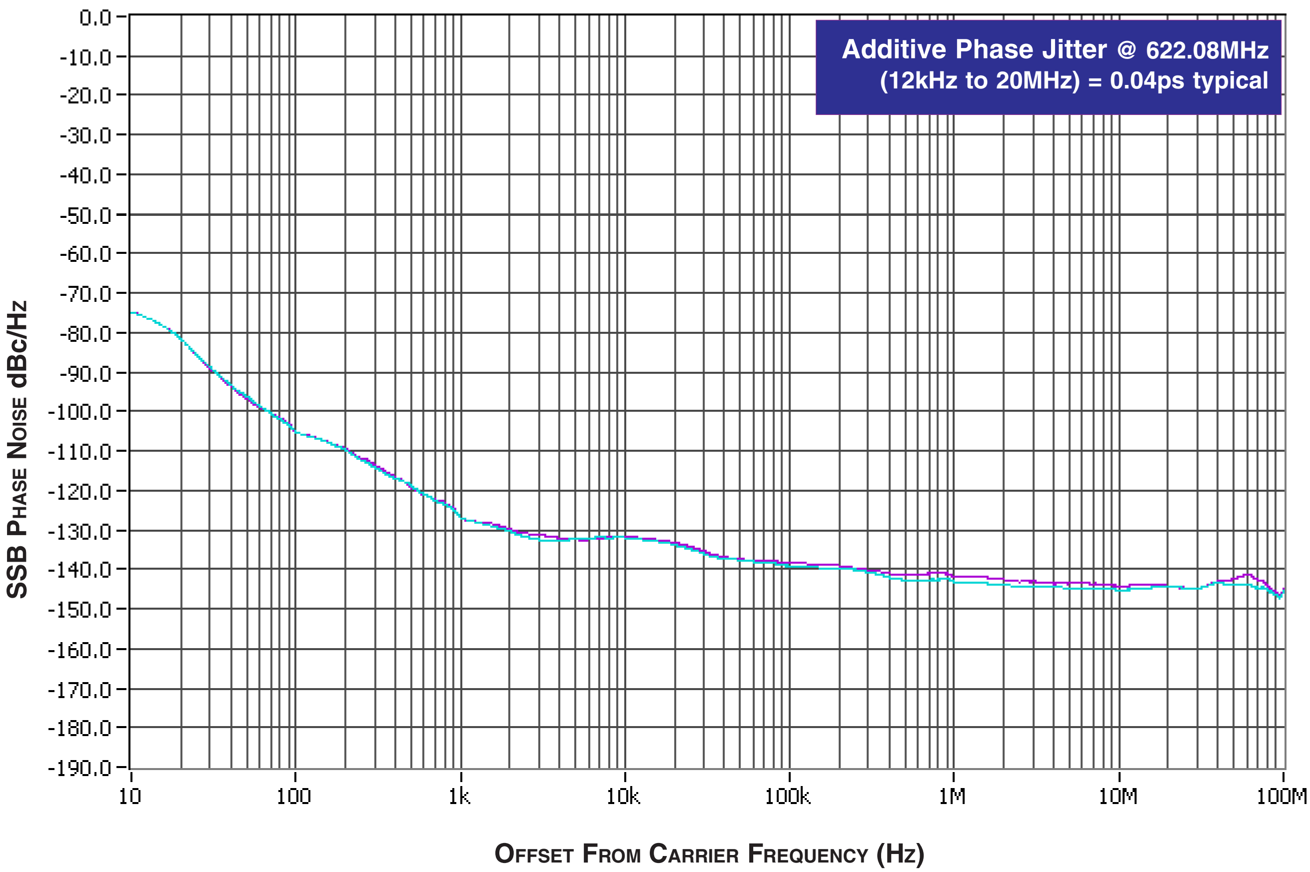
**Table 5. AC Characteristics,** $V_{DD}$ = 3.3V±0.3V; TA = -40°C to 85°C

| Symbol | Parameter | | Condition | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Output Frequency | | | 2.0 | | | GHz |
| $t_{PD}$ | Propagation Delay, (Differential); NOTE 1 | IN to Qx | | 300 | | 520 | ps |
| *t*sk(o) | Output Skew; NOTE 2, 3 | | | | | 40 | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | | 200 | ps |
| *tjit* (cc) | Cycle-to-Cycle Jitter, RMS; NOTE 5 | | | | | 0.2 | ps |
| *tjit* | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section | | 622.08MHz, Integration Range: 12kHz - 20MHz | | 0.04 | | ps |
| *tjit* (j) | Total Jitter; NOTE 5 | | | | | 10 | ps |
| *tjit* (rj) | Random Jitter; NOTE 5 | | | | | 1 | ps |
| *tjit* (tj) | Deterministic Jitter; NOTE 5 | | | | | 2 | ps |
| $t_S$ | Setup Time | EN to IN/nIN | | 300 | | | ps |
| $t_H$ | Hold Time | EN to IN/nIN | | 500 | | | ps |
| $t_R/t_F$ | Output Rise/Fall Time; NOTE 5 | | 20% - 80% | 100 | | 220 | ps |

All parameters characterized at ≤ 1.4GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: Tested at $f \leq$ 750MHz.

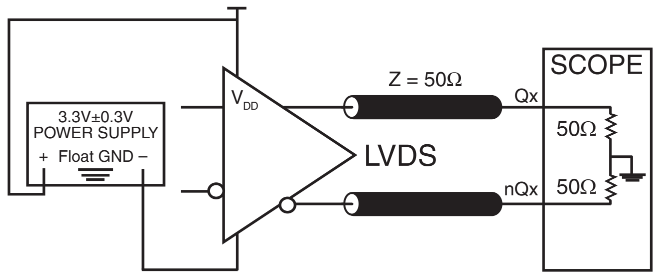
# Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

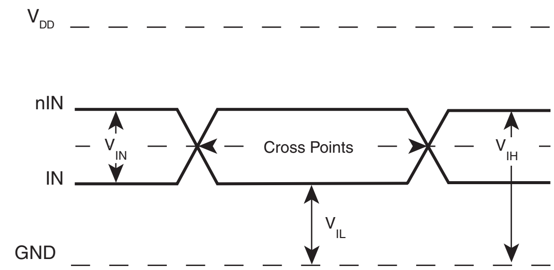



As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

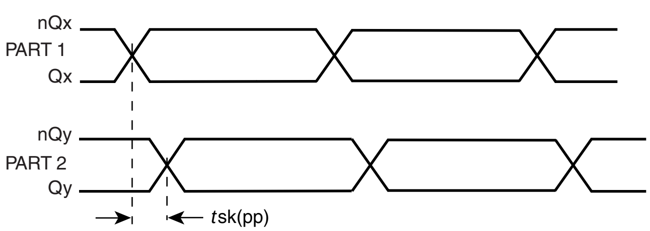
# Parameter Measurement Information



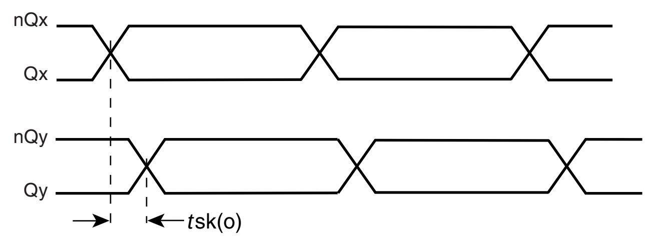

**Output Load AC Test Circuit**



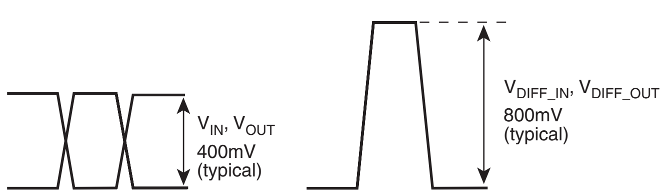

**Differential Input Level**



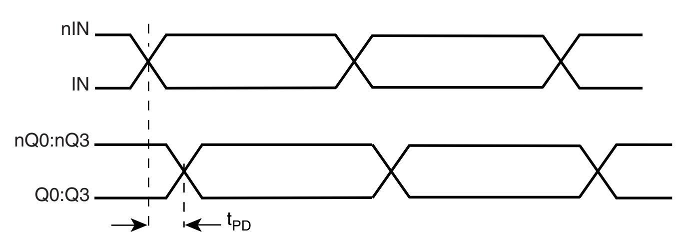

**Part-to-Part Skew**



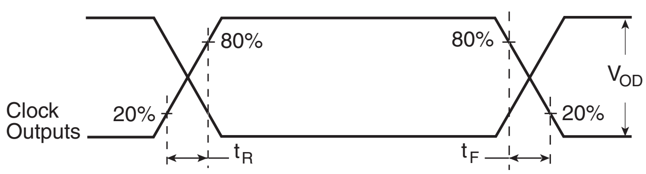

**Output Skew**



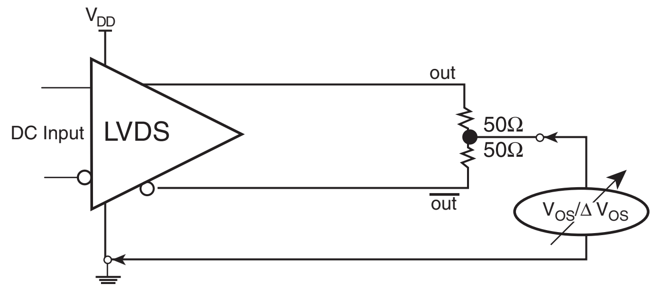

**Single Ended & Differential Input Voltage Swing**



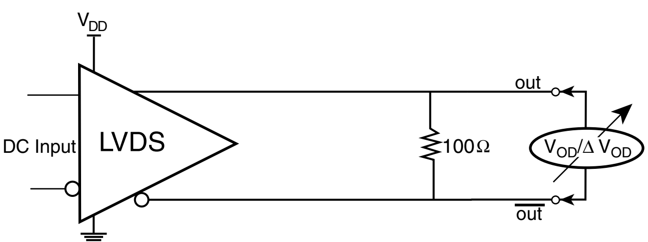

**Propagation Delay**




**OUTPUT RISE/FALL TIME**




**OFFSET VOLTAGE SETUP**




**DIFFERENTIAL OUTPUT VOLTAGE SETUP**

# Application Information

## LVPECL Input with Built-In 50Ω Terminations Interface

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, CML and other differential signals. The signal must meet the $V_{IN}$ and $V_{IH}$ input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

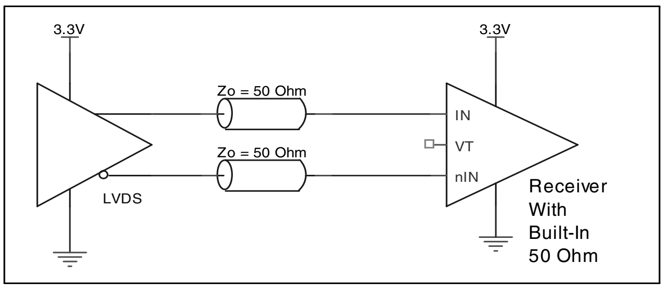



**Figure 2A. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by an LVDS Driver**

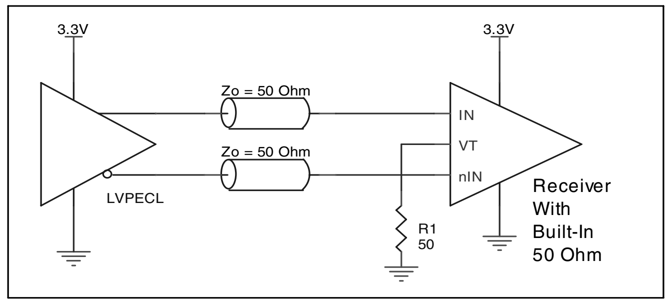



**Figure 2B. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by an LVPECL Driver**

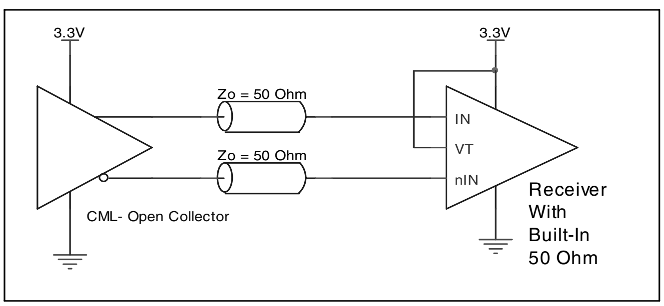



**Figure 2C. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by a CML Driver with Open Collector**

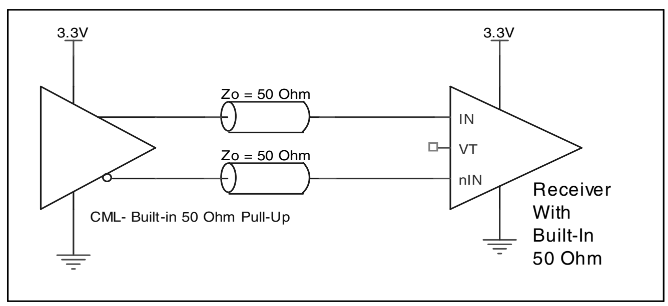



**Figure 2D. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by a CML Driver with Built-In 50Ω Pullup**

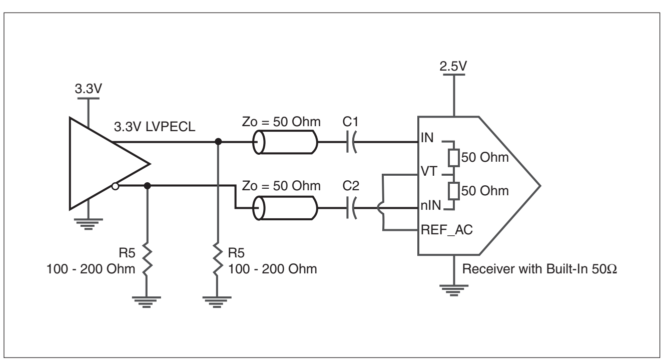



**Figure 2E. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by a 3.3V LVPECL Driver**

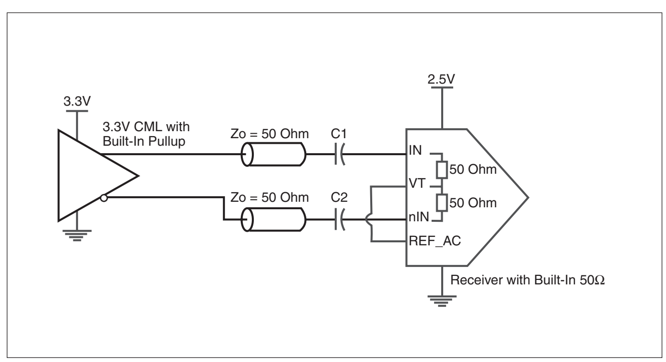



**Figure 2F. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by a 3.3V CML Driver with Built-In Pullup**

## Recommendations for Unused Input and Output Pins

### Inputs:

**LVCMOS Select Pins:**
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

**LVDS Output**
All unused LVDS output pairs must be terminated with 100Ω across.

## 3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

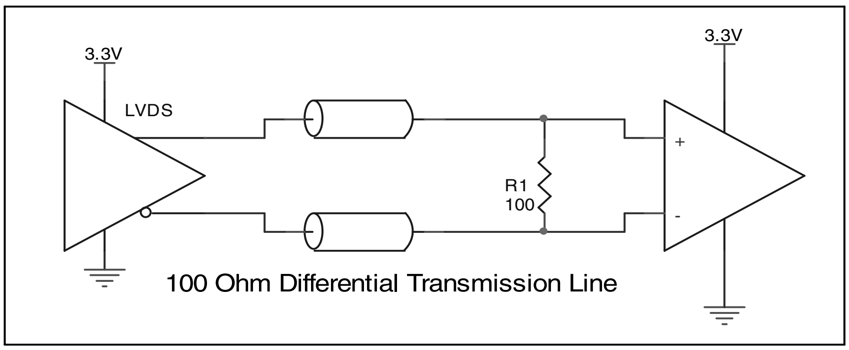



**Figure 3. Typical LVDS Driver Termination**

## Thermal Release Path

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through solder as shown in *Figure 4.* For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

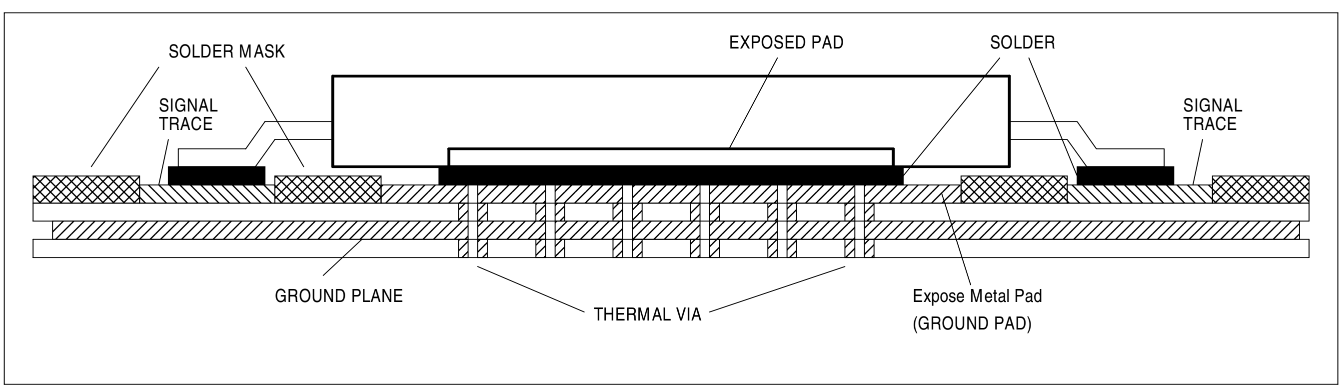



**Figure 4. P.C. Board for Exposed Pad Thermal Release Path Example**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS889833. Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the ICS889833 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD}$ = 3.3V + 0.3V = 3.6V, which gives worst case results.

- $Power\_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.6V * 100mA = **360mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 78.8°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.360W * 78.8°C/W = 113.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**Table 6. Thermal Resistance $\theta_{JA}$ for 16-Pin VFQFN, Forced Convection**

| $\theta_{JA}$ vs. 0 Air Flow (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 90.2°C/W | 78.8°C/W | 70.7°C/W |

# Reliability Information

**Table 7. $\theta_{JA}$ vs. Air Flow Table for 16 Lead VFQFN**

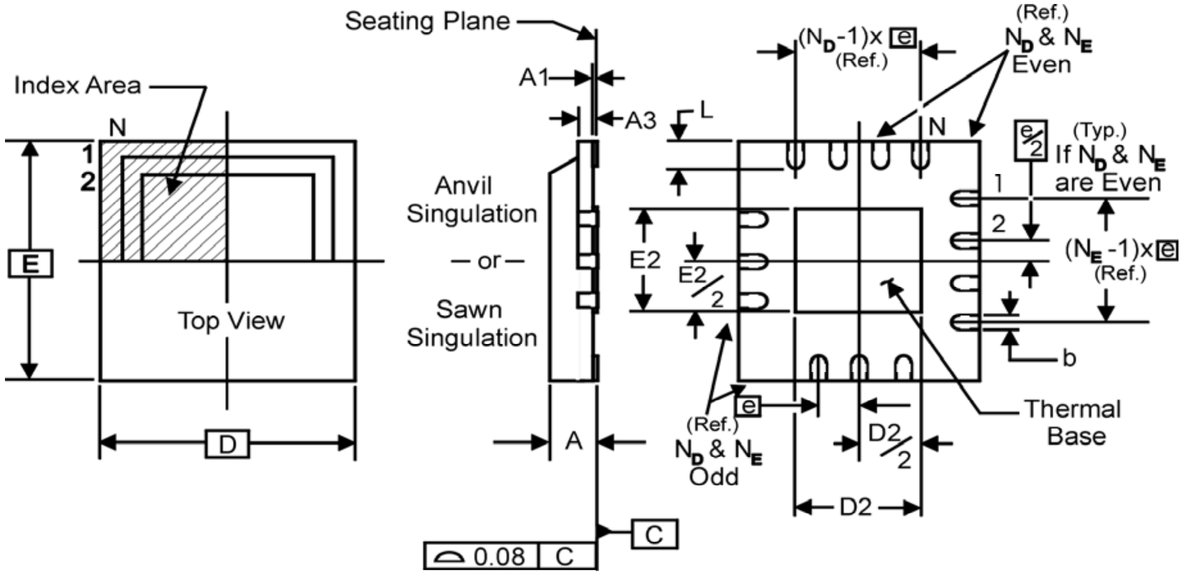
| $\theta_{JA}$ vs. 0 Air Flow (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 90.2°C/W | 78.8°C/W | 70.7°C/W |

**Transistor Count**

The transistor count for ICS889833 is: 181

Pin compatible with SY89833L

## Package Outline - K Suffix for 16 Lead VFQFN




### Table 8. Package Dimensions

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | |
|---|---|---|
| **SYMBOL** | **MINIMUM** | **MAXIMUM** |
| **N** | 16 | |
| **A** | 0.80 | 1.0 |
| **A1** | 0 | 0.05 |
| **A3** | 0.25 Reference | |
| **b** | 0.18 | 0.30 |
| **e** | 0.50 BASIC | |
| **$N_D$** | 4 | |
| **$N_E$** | 4 | |
| **D** | 3.0 | |
| **D2** | 1.0 | 1.8 |
| **E** | 3.0 | |
| **E2** | 1.0 | 1.8 |
| **L** | 0.30 | 0.50 |

Reference Document: JEDEC Publication 95, MO-220

### TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| ICS889833AK | 833A | 16 Lead VFQFN | tube | -40°C to 85°C |
| ICS889833AKT | 833A | 16 Lead VFQFN | 2500 tape & reel | -40°C to 85°C |
| ICS889833AKLF | 33AL | 16 Lead "Lead-Free" VFQFN | tube | -40°C to 85°C |
| ICS889833AKLFT | 33AL | 16 Lead "Lead-Free" VFQFN | 2500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

**For Sales**
800-345-7015
408-284-8200
Fax: 408-284-2775

**For Tech Support**
netcom@idt.com
480-763-2056

**Corporate Headquarters**
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

**Asia Pacific and Japan**
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

**Europe**
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851