Transceivers

74ALS620A/74ALS620A-1
74ALS623A/74ALS623A-1

74ALS620A/74ALS620A-1 Octal bus transceiver, inverting (3-State)
74ALS623A/74ALS623A-1 Octal bus transceiver, non-inverting (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- The -1 version sinks 48mA I_{OL} within the +5% V_{CC} range

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS620A/620A-1	4.0ns	33mA
74ALS623A/623A-1	4.0ns	38mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE: COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	DRAWING NUMBER
20-pin plastic DIP	74ALS620AN, 74ALS620A-1N 74ALS623AN, 74ALS623A-1N	SOT146-1
20-pin plastic SOL	74ALS620AD, 74ALS620A-1D 74ALS623AD, 74ALS623A-1D	SOT163-1

DESCRIPTION

The 74ALS620A and 74ALS623A are octal transceiver featuring 3-State bus compatible outputs in both transmit and receive directions. The 74ALS620A is an inverting version of the 74ALS623A. The outputs are capable of sinking 24mA and sourcing up to 15mA, providing very good capacitive drive characteristics.

The outputs for the 74ALS620A-1 and 74ALS623A are capable of sinking up to 48mA when within the ±5% V_{CC} range.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

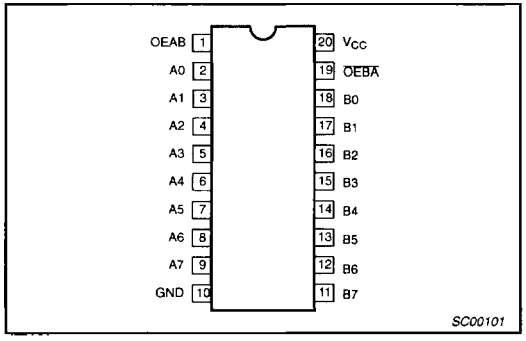
These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending on the logic levels at the enable inputs ($\overline{OEBA}$ and OEAB). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the 74ALS620A and 74ALS623A the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of the bus lines (16 in all) will remain at their last states.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

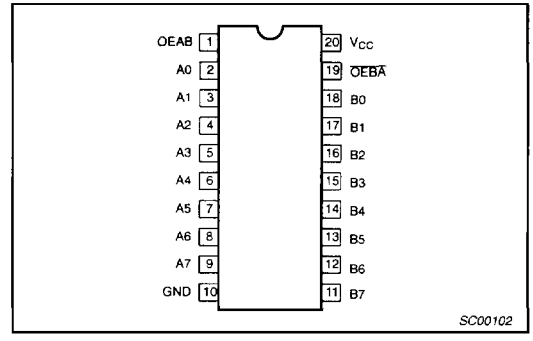
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7, B0 – B7	Data inputs	1.0/1.0	20µA/0.1mA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/1.0	20µA/0.1mA
A0 – A7, B0 – B7	Data outputs	750/240	15mA/24mA
A0 – A7, B0 – B7	Data outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20µA in the High state and 0.1mA in the Low state.

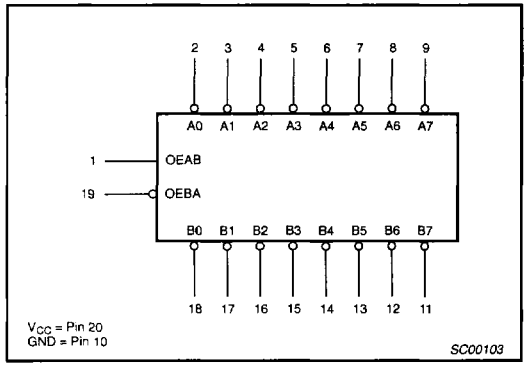
PIN CONFIGURATION – 74ALS620A/74ALS620A-1



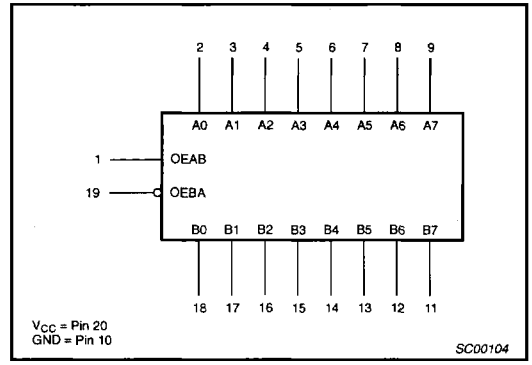
PIN CONFIGURATION – 74ALS623A/74ALS623A-1



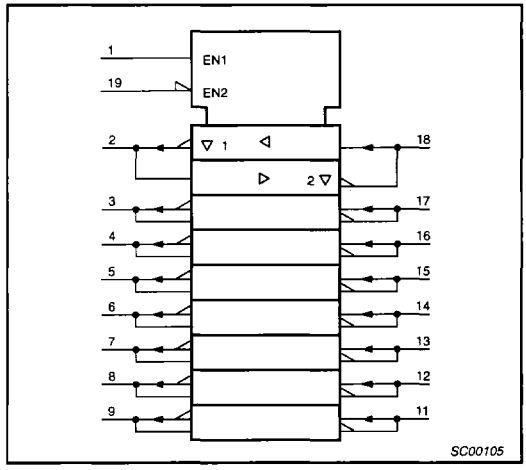
LOGIC SYMBOL – 74ALS620A/74ALS620A-1



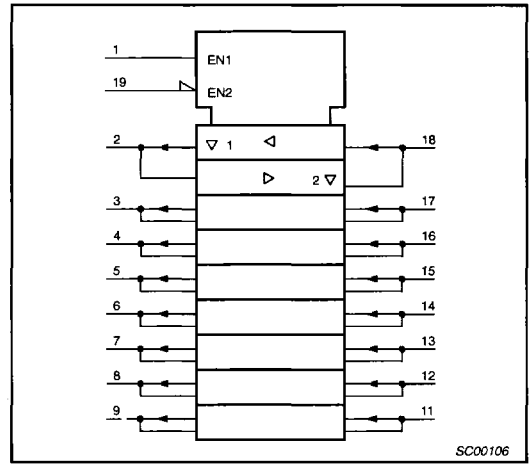
LOGIC SYMBOL – 74ALS623A/74ALS623A-1



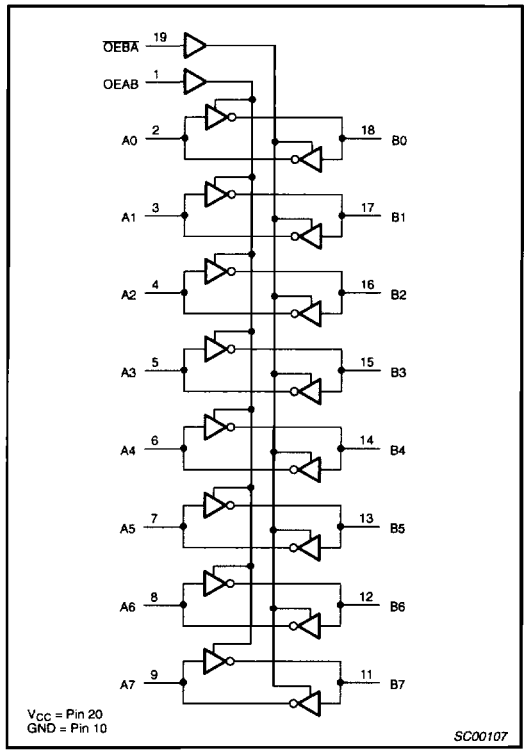
IEC/IEEE SYMBOL – 74ALS620A/74ALS620A-1



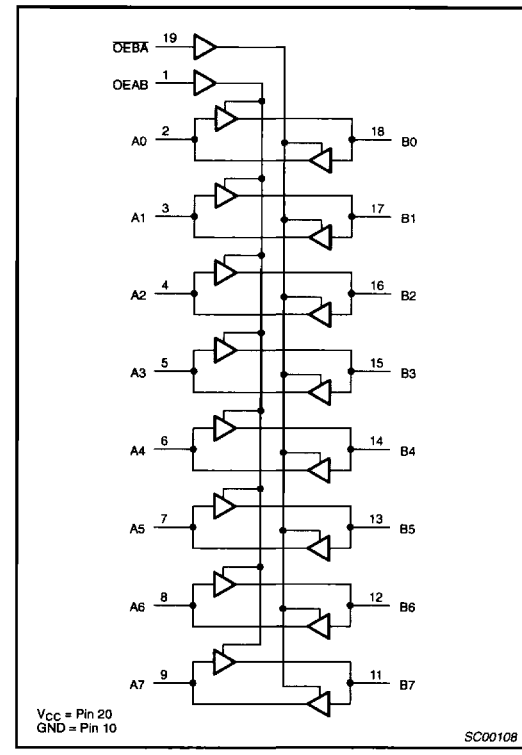
IEC/IEEE SYMBOL – 74ALS623A/74ALS623A-1



LOGIC DIAGRAM – 74ALS620A/74ALS620A-1



LOGIC DIAGRAM – 74ALS623A/74ALS623A-1



FUNCTION TABLE

INPUTS		OPERATING MODES	
$\overline{OEBA}$	OEAB	74ALS620A	74ALS623A
L	L	$\overline{B}$ data to A Bus	B data to A Bus
L	H	$\overline{A}$ data to B Bus	A data to B Bus
H	L	Z	Z
L	H	$\overline{B}$ data to A Bus	B data to A Bus
L	H	$\overline{A}$ data to B Bus	A data to B Bus

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current	All versions			24	mA
		-1 version			48 [1]	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

NOTE:
1. The 48mA limit applies only under the condition of V_{CC} = 5.0V ±5%.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = ±10%, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −0.4mA	V_{CC} − 2			V
					I_{OH} = −3mA	2.4	3.2		V
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −15mA	2.0			V
V_{OL}	Low-level output voltage	All versions		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 12mA		0.25	0.40	V
					I_{OL} = 24mA		0.35	0.50	V
		−1 versions		V_{CC} = 4.75V, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.5	V
I_I	Input current at maximum input voltage	$\overline{OEBA}$ or OEAB		V_{CC} = MAX, V_I = 7.0V				0.1	mA
		A or B ports		V_{CC} = MAX, V_I = 5.5V				0.1	mA
I_{IH}	High-level input current[3]			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current[3]			V_{CC} = MAX, V_I = 0.4V				−0.1	mA
I_O	Output current[4]			V_{CC} = MAX, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply current (total)	74ALS620A 74ALS620A-1	I_{CCH}	V_{CC} = MAX			24	34	mA
			I_{CCL}				42	49	mA
			I_{CCZ}				45	52	mA
		74ALS623A 74ALS623A-1	I_{CCH}	V_{CC} = MAX			24	43	mA
			I_{CCL}				41	50	mA
			I_{CCZ}				46	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. For I/O ports, the parameter I_{IH} and I_{IL} include the off-state current.
4. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS FOR 74ALS620A/74ALS620A-1

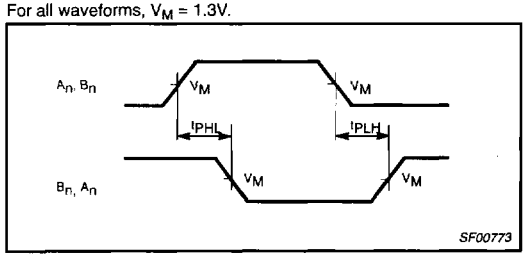
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.0 2.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	Waveform 3 Waveform 4	2.0 3.0	17.0 25.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	Waveform 3 Waveform 4	2.0 2.0	12.0 18.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	Waveform 3 Waveform 4	2.0 3.0	18.0 25.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	Waveform 3 Waveform 4	2.0 3.0	12.0 18.0	ns

AC ELECTRICAL CHARACTERISTICS FOR 74ALS623A/74ALS623A-1

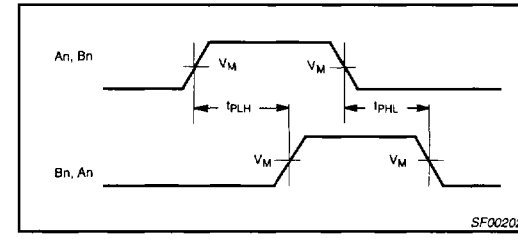
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 2	2.0 2.0	13.0 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	Waveform 3 Waveform 4	2.0 3.0	22.0 22.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	Waveform 3 Waveform 4	2.0 2.0	16.0 19.0	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	Waveform 3 Waveform 4	2.0 3.0	22.0 22.0	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	Waveform 3 Waveform 4	2.0 2.0	16.0 19.0	ns

AC WAVEFORMS

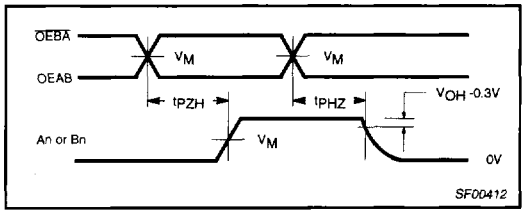
For all waveforms, V_M = 1.3V.



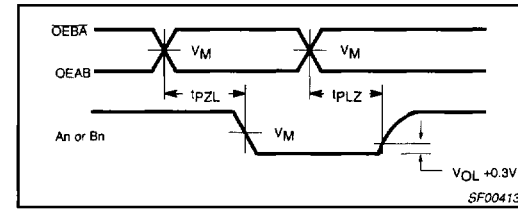
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-inverting Outputs

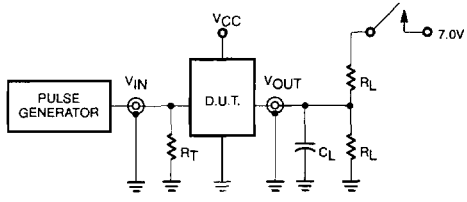


Waveform 3. 3-State Output Enable Time to High Level and Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs

SWITCH POSITION

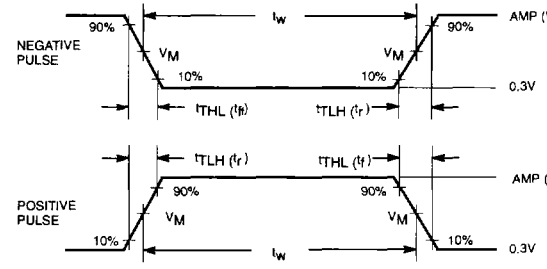
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

Family	INPUT PULSE REQUIREMENTS					
	Amplitude	V_M	Rep.Rate	t_w	t_{TLH}	t_{THL}
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

SC00072