QUALITY SEMICONDUCTOR, INC.

High-Speed CMOS 3.3V 16-Bit Latched Transceiver with Output Resistor

QS74LCX16H543

FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- Industry standard pinouts
- Bus Hold feature holds last active state during 3-state operation
- 10µA I_{CCQ} quiescent power supply current
- Hot Insertable
- 2.0V – 3.6V V_{CC} supply operation
- ±24mA balanced output drive
- Meets or exceeds JEDEC Standard 36 specifications
- t_{PD} = 5.3ns
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise
- Operating temperature range: –40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Packages available:
  - 56-pin TSSOP
  - 56-pin SSOP

DESCRIPTION

The LCX16H543 is a 16-bit latched bus transceiver with three-state outputs that is ideal for driving address and data buses. Two independent 8-bit D-type latched transceivers are used with separate input and output control to permit independent control of data flow in either direction. The QS74LCX16H543 provides Bus Hold circuitry on the data inputs to retain the last active state during 3-state operation, eliminating the need for external pull-up resistors. The 3.3V LCXPlus family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end advanced workstation applications. 5V tolerant inputs and outputs allow this LCXPlus product to be used in mixed 5V and 3.3V applications. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. To accommodate hot-plug or live insertion applications, this product is designed not to load an active bus when V_{CC} is removed.

Figure 1. Functional Block Diagram

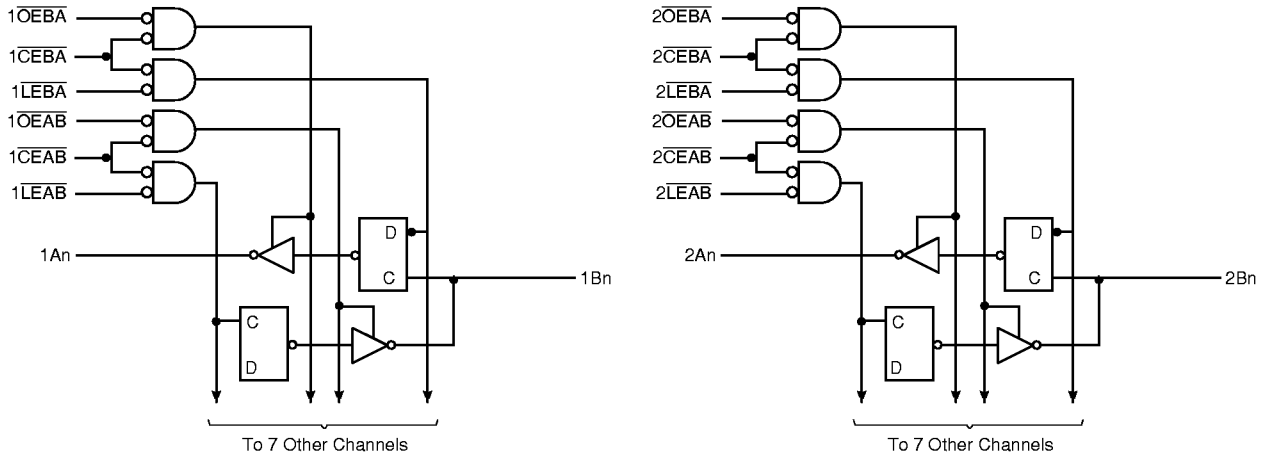


Figure 2. Pin Configuration
(All Pins Top View)

SSOP, TSSOP

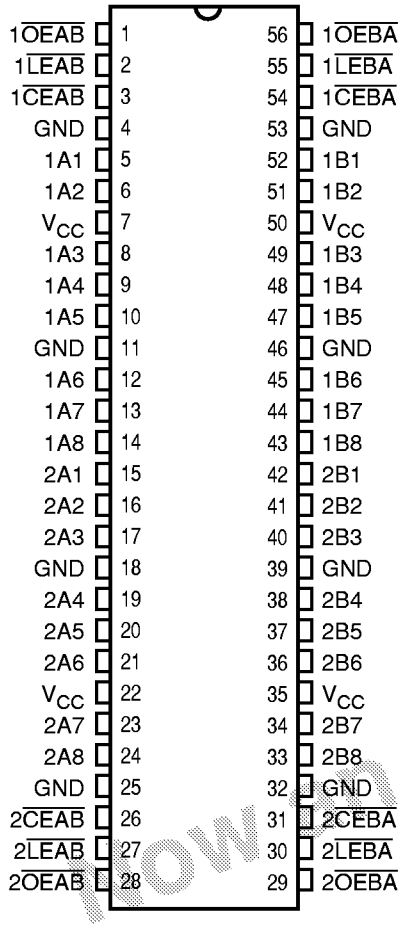


Table 1. Pin Description

Name	Description
x$\overline{\text{OEAB}}$	A to B Output Enable Inputs (Active LOW)
x$\overline{\text{OEBA}}$	B to A Output Enable Inputs (Active LOW)
x$\overline{\text{CEAB}}$	A to B Enable Inputs (Active LOW)
x$\overline{\text{CEBA}}$	B to A Enable Inputs (Active LOW)
x$\overline{\text{LEAB}}$	A to B Latch Enable Inputs (Active LOW)
x$\overline{\text{LEBA}}$	B to A Latch Enable Inputs (Active LOW)
xAx	A to B Data Inputs or B to A 3-State Outputs (Bus Hold Inputs)
xBx	B to A Data Inputs or A to B 3-State Outputs (Bus Hold Inputs)

Table 2. Function Table

Inputs			Latch Status	Output Buffers
x$\overline{\text{CEAB}}$	x$\overline{\text{LEAB}}$	x$\overline{\text{OEAB}}$	xAx to xBx	xBx
H	X	X	Storing	High-Z
X	H	X	Storing	X
X	X	H	X	High-Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

Notes:
1. * = Before x$\overline{\text{LEAB}}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. A-to-B data flow shown: B-to-A flow control is the same, except using x$\overline{\text{CEBA}}$, x$\overline{\text{LEBA}}$, x$\overline{\text{OEBA}}$

Table 3. Capacitance

Symbol	Pins	Typ	Unit	Conditions
C_{IN}	Input Capacitance	7.0	pF	V_{IN} = 0V, V_{OUT} = 0V, f = 1MHz
$C_{I/O}$	I/O Capacitance	8.0	pF	V_{IN} = 0V, V_{OUT} = 0V, f = 1MHz
C_{PD}	Power Dissipation Capacitance	25	pF	V_{CC} = 3.3V, V_{IN} = 0 or V_{CC} f = 10MHz

Note: Capacitance is characterized but not production tested.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground ..... –0.5V to 7.0V
DC Output Voltage V_{OUT}
Outputs HIGH-Z ..... –0.5V to 7.0V
Outputs Active ..... –0.5V to V_{CC} + 0.5V
DC Input Voltage V_{IN} ..... –0.5V to 7.0V
DC Input Diode Current with V_{IN} < 0 ..... –50mA
DC Output Diode Current
V_O < 0 ..... –50mA
V_O > V_{CC} 50mA
DC Output Source/Sink Current (I_{OH}/I_{OL}) ..... ±50mA
DC Supply Current per Supply Pin ..... ±100mA
DC Ground Current per Ground Pin ..... ±100mA
T_{STG} Storage Temperature ..... –65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 5. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage, Operating		2.0	3.6	V
	Supply Voltage, Data Retention Only		1.5	3.6	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage in Active State		0	V_{CC}	V
	Output Voltage in "OFF" State		0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0 – 3.6V	—	±24	mA
		V_{CC} = 2.7V	—	±12	
$\Delta t/\Delta v$	Input Transition Slew Rate		—	10	ns/V
T_A	Operating Free Air Temperature		–40	85	°C

Table 6. DC Electrical Characteristics Over Operating Range

Industrial Temperature Range, T_A = –40°C to 85°C

Symbol	Parameter	Test Conditions[1]	Min	Typ[2]	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = 2.7V, I_{OH} = –100µA V_{CC} = 2.7V, I_{OH} = –12mA V_{CC} = 3.0V, I_{OH} = –18mA V_{CC} = 3.0V, I_{OH} = –24mA	V_{CC} –0.2 2.2 2.4 2.2	— — — —	— — — —	V
V_{OL}	Output LOW Voltage	V_{CC} = 2.7V, I_{OL} = 100µA V_{CC} = 2.7V, I_{OL} = 12mA V_{CC} = 3.0V, I_{OL} = 16mA V_{CC} = 3.0V, I_{OL} = 24mA	— — — —	— — — —	0.2 0.4 0.4 0.5	V
ΔV_T	Input Hysteresis[3]	V_{TLH} – V_{THL} for All Inputs	—	150	—	mV
I_I	Input Leakage Current	V_I = 0V, V_I = 5.5V	—	—	±1.0	µA
$\lvert I_{BH} \rvert$	Input Current Input High or Low Bus Hold Inputs[3,4]	V_{CC} = 3.6V, V_{IN} = 0V or V_{IN} = V_{CC}	—	—	50	µA
		V_{CC} = 3.6V, 0.8V < V_{IN} < 2.0V	—	—	500[5]	µA
I_{BHH}	Bus Hold Sustaining Current Bus Hold Inputs	V_{CC} = 3V, V_{IN} = 2.0V	–75	—	—	µA
I_{BHL}		V_{IN} = 0.8V	75	—	—	µA
I_{OZ}	High-Z I/O Leakage[3]	V_O = 0V, V_O = 5.5V, V_I = V_{IH} or V_{IL}, V_{CC} = 3.6V	—	—	±1.0	µA
I_{OS}	Short Circuit Current[3,6]	V_{CC} = 3.6V, V_O = GND	–60	—	–200	mA
I_{OFF}	Power Off Leakage	V_{CC} = 0V, V_I or V_O = 5.5V	—	—	10	µA
V_{IK}	Input Clamp Voltage	V_{CC} = 2.7V, I_{IN} = –18mA	—	–0.7	–1.2	V

Notes:
1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operation Conditions for the applicable device type.
2. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
3. These parameters are guaranteed by characterization, but not production tested.
4. Pins with Bus Hold are identified in the Pin Description.
5. An external driver must provide at least $\lvert I_{BH} \rvert$ during transition to guarantee that the Bus Hold input will change state.
6. Not more than one output should be tested at one time. Duration of test should not exceed one second.

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Typ[2]	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = 3.6V, Freq. = 0 V_{IN} = GND or V_{CC}		0.1	10	µA
ΔI_{cc}	Supply Current per Input @ TTL HIGH	V_{CC} = 3.6V, V_{IN} = V_{CC} –0.6V[3]	Control Inputs	2.0	30	µA
			Bus Hold Inputs	—	500	
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = 3.6V, Outputs Open One Bit Toggling @ 50% Duty Cycle x$\overline{CEAB}$, x$\overline{OEAB}$ and x$\overline{LEAB}$ = GND	V_{IN} = V_{CC} V_{IN} = GND	65	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = 3.6V, Outputs Open One Bit Toggling @ 50% Duty Cycle f = 10MHz, x$\overline{CEBA}$ = V_{CC} x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$ = GND	V_{IN} = V_{CC}–0.6V V_{IN} = GND	0.5[5]	1.0[5]	mA
		V_{CC} = 3.6V, Outputs Open Sixteen Bits Toggling @ 50% Duty Cycle f = 2.5MHz, x$\overline{CEBA}$ = V_{CC} x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$ = GND	V_{IN} = V_{CC}–0.6V V_{IN} = GND	2.7[5]	8.0[5]	mA

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
2. Typical values are at V_{CC} = 3.3V, 25°C ambient.
3. Per TTL driven input. All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in total power supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$.
   $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} f N_O$.
   I_{CCQ} = Quiescent Current (I_{CCL}, I_{CCH}, and I_{CCZ}).
   ΔI_{CC} = Power Supply Current for a TTL-High Input (V_{IN} = V_{CC} –0.6V).
   D_H = Duty Cycle for TTL High Inputs.
   N_T = Number of TTL High Inputs.
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
   f = Average Switching Frequency per Output.
   N_O = Number of Outputs Switching.

Table 8. Dynamic Switching Characteristics[1]

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V

Note:
1. Characterized but not production tested.

Table 9. Switching Characteristics Over Operating Range

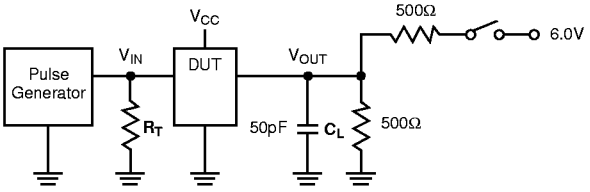
Industrial Temperature Range, T_A = –40°C to 85°C.
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	V_{CC} = 3.3 ±0.3V		V_{CC} = 2.7V[2]		Unit
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	1.5	5.3	1.5	6.3	ns
t_{PHL} t_{PLH}	Propagation Delay x$\overline{LEBA}$ to xAx, x$\overline{LEAB}$ to xBx	1.5	7.0	1.5	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx, x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx	1.5	8.0	1.5	9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2] x$\overline{OEBA}$ or x$\overline{OEAB}$ to xAx or xBx, x$\overline{CEBA}$ or x$\overline{CEAB}$ to xAx or xBx	1.5	6.5	1.5	7.5	ns
t_{SU}	Setup Time HIGH or LOW xAx or xBx to x$\overline{LEBA}$ or x$\overline{LEAB}$	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW xAx or xBx to x$\overline{LEBA}$ or x$\overline{LEAB}$	1.0	—	1.0	—	ns
t_W	Pulse Width LOW[2]	5.0	—	5.0	—	ns
$t_{SK(O)}$	Output Skew[3]	—	0.5	—	—	ns

Notes:
1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit



SWITCH POSITION	
Test	**Switch**
Open Drain Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND
All Other Inputs	Open

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Figure 4. Setup, Hold, and Release Timing

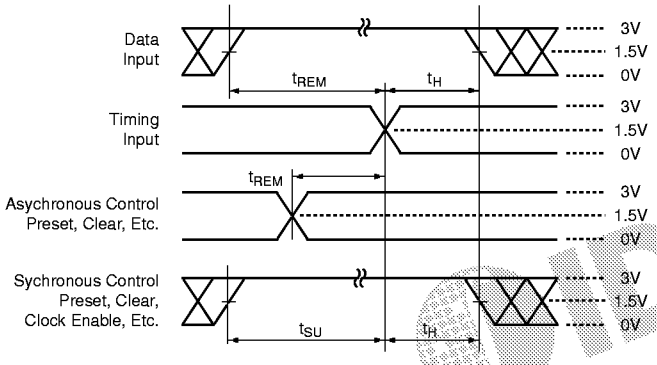


Figure 6. Pulse Width

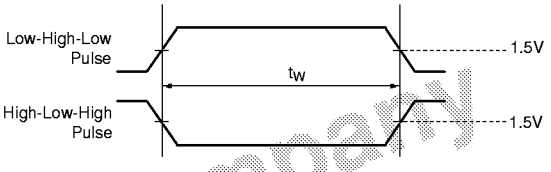


Figure 5. Enable and Disable Timing

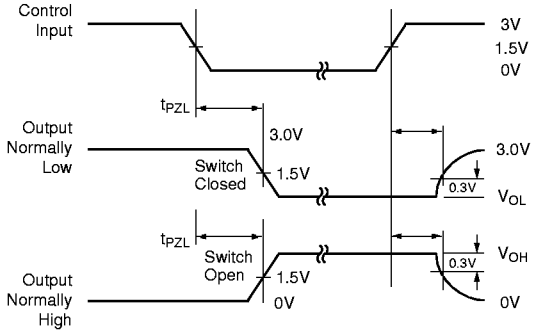
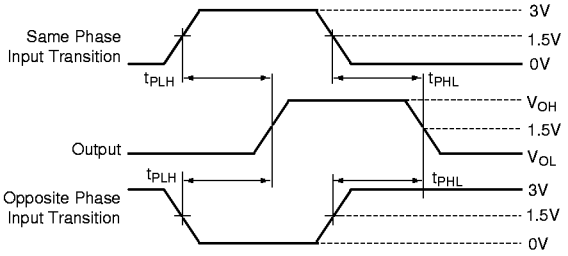
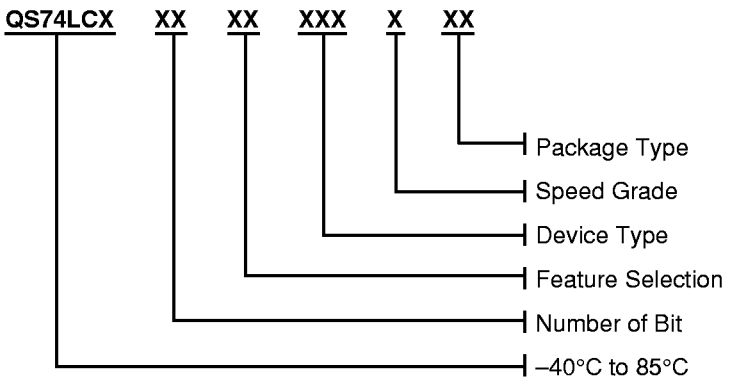


Figure 7. Propagation Delay



Notes:
1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_F, $t_R \leq 2.5$ns.

ORDERING INFORMATION



Device Type:
543

Speed Grades:
Blank – Standard

Package Type:
PV – SSOP, 300 mil
PA – TSSOP, 240 mil

Feature Selection:
H – Bus Hold

Number of Bit:
16 – 16-Bit