



# CY74FCT163952 CY74FCT163H952

## 16-Bit Registered Transceiver

### Features

- 5V tolerant Inputs and Outputs
- 24 mA balanced drive outputs
- Low power, pin-compatible replacement for LCX, LPT, LVC, LVCH & LVT families
- FCT-C speed at 6.3 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of -40°C to +85°C
- V<sub>CC</sub> = 2.7V to 3.6V
- Typical V<sub>OLP</sub> (ground bounce) < 0.6V at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C

### CY74FCT163H952 Features:

- Bus hold retains last active state
- Eliminates the need for external pull-up or pull-down resistors

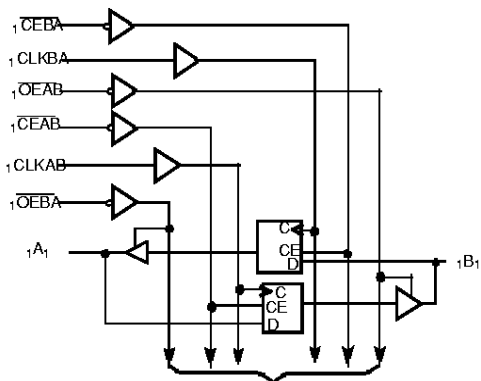
### Functional Description

These 16-bit registered transceivers are high-speed, low-power devices. 16-bit operation is achieved by connecting the control lines of the two 8-bit registered transceivers together. For data flow from bus A-to-B,  $\overline{CEAB}$  must be LOW to allow data to be stored when CLKAB transitions from LOW-to-HIGH. The stored data will be present on the output when  $\overline{OEAB}$  is LOW. Control of data from B-to-A is similar and is controlled by using the  $\overline{CEBA}$ , CLKBA, and  $\overline{OEBA}$  inputs. The outputs are 24-mA balanced output drivers with current limiting resistors to reduce the need for external terminating resistors and provide for minimal undershoot and reduced ground bounce.

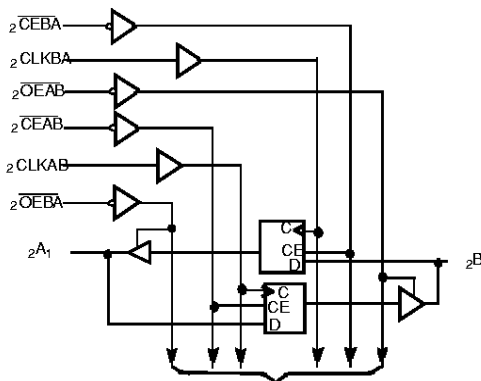
The CY74FCT163H952 has "bus hold" on the data inputs, which retain the input's last state whenever the source driving the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

The CY74FCT163952 and the CY74FCT163H952 are designed with inputs and outputs capable of being driven by 5.0V buses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power off disable feature enabling them to be used in applications requiring live insertion.

### Logic Block Diagrams



TO7 OTHERCHANNELS



TO7 OTHERCHANNELS

### Pin Configuration SSOP/TSSOP Top View

1OEAB	1	56	1OEBA
1CLKAB	2	55	1CLKBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A <sub>1</sub>	5	52	1B <sub>1</sub>
1A <sub>2</sub>	6	51	1B <sub>2</sub>
V <sub>CC</sub>	7	50	V <sub>CC</sub>
1A <sub>3</sub>	8	49	1B <sub>3</sub>
1A <sub>4</sub>	9	48	1B <sub>4</sub>
1A <sub>5</sub>	10	47	1B <sub>5</sub>
GND	11	46	GND
1A <sub>6</sub>	12	45	1B <sub>6</sub>
1A <sub>7</sub>	13	44	1B <sub>7</sub>
1A <sub>8</sub>	14	43	1B <sub>8</sub>
2A <sub>1</sub>	15	42	2B <sub>1</sub>
2A <sub>2</sub>	16	41	2B <sub>2</sub>
2A <sub>3</sub>	17	40	2B <sub>3</sub>
GND	18	39	GND
2A <sub>4</sub>	19	38	2B <sub>4</sub>
2A <sub>5</sub>	20	37	2B <sub>5</sub>
2A <sub>6</sub>	21	36	2B <sub>6</sub>
V <sub>CC</sub>	22	35	V <sub>CC</sub>
2A <sub>7</sub>	23	34	2B <sub>7</sub>
2A <sub>8</sub>	24	33	2B <sub>8</sub>
GND	25	32	GND
2CEAB	26	31	2CEBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA



**Pin Description**

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A	A-to-B Data Inputs or B-to-A Three-State Outputs <sup>[1]</sup>
B	B-to-A Data Inputs or A-to-B Three-State Outputs <sup>[1]</sup>

**Function Table**<sup>[2, 3]</sup>

For A-to-B (Symmetric with B-to-A)

Inputs				Outputs
$\overline{CEAB}$	CLKAB	$\overline{OEAB}$	A	B
H	X	L	X	B <sup>[4]</sup>
X	L	L	X	B <sup>[4]</sup>
L	$\downarrow$	L	L	L
L	$\uparrow$	L	H	H
X	X	H	X	Z

**Notes:**

- On the CY74FCT163H952 these pins have bus hold.
- A-to-B data flow is shown; B-to-A data flow is similar but uses  $\overline{CEBA}$ , CLKBA, and  $\overline{OEBA}$ .
- H = HIGH Voltage Level.  
L = LOW Voltage Level.  
X = Don't Care.  
 $\downarrow$  = LOW-to-HIGH Transition.  
Z = HIGH Impedance.
- Level of B before the indicated steady-state input conditions were established.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- With the exception of inputs with bus hold, unused inputs must always be connected to an appropriate logic voltage level, preferably either  $V_{CC}$  or ground.

**Maximum Ratings**<sup>[5, 6]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-55°C to +125°C
Ambient Temperature with Power Applied .....	-55°C to +125°C
Supply Voltage Range .....	0.5V to +4.6V
DC Input Voltage .....	-0.5V to +7.0V
DC Output Voltage .....	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin) .....	-60 to +120 mA
Power Dissipation .....	1.0W
Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)	

**Operating Range**

Range	Ambient Temperature	$V_{CC}$
Commercial	-40°C to +85°C	2.7V to 3.6V



**Electrical Characteristics** Over the Operating Range  $V_{CC}=2.7V$  to  $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. <sup>[7]</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage		2.0		5.5	V
$V_{IL}$	Input LOW Voltage				0.8	V
$V_H$	Input Hysteresis <sup>[8]</sup>			100		mV
$V_{IK}$	Input Clamp Diode Voltage	$V_{CC}=\text{Min.}, I_{IN}=-18\text{ mA}$		-0.7	-1.2	V
$I_{IH}$	Input HIGH Current	Standard	$V_{CC}=\text{Max.}, V_I=5.5$		$\pm 1$	$\mu\text{A}$
		Bus Hold	$V_{CC}=\text{Max.}, V_I=V_{CC}$		$\pm 100$	
$I_{IL}$	Input LOW Current	Standard	$V_{CC}=\text{Max.}, V_I=\text{GND}$		$\pm 1$	$\mu\text{A}$
		Bus Hold			$\pm 100$	
$I_{BBH}$ $I_{BBL}$	Bus Hold Sustain Current on Bus Hold Input <sup>[9]</sup>	$V_{CC}=\text{Min.}$	$V_I=2.0V$	-50		$\mu\text{A}$
			$V_I=0.8V$	+50		
$I_{BHHO}$ $I_{BHLO}$	Bus Hold Overdrive Current on Bus Hold Input <sup>[9]</sup>	$V_{CC}=\text{Max.}, V_I=1.5V$			$\pm 500$	$\mu\text{A}$
$I_{OZH}$	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}, V_{OUT}=5.5V$			$\pm 1$	$\mu\text{A}$
$I_{OZL}$	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}, V_{OUT}=\text{GND}$			$\pm 1$	$\mu\text{A}$
$I_{ODL}$	Output LOW Current <sup>[11]</sup>	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	50	90	200	mA
$I_{ODH}$	Output HIGH Current <sup>[11]</sup>	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	-36	-60	-110	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC}=\text{Min.}, I_{OH}=-0.1\text{ mA}$	$V_{CC}-0.2$			V
		$V_{CC}=3.0, I_{OH}=-8\text{ mA}$	2.4 <sup>[10]</sup>	3.0		
		$V_{CC}=3.0V, I_{OH}=-24\text{ mA}$	2.0	3.0		
$V_{OL}$	Output LOW Voltage	$V_{CC}=\text{Min.}, I_{OL}=0.1\text{ mA}$			0.2	V
		$V_{CC}=\text{Min.}, I_{OL}=24\text{ mA}$		0.3	0.5	
$I_{OS}$	Short Circuit Current <sup>[11]</sup>	$V_{CC}=\text{Max.}, V_{OUT}=\text{GND}$	-60	-140	-200	mA
$I_{OFF}$	Power-Off Disable	$V_{CC}=0V, V_{OUT}\leq 4.5V$			$\pm 100$	$\mu\text{A}$

**Capacitance** ( $T_A = +25^\circ\text{C}, f = 1.0\text{ MHz}$ )

Parameter	Description	Test Conditions	Typ. <sup>[7]</sup>	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

**Note:**

7. Typical values are at  $V_{CC}=3.3V, T_A=+25^\circ\text{C}$  ambient.
8. This parameter is guaranteed but not tested.
9. Pins with bus hold are described in the Pin Description.
10.  $V_{OH}=V_{CC}-0.6V$  at rated current.
11. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.



**Power Supply Characteristics**

Parameter	Description	Test Conditions		Typ. <sup>[7]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$	0.1	10	$\mu A$
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{[12]}$	2.0	30	$\mu A$
$I_{CCD}$	Dynamic Power Supply Current <sup>[13]</sup>	$V_{CC} = \text{Max.}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OEAB}$ or $\overline{OEBA} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	50	75	$\mu A/\text{MHz}$
$I_C$	Total Power Supply Current <sup>[14]</sup>	$V_{CC} = \text{Max.}$ , $f_1 = 5 \text{ MHz}$ , $f_0 = 10 \text{ MHz}$ (CLKAB) $\overline{OEAB} = \overline{OEBA} = \text{GND}$ $\overline{OEBA} = V_{CC}$ 50% Duty Cycle, Outputs Open, One Bit Toggling	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	0.5	0.8	mA
			$V_{IN} = V_{CC} - 0.6V$ or $V_{IN} = \text{GND}$	0.5	0.8	
		$V_{CC} = \text{Max.}$ , $f_0 = 10 \text{ MHz}$ (CLKAB) $f_1 = 2.5 \text{ MHz}$ , $\overline{OEAB} = \overline{OEBA} = \text{GND}$ $\overline{OEBA} = V_{CC}$ 50% Duty Cycle, Outputs Open, Sixteen Bit Toggling	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	2.3	3.8 <sup>[15]</sup>	
			$V_{IN} = V_{CC} - 0.6V$ or $V_{IN} = \text{GND}$	2.3	4.0 <sup>[15]</sup>	

**Notes:**

- 12. Per TTL driven input, all other inputs at  $V_{CC}$  or GND.
- 13. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- 14.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0 N_C / 2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $N_C$  = Number of clock inputs changing at  $f_1$   
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
- 15. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.



**Switching Characteristics** Over the Operating Range  $V_{CC}=3.0V$  to  $3.6V$  [16,17]

Parameter	Description	CY74FCT163952A CY74FCT163H952A		CY74FCT163952C CY74FCT163H952C		Unit	Fig. No. [18]
		Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay CLKAB, CLKBA to B, A	2.0	10.0	2.0	6.3	ns	1, 5
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}BA, \overline{OE}AB$ to A, B	1.5	10.5	1.5	7.0	ns	1, 7, 8
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}BA, \overline{OE}AB$ to A, B	1.5	10.0	1.5	6.5	ns	1, 7, 8
$t_{SU}$	Set-Up Time, HIGH or LOW A, B to CLKAB, CLKBA	2.5	—	2.5	—	ns	4
$t_H$	Hold Time, HIGH or LOW A, B to CLKAB, CLKBA	2.0	—	1.5	—	ns	4
$t_{SU}$	Set-Up Time, HIGH or LOW $\overline{CE}AB, \overline{CE}BA$ to CLKAB, CLKBA	3.0	—	3.0	—	ns	4
$t_H$	Hold Time, HIGH or LOW $\overline{CE}AB, \overline{CE}BA$ to CLKAB, CLKBA	2.0	—	2.0	—	ns	4
$t_W$	Pulse Width HIGH or LOW CLKAB or CLKBA [19]	3.0	—	3.0	—	ns	5
$t_{SK(O)}$	Output Skew [20]	—	0.5	—	0.5	ns	—

**Ordering Information CY74FCT163952**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT163952CPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163952CPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT163952APAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163952APVC	O56	56-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT163H952**

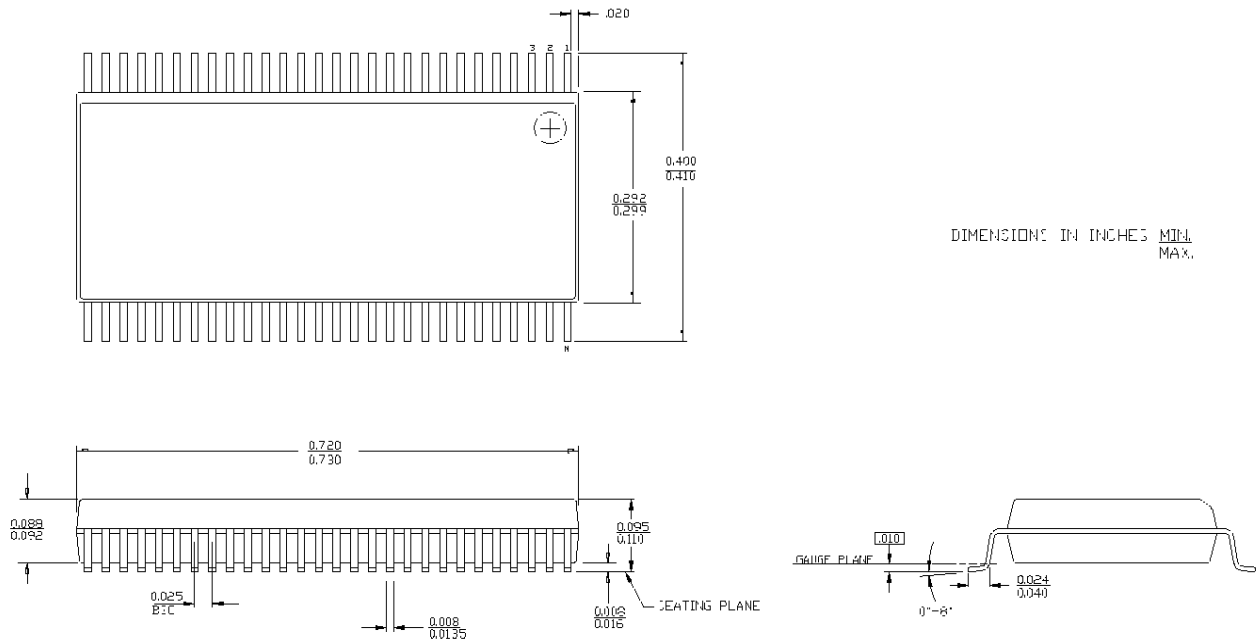
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6.3	CY74FCT163H952CPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163H952CPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT163H952APAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT163H952APVC	O56	56-Lead (300-Mil) SSOP	

**Notes:**

16. Minimum limits are guaranteed but not tested on Propagation Delays.
17. For  $V_{CC}=2.7$ , propagation delay, output enable and output disable times should be degraded by 20%.
18. See "Parameter Measurement Information" in the General Information section.
19. This parameter is guaranteed but not tested.
20. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

**Package Diagrams**

**56-Lead Shrunken Small Outline Package O56**



**56-Lead Thin Shrunken Small Outline Package Z56**

