8-Bit Bus Front-Loading-Latch Transceivers

SN54/74LS651
SN54/74LS653
SN54/74LS652
SN54/74LS654

Features/Benefits

- **Bidirectional bus transceivers and registers**
- **Independent registers for A and B buses**
- **Real-time data transfer or stored data transfer**
- **Simultaneous outputs on both buses**
- **24-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Three-state or open-collector outputs drive bus lines**
- **'LS653/4 are open-collector in A direction, three-state in B direction**

Description

These 8-bit bus transceivers with 3-state ('LS651, 'LS652) or open-collector ('LS653, 'LS654) outputs have 16 D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS651/653 and 'LS652/654 are given in their respective Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a by-passing path or "feed-through" into a two-way mux, is sometimes called a "front-loading latch."

A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs.

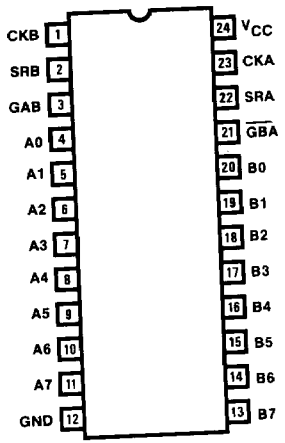
Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	OUTPUTS	POWER
SN54LS651	JS,W,L*	Mil	Invert	Three-state	LS
SN74LS651	NS,JS, NL (28)	Com	Invert	Three-state	LS
SN54LS652	JS,W,L*	Mil	Noninvert	Three-state	LS
SN74LS652	NS,JS, NL (28)	Com	Noninvert	Three-state	LS
SN54LS653	JS,W,L*	Mil	Invert	A bus open-collector; B bus three-state	LS
SN74LS653	NS,JS, NL (28)	Com	Invert		LS
SN54LS654	JS,W,L*	Mil	Noninvert		LS
SN74LS654	NS,JS, NL (28)	Com	Noninvert		LS

* L package here is L28. The other packages are 24-pin.

Pin Configurations

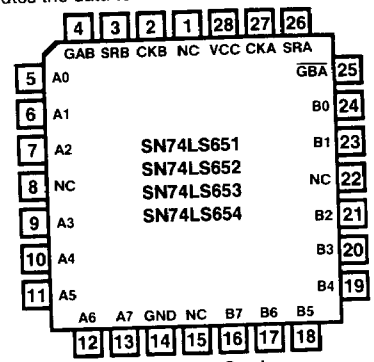
'LS651/652/653/654
8-Bit Bus Front-Loading-Latch Transceivers



Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by two enable lines, GAB and $\overline{GBA}$.

When GAB is Low and $\overline{GBA}$ is High, data from the buses can be loaded into registers A and B. When $\overline{GBA}$ is Low, the A bus is configured for output. When GAB is High, the B bus is configured for output. The A and B buses can be enabled at the same time, to operate as outputs simultaneously.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.



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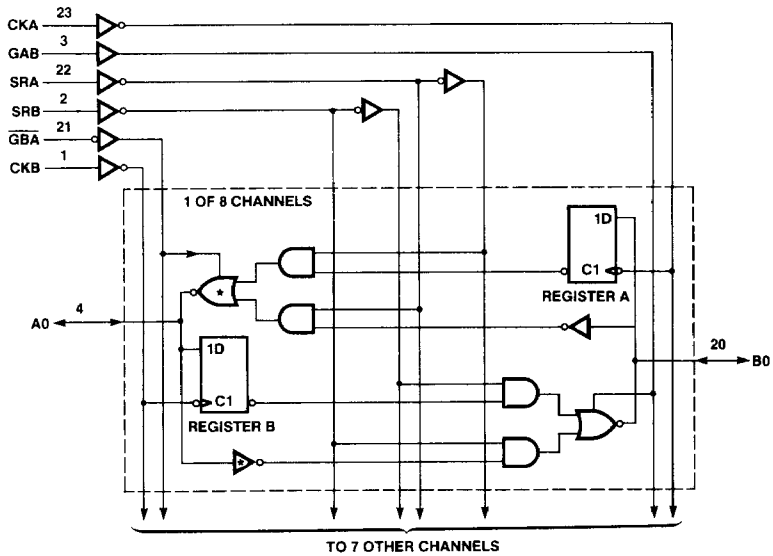
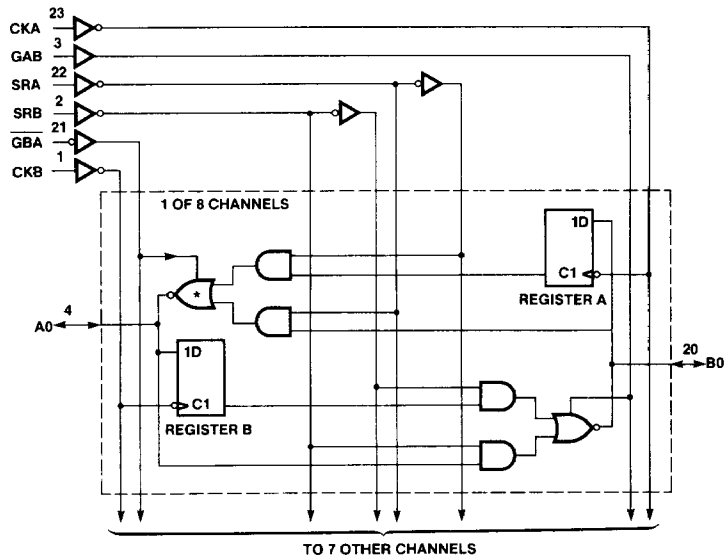
Logic Diagrams

'LS652/654 (Non-Inverting)



* For the 'LS652 devices, the A bus outputs are 3-state.
For the 'LS654 devices, the A bus outputs are open-collector.
The B bus outputs are 3-state for both devices.

'LS651/653 (Inverting)



* For the 'LS651 devices, the A bus outputs are 3-state.
For the 'LS653 devices, the A bus outputs are open-collector.
The B bus outputs are 3-state for both devices.

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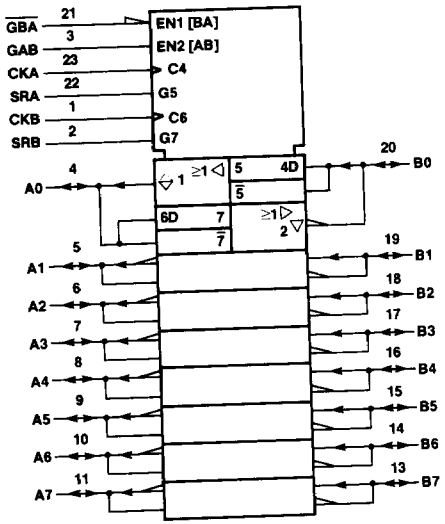
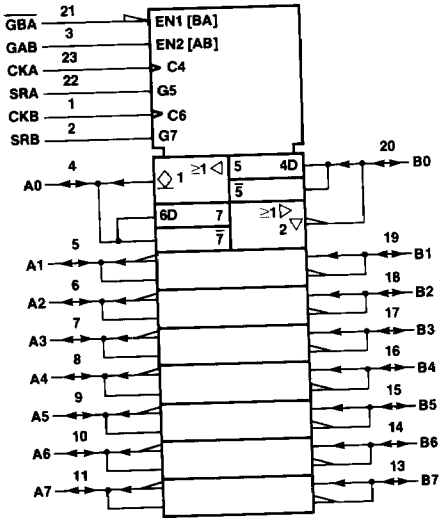
IEEE Symbols

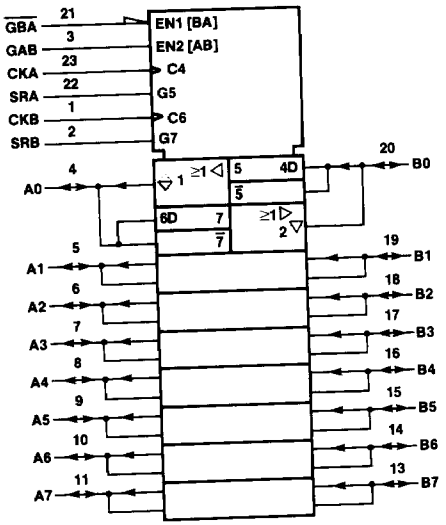
'LS651



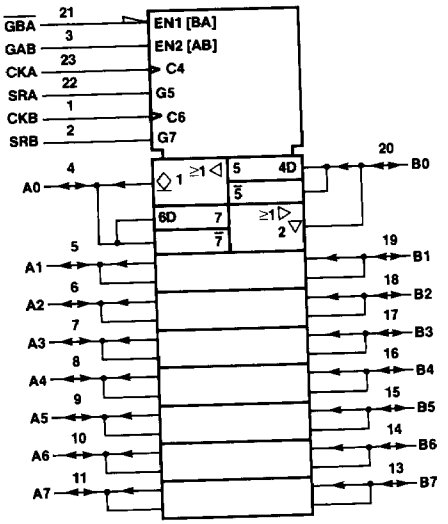
'LS653



'LS652

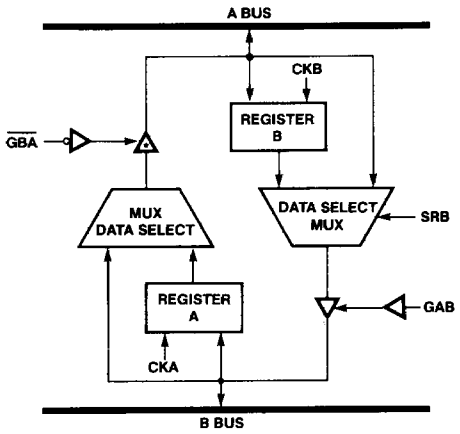


'LS654

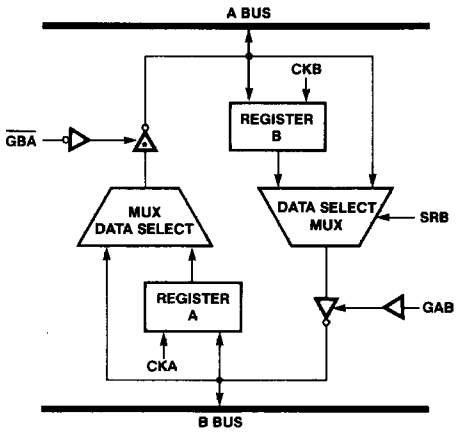


Block Diagrams

'LS652/654 (Non-Inverting)



'LS651/653 (Inverting)



* For the 'LS651/652 devices, the A bus outputs are 3-state.
For the 'LS653/654 devices, the A bus outputs are open-collector.
The B bus outputs are 3-state for both devices.

Function Table Nomenclature Description

GAB: To enable the A-to-B operation.

$\overline{GBA}$: To enable the B-to-A operation.

GAB	$\overline{GBA}$	OPERATION DIRECTION
L	L	B to A
L	H	A and B buses both are inputs (storage)
H	L	A and B buses both are outputs (Transfer stored data to bus)
H	H	A to B

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for Register A/B.

X: H or L state irrelevant ("Don't Care" conditions).

↑: Positive edge of CK causes clocking, if clocking enable is asserted.

UC: H or L or ↓ case (nonclocked operation).

RGTR: Register.

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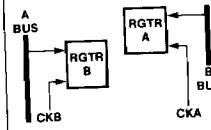
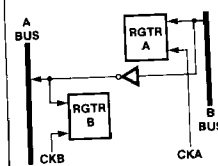
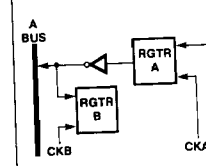
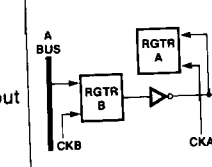
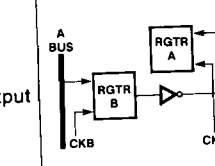
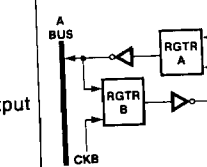
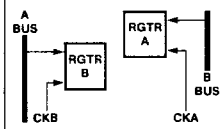
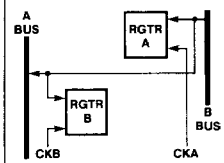
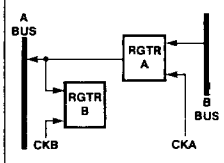
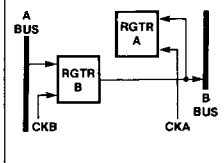
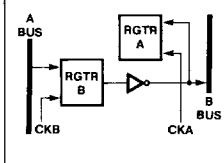
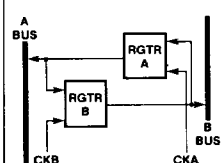
Bus Operation for 'LS651/653

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS651/653
	GAB	$\overline{GBA}$	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	L	H	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time $\overline{B}$ bus data → A bus
								UC	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR B
								↑	UC	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR A Real time $\overline{B}$ bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR $\overline{A}$ data → A bus
								UC	↑	RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
Real time A-to-B Operation	H	H	X	L	Input	Output		UC	UC	Real time $\overline{A}$ bus data → B bus
								UC	↑	Real time $\overline{A}$ bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A
								↑	↑	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	H	H	X	H	Input	Output		UC	UC	RGTR $\overline{B}$ data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus
								↑	UC	RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
Transfer Stored Data	H	L	H	H	Output	Output		UC	UC	RGTR $\overline{A}/\overline{B}$ data → A/B bus
								UC	↑	RGTR $\overline{A}/\overline{B}$ data → A/B bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	RGTR $\overline{A}/\overline{B}$ data → A/B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	RGTR $\overline{A}/\overline{B}$ data → A/B bus RGTR $\overline{A}$ data → RGTR B RGTR $\overline{B}$ data → RGTR A

Bus Operation for 'LS652/654

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS652/654
	GAB	$\overline{GBA}$	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	L	H	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time B bus data → A bus
								UC	↑	Real time B bus data → A bus Real time B bus data → RGTR B
								↑	UC	Real time B bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR A data → A bus
								UC	↑	RGTR A data → A bus RGTR A data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR A data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
Real time A-to-B Operation	H	H	X	L	Input	Output		UC	UC	Real time A bus data → B bus
								UC	↑	Real time A bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time A bus data → B bus Real time A bus data → RGTR A
								↑	↑	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	H	H	X	H	Input	Output		UC	UC	RGTR B data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR B data → B bus
								↑	UC	RGTR B data → B bus RGTR B data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A
Transfer Stored Data	H	L	H	H	Output	Output		UC	UC	RGTR A/B data → A/B bus
								UC	↑	RGTR A/B data → A/B bus RGTR A data → RGTR B
								↑	UC	RGTR A/B data → A/B bus RGTR B data → RGTR A
								↑	↑	RGTR A/B data → A/B bus RGTR A data → RGTR B RGTR B data → RGTR A

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Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		-55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS651	20 ↑			20 ↑			ns
		'LS652	20 ↑			20 ↑			
t_h	Hold time	'LS651	0 ↑			0 ↑			ns
		'LS652	0 ↑			0 ↑			
I_{OH}	High-level output current				-12			-15	mA
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5			-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			-0.4			-0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = -3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			-400			-400	μA
I_{OZH}				V_O = 2.7 V			20			20	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		-40		-225	-40		-225	mA
I_{CC}	Supply current		V_{CC} = MAX	'LS651 Outputs High			145			145	mA
				'LS651 Outputs Low			165			165	
				'LS651 Outputs disabled			165			165	
				'LS652 Outputs High			145			145	
				'LS652 Outputs Low			165			165	
				'LS652 Outputs disabled			165			165	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS651 MIN	'LS651 MAX	'LS652 MIN	'LS652 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		15		15	ns
t_{PHL}				15		20	ns
t_{PLH}	Clock to output delay			20		20	ns
t_{PHL}				30		30	ns
t_{PLH}	Select to output delay † (data input High)			35		35	ns
t_{PHL}				20		25	ns
t_{PLH}	Select to output delay † (data input Low)			35		35	ns
t_{PHL}				30		20	ns
t_{PZL}	$\overline{GBA}$ to A bus output enable delay			25		25	ns
t_{PZH}				20		20	ns
t_{PLZ}	$\overline{GBA}$ to A bus output disable delay	C_L = 5pF R_L = 667Ω		25		25	ns
t_{PHZ}				35		35	ns
t_{PZL}	GAB to B bus output enable delay	C_L = 45pF R_L = 667Ω		30		30	ns
t_{PZH}				25		25	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω		25		25	ns
t_{PHZ}				35		35	ns

† See Figure 4.

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIL 'LS651 MIN	MIL 'LS651 MAX	MIL 'LS652 MIN	MIL 'LS652 MAX	COM 'LS651 MIN	COM 'LS651 MAX	COM 'LS652 MIN	COM 'LS652 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		20		20		15		20	ns
t_{PHL}				20		25		17		22	ns
t_{PLH}	Clock to output delay			25		25		22		22	ns
t_{PHL}				35		35		30		30	ns
t_{PLH}	Select to output delay † (data input High)			40		40		35		35	ns
t_{PHL}				25		30		25		28	ns
t_{PLH}	Select to output delay † (data input Low)			40		40		35		35	ns
t_{PHL}				35		25		30		22	ns
t_{PZL}	$\overline{GBA}$ to A bus output enable delay			30		30		25		25	ns
t_{PZH}				25		25		20		20	ns
t_{PLZ}	$\overline{GBA}$ to A bus output disable delay	C_L = 5pF R_L = 667Ω		35		30		30		28	ns
t_{PHZ}				40		45		40		40	ns
t_{PZL}	GAB to B bus output enable delay	C_L = 45pF R_L = 667Ω		35		35		30		32	ns
t_{PZH}				30		30		25		25	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω		35		35		30		30	ns
t_{PHZ}				40		45		35		40	ns

† See Figure 4.

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Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		-55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS653	20 ↑			20 ↑			ns
		'LS654	20 ↑			20 ↑			
t_h	Hold time	'LS653	0 ↑			0 ↑			ns
		'LS654	0 ↑			0 ↑			
V_{OH}	High-level output voltage (A bus only)				5.5			5.5	V
I_{OH}	High-level output current (B bus only)				-12			-15	mA
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions, ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			−0.4			−0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage (B bus only)		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
I_{OH}	High-level output current (A bus only)		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	V_{OH} = 5.5 V			100			100	μA
I_{OZL}	Off-state output current (B bus only)		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			−400			−400	μA
I_{OZH}				V_O = 2.7 V (B bus only)			20			20	μA
I_{OS}	Output short-circuit current* (B bus only)		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current		V_{CC} = MAX	'LS-653 Outputs High			145			145	mA
				'LS-653 Outputs Low			165			165	
				'LS-653 Outputs disabled			165			165	
				'LS-654 Outputs High			145			145	
				'LS-654 Outputs Low			165			165	
				'LS-654 Outputs disabled			165			165	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

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Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS* (See Test Load/Waveforms)	'LS653 MIN	'LS653 MAX	'LS654 MIN	'LS654 MAX	UNIT
t_{PLH}	Data to A bus output delay	C_L = 45pF R_L = 667Ω		25		25	ns
t_{PHL}				20		25	ns
t_{PLH}	Data to B bus output delay			15		15	ns
t_{PHL}				15		20	ns
t_{PLH}	Clock to A bus output delay			30		30	ns
t_{PHL}				30		30	ns
t_{PLH}	Clock to B bus output delay			20		20	ns
t_{PHL}				30		30	ns
t_{PLH}	Select to A bus † output delay (data input High)			45		45	ns
t_{PHL}				25		30	ns
t_{PLH}	Select to A bus † output delay (data input Low)			40		45	ns
t_{PHL}				30		25	ns
t_{PLH}	Select to B bus † output delay (data input High)			35		35	ns
t_{PHL}				25		25	ns
t_{PLH}	Select to B bus † output delay (data input Low)			35		35	ns
t_{PHL}				30		20	ns
t_{PLH}	$\overline{GBA}$ to A bus output enable delay			35		35	ns
t_{PHL}				25		30	ns
t_{PZL}	GAB to B bus output enable delay			30		30	ns
t_{PZH}				25		25	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω		25		25	ns
t_{PHZ}				35		35	ns

* For A bus, the test load will refer to the open-collector test load. See Figure 6.
For B bus, the test load will refer to the three-state test load. See Figure 7.

† See Figure 4.

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS* (See Test Load/Waveforms)	MIL		COM		UNIT
			'LS653 MIN MAX	'LS654 MIN MAX	'LS653 MIN MAX	'LS654 MIN MAX	
t_{PLH}	Data to A bus output delay	C_L = 45pF R_L = 667Ω	30	30	28	30	ns
t_{PHL}			25	30	23	28	ns
t_{PLH}	Data to B bus output delay		20	20	18	18	ns
t_{PHL}			20	25	18	20	ns
t_{PLH}	Clock to A bus output delay		40	40	35	35	ns
t_{PHL}			40	40	35	35	ns
t_{PLH}	Clock to B bus output delay		25	25	23	23	ns
t_{PHL}			35	35	30	30	ns
t_{PLH}	Select to A bus output † delay (data input High)		50	50	45	48	ns
t_{PHL}			30	40	25	35	ns
t_{PLH}	Select to A bus output † delay (data input Low)		45	55	43	50	ns
t_{PHL}			35	30	30	28	ns
t_{PLH}	Select to B bus output † delay (data input High)		40	35	35	35	ns
t_{PHL}			25	35	25	30	ns
t_{PLH}	Select to B bus output † delay (data input Low)		40	45	35	40	ns
t_{PHL}			35	25	30	23	ns
t_{PLH}	$\overline{GBA}$ to A bus output enable delay		40	35	35	35	ns
t_{PHL}			30	40	28	35	ns
t_{PZL}	GAB to B bus output enable delay		35	35	30	33	ns
t_{PZH}			30	30	25	28	ns
t_{PLZ}	GAB to B bus output disable delay	C_L = 5pF R_L = 667Ω	35	35	30	30	ns
t_{PHZ}			40	45	38	40	ns

* For A bus, the test load will refer to the open-collector test load. See Figure 6.
For B bus, the test load will refer to the three-state test load. See Figure 7.

† See Figure 4.

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Test Waveforms

Setup Time/Hold Time

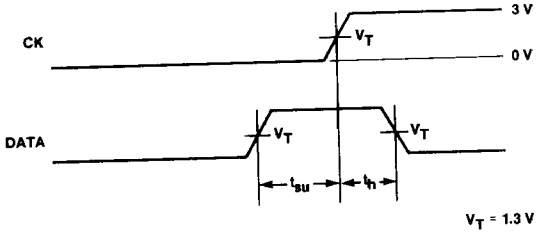


Figure 1.

Bus Data To Bus Output Delay

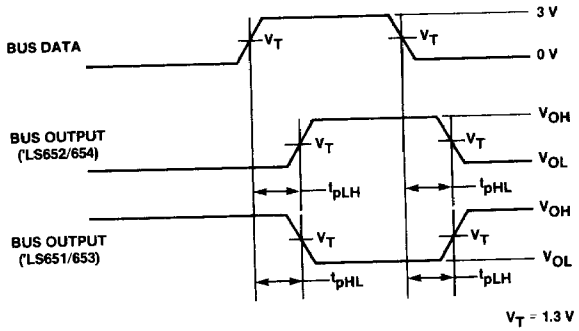


Figure 2.

CK To Bus Output Propagation Delay Time

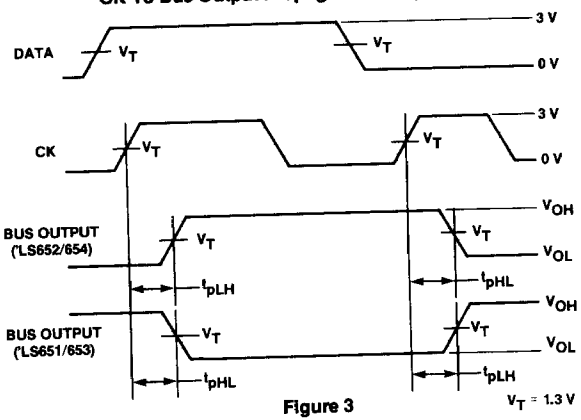


Figure 3

Select To Output Delay

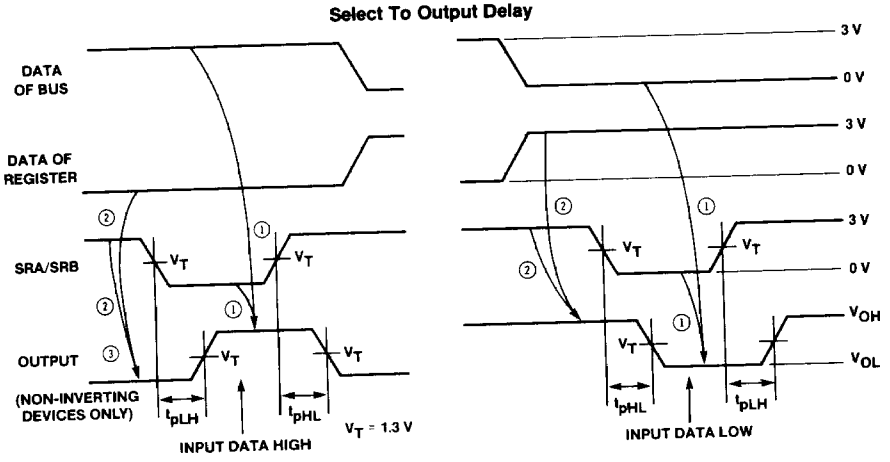


Figure 4

NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Enable/Disable Delay

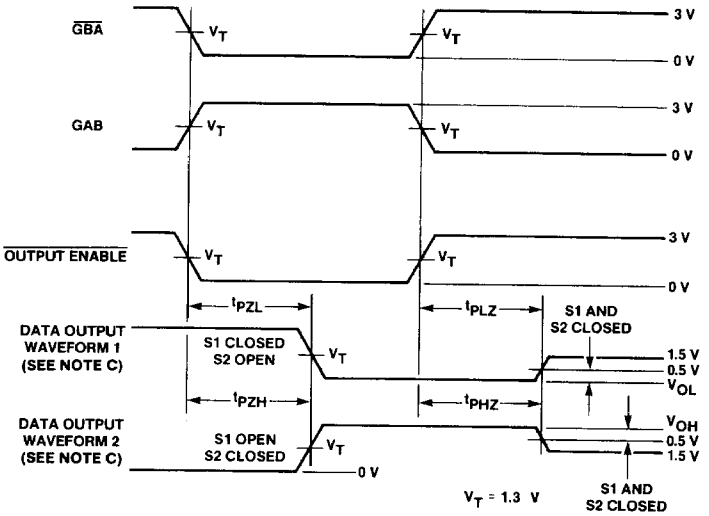
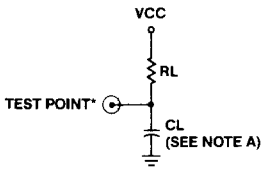
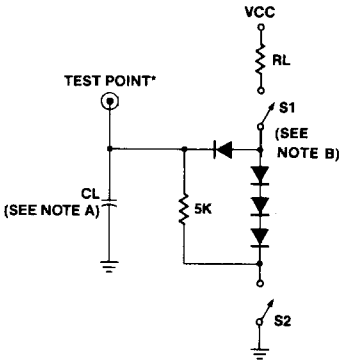


Figure 5

Test Loads



Load Circuit For Open-Collector Outputs



Load Circuit For Three-State Outputs

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Notes: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50 Ω and t_R = 15 ns t_F ≤ 6 ns.
F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

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