Order Number: MC100EP222/D
Rev. 2, 09/2001

Low Voltage ECL/PECL 1:15 Clock Driver

MC100EP222

See Upgrade Product – MC100ES6222

LOW VOLTAGE 3.3 V/2.5 V 1:15 DIFFERENTIAL ECL/PECL CLOCK DRIVER

TB SUFFIX
52–LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336

The MC100EP222 is a low voltage, low skew 1:15 differential ÷1 and ÷2 ECL/PECL clock distribution buffer. The MC100EP222 has been designed and optimized for 2.5 V and 3.3 V systems. Target applications for this clock driver are high performance clock distribution systems for computer, networking and telecommunication systems.

Features:

- 15 differential ECL outputs (4 output banks)
- 2 selectable differential ECL inputs
- Selectable 1:1 or 1:2 frequency outputs
- Operates from a -2.5, -3.3 V (ECL) or 2.5, 3.3 V (PECL) power supply
- Extended temperature operating range of -40 to +85 deg C

The MC100EP222 device characteristics allows low-skew clock distribution of differential and single-ended LVECL/LVPECL signals. Typical applications for the MC100EP222 are primary clock distribution systems on backplanes of high-performance computer, networking and telecommunication systems.

The MC100EP222 can be operated from a 3.3 V or 2.5 V positive supply (PECL mode) without the requirement of a negative supply line. Each of the four output banks of two, three, four and six differential clock output pairs may be independently configured to distribute the input frequency or ÷2 of the input frequency. The FSELA, FSELB, FSELC, FSELD and CLK_SEL are asychronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the the ÷2 outputs. For the functionality of the MR control input, “Timing Diagram” on page 648.

Each of the CLK0, CLK1 inputs can be used differential of single-ended. For single-ended signals, connect the bypassed V_{BB} output reference to the unused input of the pair.

The MC100EP222 guarantees low output-to-output skew of 40 (70) ps and device-to-device skew of max. 350 ps. To ensure low skew clock signals in the application, both sides of any differential output pair need to be terminated identically, even if only one side is used. When fewer than all fifteen pairs are used, identical termination of all output pairs on the same package side is recommended. If no outputs on a side are used, it is recommended to leave all of these outputs open and unterminated. This will maintain minimum output skew.

Rev 2

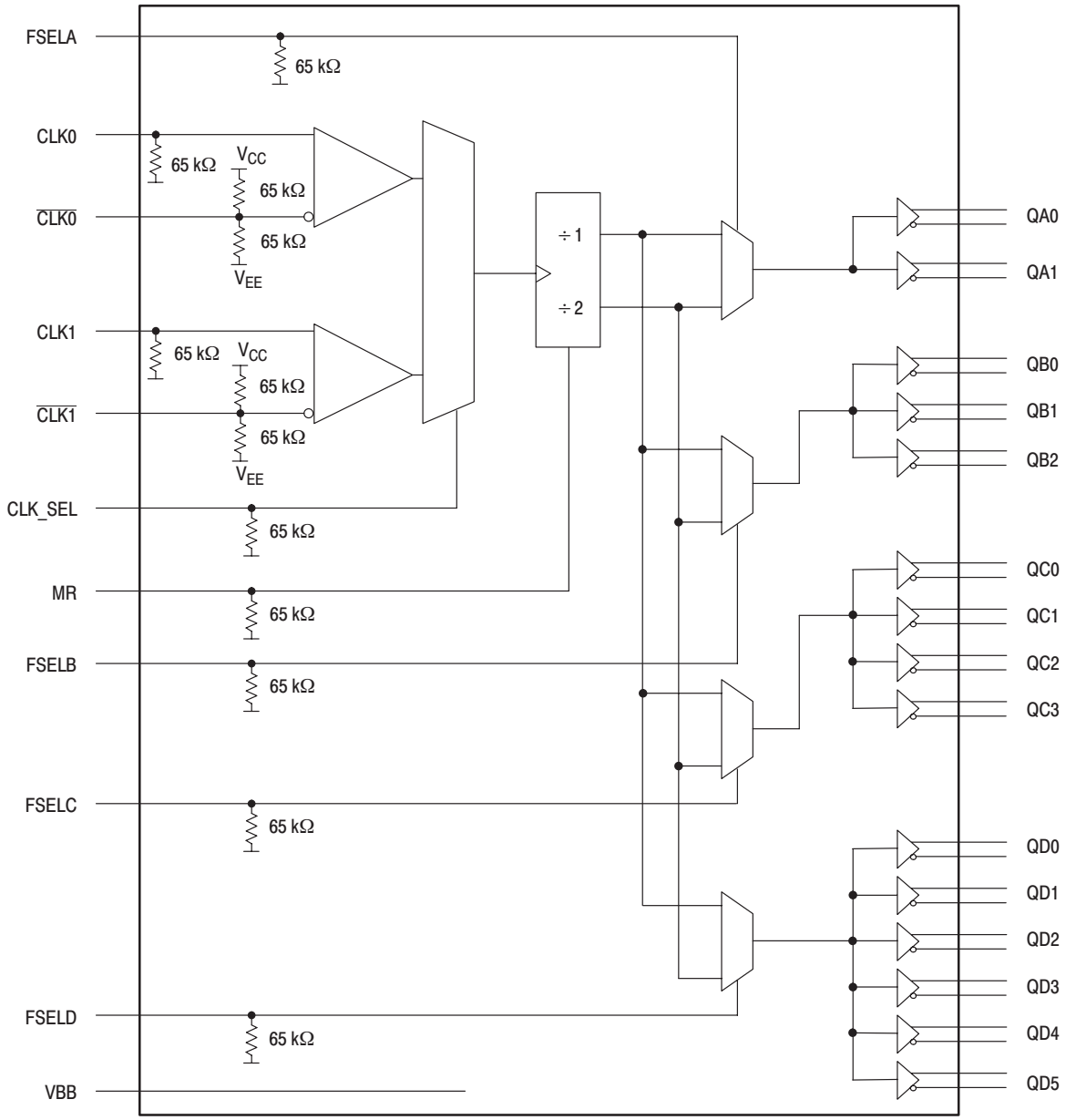

Figure 1. MC100EP222 Logic Diagram

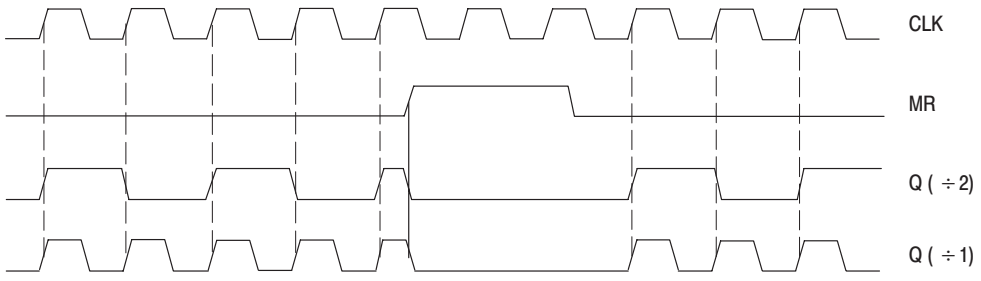

Figure 2. MC100EP222 Function Diagram

Figure 3. 52 Lead Package Pinout (Top View)

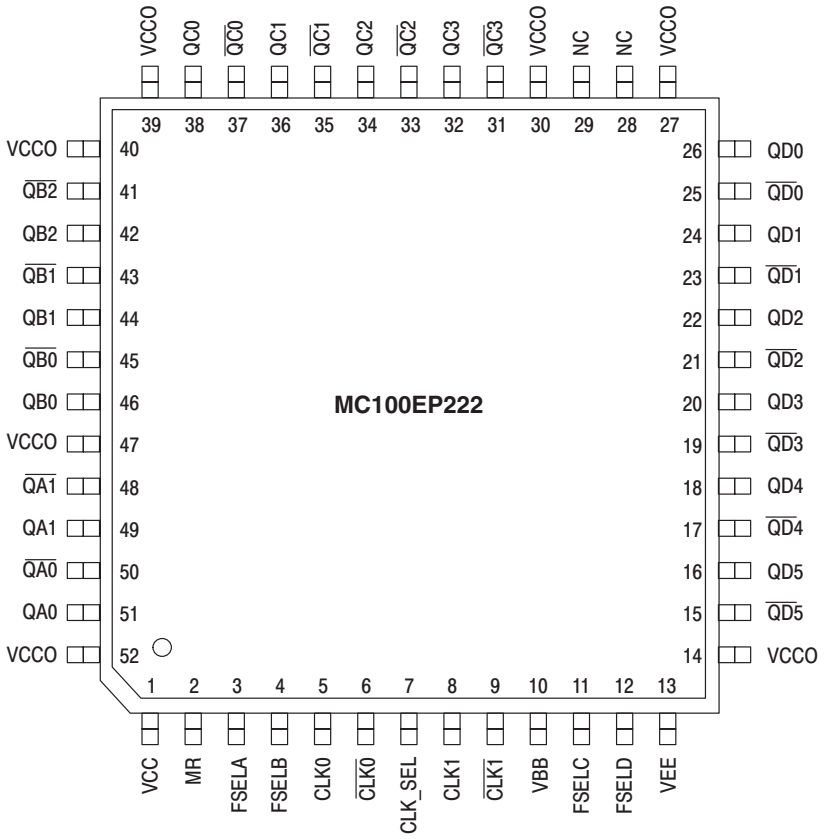

Table 1: FUNCTION TABLE

Control Pin	0	1
FSELA (asynchronous)	÷1	÷2
FSELB (asynchronous)	÷1	÷2
FSELC (asynchronous)	÷1	÷2
FSELD (asynchronous)	÷1	÷2
CLK_SEL (asynchronous)	CLK0	CLK1
MR (asynchronous)	Active	Reset

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Table 2: PIN CONFIGURATION

Pin	I/O	Type	Description
CLK0, $\overline{CLK0}$	Input	ECL/PECL	Differential reference clock signal input
CLK1, $\overline{CLK1}$	Input	ECL/PECL	Alternative differential reference clock signal input
CLK_SEL	Input	ECL/PECL	Clock input select
QAn, $\overline{QAn}$	Output	ECL/PECL	Bank A differential outputs
QBn, $\overline{QBn}$	Output	ECL/PECL	Bank B differential outputs
QCn, $\overline{QCn}$	Output	ECL/PECL	Bank C differential outputs
QDn, $\overline{QDn}$	Output	ECL/PECL	Bank D differential outputs
FSELA	Input	ECL/PECL	Selection of bank A output frequency
FSELB	Input	ECL/PECL	Selection of bank B output frequency
FSELC	Input	ECL/PECL	Selection of bank C output frequency
FSELD	Input	ECL/PECL	Selection of bank D output frequency
MR	Input	ECL/PECL	Reset
VBB	Output		DC bias output for single ended input operation
VEE[a]	Supply		Negative power supply
V_{CC}, V_{CCO}	Supply		Positive power supply. All V_{CC} and V_{CCO} pins must be connected to the positive power supply for correct DC and AC operation

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V).
In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V .
In both modes, the input and output levels are referrenced to the most positive supply.

Table 3: ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-65	125	°C	

a. Absolute maximum continuos ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		V_{CC} - 2[a]		V	
MM	ESD Protection (Machine model)	75			V	
HBM	ESD Protection (Human body model)	1500			V	
CDM	ESD Protection (Charged device model	500			V	
LU	Latch-up immunity	200			mA	
C_{IN}			4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient	See application information[b]				
θ_{JC}	Thermal resistance junction to case	See application information				

a. Output termination voltage V_{TT} = 0V for V_{CC}=2.5V operation is supported but the power consumption of the device will increase
b. Proper thermal management is critical for reliable system operation. This especially true for high-fanout and high drive capability products. Thermal package information and exposed pad land pattern design recommendations are available in the applications section of this datasheet. In addition, the means of calculating die power consumption, the corresponding die temperature and the relationsship to long-term reliability is addressed in the Motorola application note AN1545. Thermal modeling is recommended for the MC100EP222.

Table 5: PECL DC Characteristics (V_{CCO} = V_{CC} = 2.375 V to 3.8 V, V_{EE} = GND)

Symbol	Characteristics	T_A = -40°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
Clock input pairs CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (LVPECL differential signals)									
V_{PP}	Differential input voltage[a] V_{CC}=3.3 V V_{CC}=2.5 V	0.10 0.15		0.10 0.15		0.10 0.15		V V	
V_{CMR}	Differential cross point voltage[b] CLK0,CLK1	1.0	V_{CC}-0.4	1.0	V_{CC}-0.4	1.0	V_{CC}-0.4	V	
I_{IH}	Input Current		150		150		150	µA	V_{IN} = V_{CC} to V_{EE}
Control inputs (LVPECL single ended)									
V_{IH}	Input high voltage	V_{CC}-1.165	V_{CC}-0.880	V_{CC}-1.165	V_{CC}-0.880	V_{CC}-1.165	V_{CC}-0.880	V	
V_{IL}	Input low voltage	V_{CC}-1.810	V_{CC}-1.480	V_{CC}-1.810	V_{CC}-1.480	V_{CC}-1.810	V_{CC}-1.480	V	
I_{IH}	Input Current		150		150		150	µA	V_{IN} = V_{CC} to V_{EE}
LVPECL clock outputs (QAn, $\overline{QAn}$, QBn, $\overline{QBn}$, QCn, $\overline{QCn}$, QDn, $\overline{QDn}$)									
V_{OH}	Output High Voltage	V_{CC}-1.20	V_{CC}-0.82	V_{CC}-1.15	V_{CC}-0.82	V_{CC}-1.15	V_{CC}-0.82	V	I_{OH}= -30mA[c]
V_{OL}	Output Low Voltage	V_{CC}-1.90	V_{CC}-1.40	V_{CC}-1.90	V_{CC}-1.40	V_{CC}-1.9	V_{CC}-1.40	V	I_{OL}= -5mA[c]
Supply current and V_{BB}									
I_{EE}	Max. Supply Current		190		190		190	mA	V_{EE} pin
I_{CC}	Max. Supply Current[d]		675		675		675	mA	V_{CC} pins
V_{BB}	Output reference voltage[e] V_{CC}=3.3 V V_{CC}=2.5 V	V_{CC}-1.35 V_{CC}-1.35	V_{CC}-1.24 V_{CC}-1.24	V_{CC}-1.35 V_{CC}-1.35	V_{CC}-1.24 V_{CC}-1.22	V_{CC}-1.35 V_{CC}-1.35	V_{CC}-1.24 V_{CC}-1.22	V V	

a. V_{PP} is the minimum differential input voltage swing required to maintain device functionality.
b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
c. Equivalent to an output termination of 50Ω to V_{TT}.
d. I_{CC} includes current through the output resistors (all outputs terminated 50Ω to V_{TT}).
e. V_{BB} output can be used to bias the complementary input when the device is used with single ended clock signals. V_{BB} can sink max. 0.3 mA DC current.

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Table 6: ECL DC Characteristics (V_{CC} = V_{CCO} = GND, V_{EE} = -3.8 V to -2.375 V)

Symbol	Characteristics	T_A = -40°C		T_A = 25°C		T_A = 85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
Clock input pairs CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (ECL differential signals)									
V_{PP}	Differential input voltage[a] V_{EE}=-3.3 V V_{EE}=-2.5 V	0.10 0.15		0.10 0.15		0.10 0.15		V V	
V_{CMR}	Differential cross point voltage[b] CLK0,CLK1	V_{EE}+1.0	-0.4	V_{EE}+1.0	-0.4	V_{EE}+1.0	-0.4	V	
I_{IH}	Input Current		150		150		150	µA	V_{IN} = V_{EE} to V_{CC}
All inputs ECL single ended signals									
V_{IH}	Input high voltage	-1.165	-0.880	-1.165	-0.880	-1.165	-0.880	V	
V_{IL}	Input low voltage	-1.810	-1.480	-1.810	-1.480	-1.810	-1.480	V	
I_{IH}	Input Current		150		150		150	µA	V_{IN} = V_{EE} to V_{CC}
LVPECL clock outputs (Q0-19, $\overline{Q0\text{-}19}$)									
V_{OH}	Output High Voltage	-1.20	-0.82	-1.20	-0.82	-1.20	-0.82	V	I_{OH}= -30 mA[c]
V_{OL}	Output Low Voltage	-1.90	-1.40	-1.90	-1.40	-1.90	-1.40	V	I_{OL}= -5 mA[c]
Supply current and V_{BB}									
I_{EE}	Max. Supply Current		190		190		190	mA	V_{EE} pin
I_{CC}	Max. Supply Current[d]		750		750		750	mA	V_{CC} Pins
V_{BB}	Output reference voltage[e] V_{EE}=-3.3 V V_{EE}=-2.5 V	-1.35 -1.35	-1.24 -1.24	-1.35 -1.35	-1.24 -1.22	-1.35 -1.35	-1.24 -1.22	V V	

a. V_{PP} is the minimum differential input voltage swing required to maintain device functionality.
b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
c. Equivalent to an output termination of 50Ω to V_{TT}.
d. I_{CC} includes current through the output resistors (all outputs terminated 50Ω to V_{TT}).
e. V_{BB} output can be used to bias the complementary input when the device is used with single ended clock signals. V_{BB} can sink max. 0.3 mA DC current.

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Table 7: ECL AC Characteristics[a] (V_{CC} = V_{CCO} = 2.375 V to 3.8 V, V_{EE} = GND) or (V_{EE} = -3.8 V to -2.375 V, V_{CC} = V_{CCO} = GND)

Symbol	Characteristics	T_A = -40°C			T_A = 25°C			T_A = 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Clock input pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (PECL/ECL differential signals)												
V_{PP}	Differential input voltage[b] (peak-to-peak) CLK0, CLK1	0.5		1.0	0.5		1.0	0.5		1.0	V	
V_{CMR}	Differential cross point voltage[c]											
	PECL mode CLK0, CLK1	V_{EE}+1.0		-0.4	V_{EE}+1.0		-0.4	V_{EE}+1.0		-0.4	V	
	ECL mode CLK0, CLK1	1.0		V_{CC}-0.4	1.0		V_{CC}-0.4	1.0		V_{CC}-0.4	V	
f_{CLK}	Input Frequency	0		1.0	0		1.0	0		1.0	GHz	
PECL/ECL clock outputs (QAn, $\overline{QAn}$, QBn, $\overline{QBn}$, QCn, $\overline{QCn}$, QDn, $\overline{QDn}$)												
t_{PD}	Propagation Delay CLK_N to Qx	560	730	910	640	790	940	740	890	1040	ps	Diff.
	MR to Qx			TBD			TBD			TBD	ps	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) f_O < 100 MHz	450			550			550			mV	
	f_O < 0.5 GHz	400			500			500			mV	
	f_O < 1.0 GHz	375			400			400			mV	
$t_{sk(O)}$	Output-to-output skew within											Diff.
	- QA[0:1]			40			40			40	ps	
	- QB[0:2]			40			40			40	ps	
	- QC[0:3]			70			70			70	ps	
	- QD[0:5]			40			40			40	ps	
											ps	
	- QA_N, QB_N, QD_N (single freq.)			60			60			60	ps	
	- all outputs (single freq.)			120			120			120	ps	
	- QA_N, QB_N, QD_N (multiple freq.)			130			130			130	ps	
	- all outputs (multiple freq.)			150			150			150	ps	
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			350			300			300	ps	Diff.
$t_{JIT(CC)}$	Output cycle-to-cycle jitter (RMS)			TBD			TBD			TBD	ps	
DC_O	Output duty cycle	49.5	50	50.5	49.5	50	50.5	49.5	50	50.5	%	DC_{fref}= 50%
t_r, t_f	Output Rise/Fall Time	100		500	100		500	100		500	ps	20% to 80%

a. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
b. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
c. V_{CMR} (AC) is the crosspoint of the differential input signal. AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay and part-to-part skew.

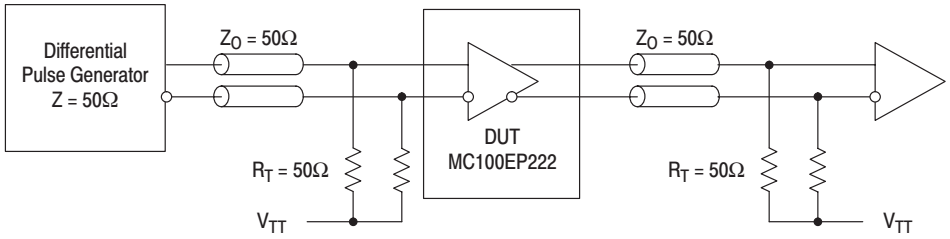

Figure 4. MC100EP222 AC test reference

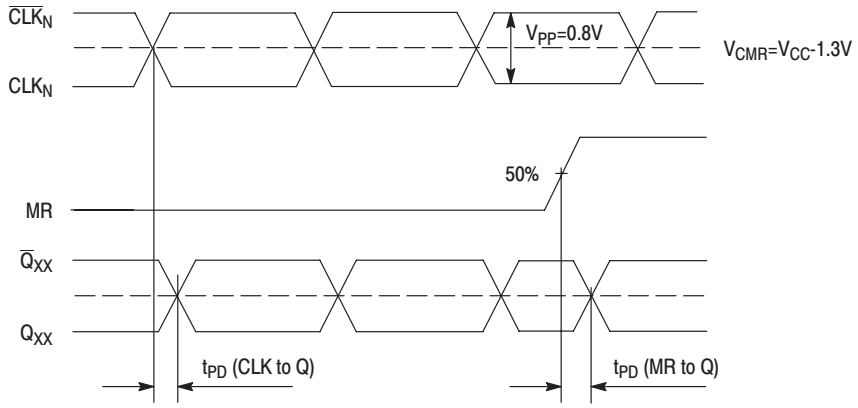

Figure 5. MC100EP222 t_{PD} / AC reference measurement waveform

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APPLICATIONS INFORMATION

Using the thermally enhanced package of the MC100EP222

The MC100EP222 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the leadframe is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100EP222 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100EP222. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is the absolute minimum requirement for MC100EP222 applications on multi-layer boards. The recommended thermal land design comprises a 5 x 5 thermal via array as shown in Figure 6 “Recommended thermal land pattern”, providing an efficient heat removal path.

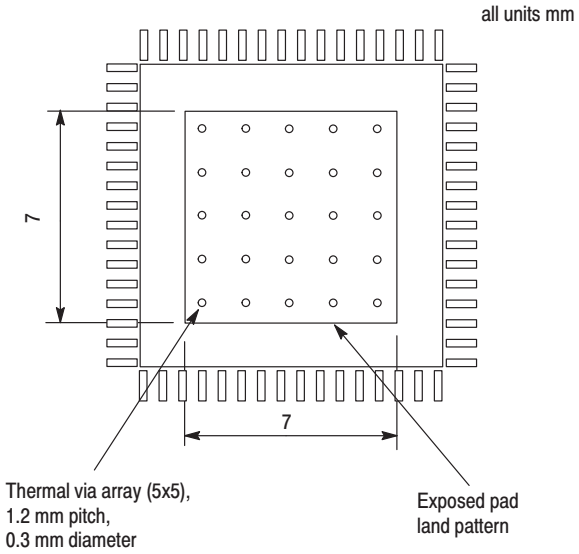

Figure 6. Recommended thermal land pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7 “Recommended solder mask openings” shows a recommend solder mask opening with respect to the recommended 5 x 5 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7 For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

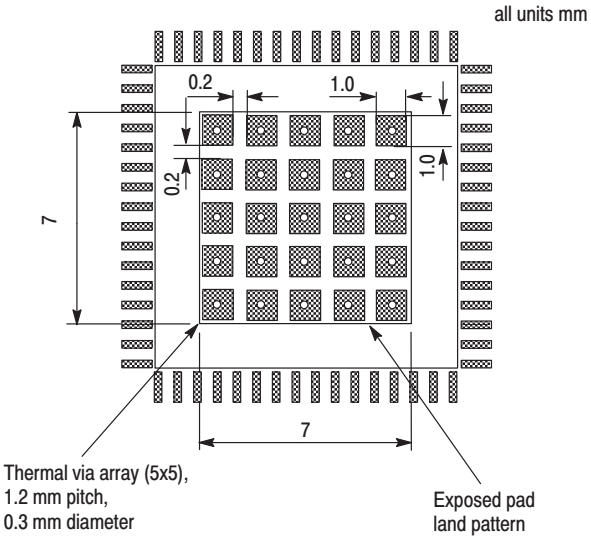

Figure 7. Recommended solder mask openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided. For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 8: Thermal Resistance[a]

Convection-LFPM	R_{THJA}[b] °C/W	R_{THJA}[c] °C/W	R_{THJC}[d] °C/W	R_{THJB}[e] °C/W
Natural	57.1	24.9	15.8	9.7
100	50.0	21.3		
200	46.9	20.0		
400	43.4	18.7		
800	38.6	16.9		

a. Thermal data pattern with a 3 x 3 thermal via array on 2S2P boards (based on empirical results)
b. Junction to ambient, single layer test board, per JESD51-6
c. Junction to ambient, four conductor layer test board (2S2P), per JES51-6
d. Junction to case, per MIL-SPEC 883E, method 1012.1
e. Junction to board, four conductor layer test board (2S2P) per JESD 51-8

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100EP222 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

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