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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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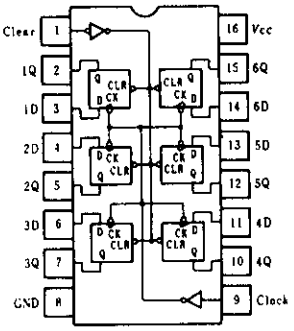
HD74LS174/HD74LS175 ●Hex/Quadruple D-type Flip-Flops (with clear)

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the HD74LS175 features complementary outputs from each flip-flops. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the outputs.

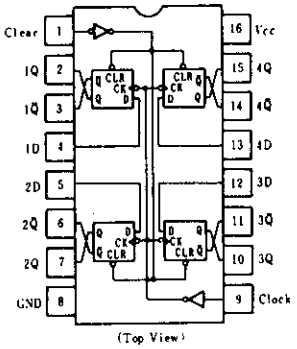
■PIN ARRANGEMENT

HD74LS174



(Top View)

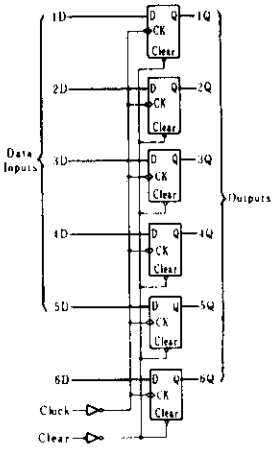
HD74LS175



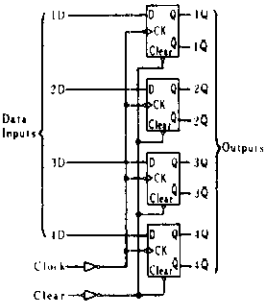
(Top View)

■BLOCK DIAGRAM

HD74LS174



HD74LS175



■FUNCTION TABLE

Inputs			Outputs	
Clear	Clock	D	Q	$\bar{Q}$
L	×	×	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	×	Q_0	$\bar{Q}_0$

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. Q_0; the level of Q before the indicated steady-state input conditions were established.
4. $\bar{Q}$ is applied to HD74LS175 only.

■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	max	Unit
Clock frequency		f_{clock}	0	30	MHz
Clock pulse width		$t_{w(CK)}$	20	–	ns
Clear pulse width		$t_{w(CLR)}$	20	–	ns
Setup time	Data input	$t_{su(data)}$	20	–	ns
	Clear inactive-state	$t_{su(CLR)}$	25	–	ns
Data hold time		$t_{h(data)}$	5	–	ns

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=8mA$	–	–	0.5	V
			$I_{OL}=4mA$	–	–	0.4	
Input current	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current**	I_{CC}	$V_{CC}=5.25V$	HD74LS174	–	16	26	mA
			HD74LS175	–	11	18	
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$

** With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary grounded, then 4.5V, is applied to clock.

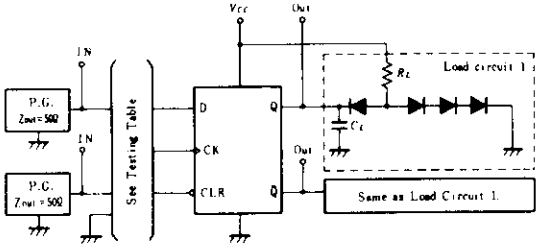
■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}	Clock	Q, Q*	$C_L=15pF$, $R_L=2k\Omega$	30	40	–	MHz
Propagation delay time	t_{PLH}	Clear	Q*		–	16	25	ns
	t_{PHL}		Q		–	23	35	
	t_{PLH}	Clock	Q, Q*		–	20	30	
	t_{PHL}	Clock	Q, Q*		–	21	30	

* HD74LS175 only

■TESTING METHOD

1) Test Circuit



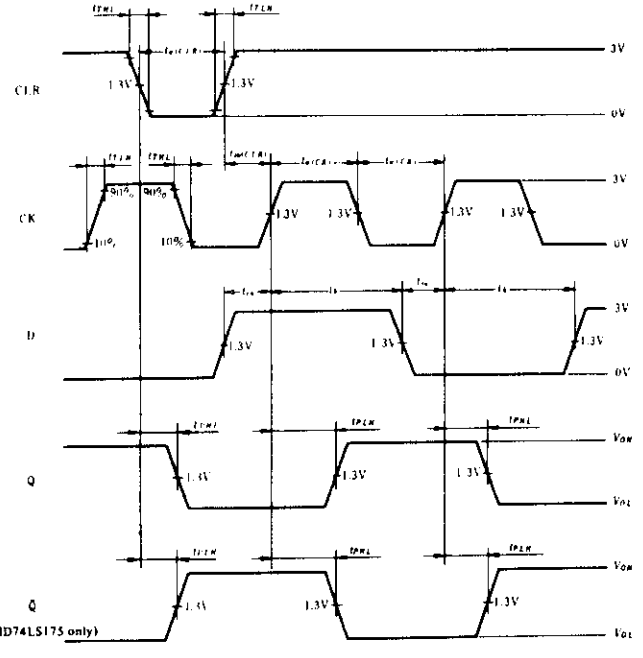
2) Testing Table

Item	From input to output	Inputs			Outputs	
		CLR	CK	D	Q	Q*
f_{max}	CK→Q, Q*	4.5V	IN	IN	OUT	OUT
t_{PLH}	CK→Q, Q*	4.5V	IN	IN		
t_{PHL}	CLR→Q, Q*	IN	IN	4.5V		

* HD74LS175 only

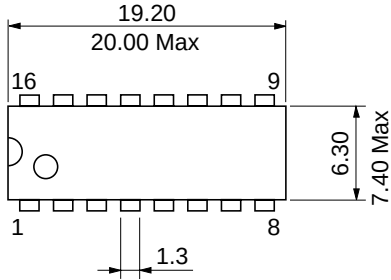
Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

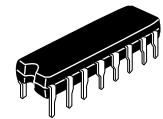
Waveform

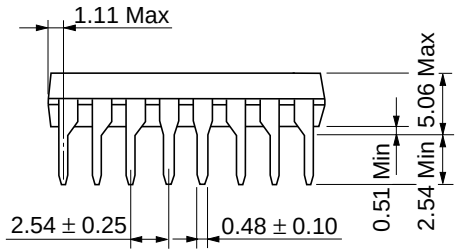


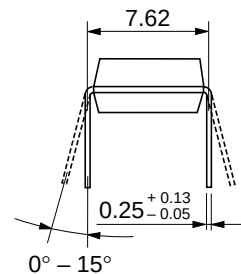
Notes) 1. Input pulse; $t_{TLH}\leqq 15ns$, $t_{THL}\leqq 6ns$, $PRR=1MHz$
and: for f_{max}, $t_{TLH}=t_{THL}\leqq 2.5ns$.

Unit: mm



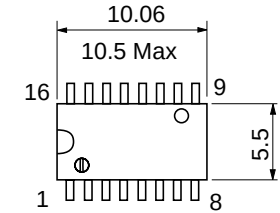


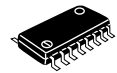


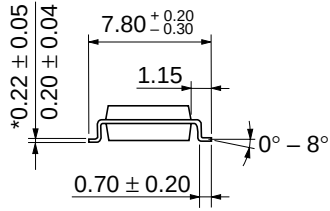


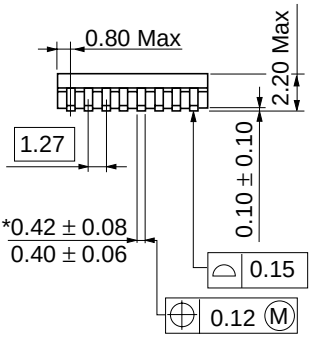
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm





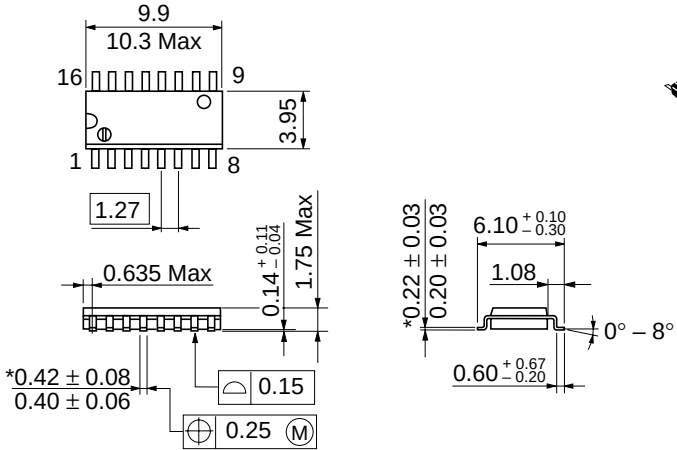


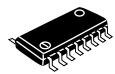


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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