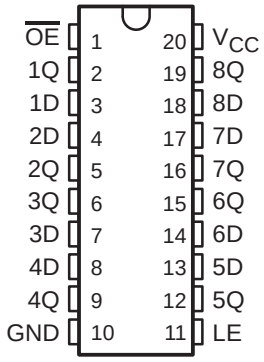
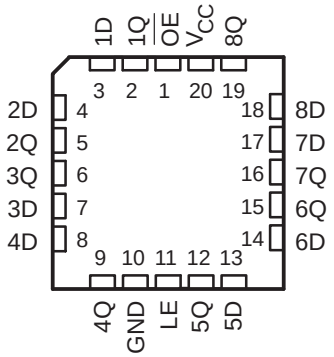
- **Eight Latches in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

**SN54F373 . . . J PACKAGE**
**SN74F373 . . . DB, DW, OR N PACKAGE**
**(TOP VIEW)**




**SN54F373 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ′F373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs will follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

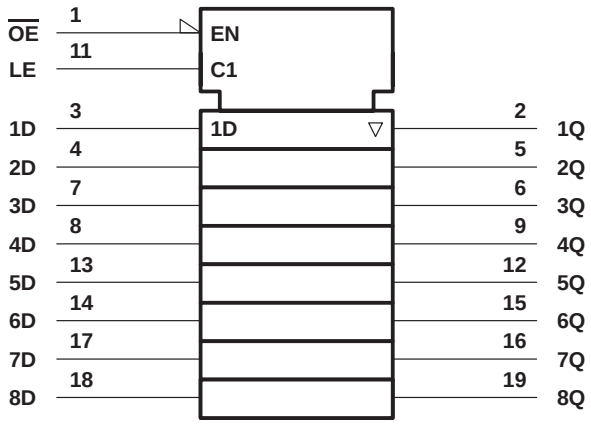
The SN74F373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F373 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**
**(each latch)**

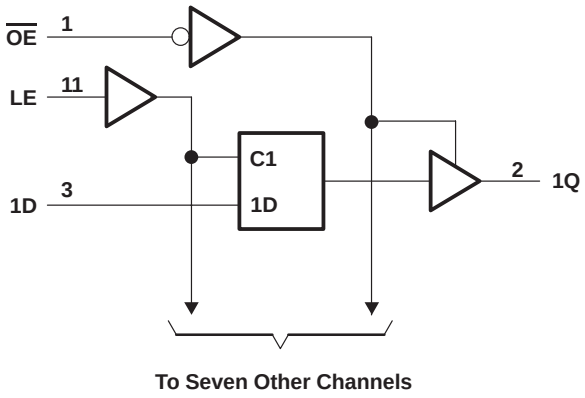
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –1.2 V to 7 V
Input current range . . . . . –30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state . . . . . –0.5 V to $V_{CC}$
Current into any output in the low state: SN54F373 . . . . . 40 mA
SN74F373 . . . . . 48 mA
Operating free-air temperature range: SN54F373 . . . . . –55°C to 125°C
SN74F373 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F373 | | | SN74F373 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | | | –18 | mA |
| $I_{OH}$ | High-level output current | | | – 3 | | | – 3 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F373 | | | SN74F373 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 1 mA | 2.5 | 3.4 | | 2.5 | 3.4 | | V |
| | | $I_{OH}$ = – 3 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | |
| | $V_{CC}$ = 4.75 V, | $I_{OH}$ = – 1 mA to –3 mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA | | 0.3 | 0.5 | | | | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 50 | | | 50 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –50 | | | –50 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.5 V | | | – 0.6 | | | – 0.6 | mA |
| $I_{OS}$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | –60 | | –150 | –60 | | –150 | mA |
| $I_{CCZ}$ | $V_{CC}$ = 5.5 V, | See Note 2 | | 38 | 55 | | 38 | 55 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: $I_{CCZ}$ is measured with $\overline{OE}$ at 4.5 V and all other inputs grounded.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | SN54F373 | | SN74F373 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | ′F373 | | | | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 6 | | 6 | | 6 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 2 | | 2 | | 2 | | ns |
| $t_h$ | Hold time, data after LE↓ | 3 | | 3 | | 3 | | ns |

## switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = 25°C | | | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | ′F373 | | | SN54F373 | | SN74F373 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | Q | 2.2 | 4.9 | 7 | 2.2 | 8.5 | 2.2 | 8 | ns |
| $t_{PHL}$ | | | 1.2 | 3.3 | 5 | 1.2 | 7 | 1.2 | 6 | |
| $t_{PLH}$ | LE | Q | 4.2 | 8.6 | 11.5 | 4.2 | 15 | 4.2 | 13 | ns |
| $t_{PHL}$ | | | 2.2 | 4.8 | 7 | 2.2 | 8.5 | 2.2 | 8 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | 1.2 | 4.6 | 11 | 1.2 | 13.5 | 1.2 | 12 | ns |
| $t_{PZL}$ | | | 1.2 | 5.2 | 7.5 | 1.2 | 10 | 1.2 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | 1.2 | 4.1 | 6.5 | 1.2 | 10 | 1.2 | 7.5 | ns |
| $t_{PLZ}$ | | | 1.2 | 3.4 | 6 | 1.2 | 7 | 1.2 | 6 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

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## SN74F373, Octal D-type transparent latches

DEVICE STATUS: **ACTIVE**

| PARAMETER NAME | SN54F373 | SN74F373 |
|---|---|---|
| Voltage Nodes (V) | 5 | 5 |
| Vcc range (V) | 4.5 to 5.5 | 4.5 to 5.5 |
| Input Level | TTL | TTL |
| Output Level | TTL | TTL |
| Output Drive (mA) | | -3/24 |
| No. of Outputs | 8 | 8 |
| th (ns) | | 3 |
| tpd max (ns) | | 8 |
| tsu (ns) | | 2 |
| Logic | True | True |

### FEATURES

Back to Top

- Eight Latches in a Single Package
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- Full Parallel Access for Loading
- Buffered Control Inputs
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### DESCRIPTION

Back to Top

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## TECHNICAL DOCUMENTS

Back to Top

To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

## DATASHEET

Back to Top

Full datasheet in Acrobat PDF: sn74f373.pdf (54 KB,Rev.A) (Updated: 10/01/1993)

## APPLICATION NOTES

Back to Top

View Application Notes for Digital Logic

- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)

## RELATED DOCUMENTS

Back to Top

View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

## PRICING/AVAILABILITY/PKG

Back to Top

| DEVICE INFORMATION | | | | | | | TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002 | | | REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ORDERABLE DEVICE | STATUS | PACKAGE TYPE\|PINS | TEMP (°C) | PRODUCT CONTENT | BUDGETARY PRICING QTY \| $US | STD PACK QTY | IN STOCK | IN PROGRESS QTY\|DATE | LEAD TIME | DISTRIBUTOR COMPANY\|REGION | IN STOCK | PURCHASE |
| SN74F373DBLE | OBSOLETE | SSOP (DB) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |
| SN74F373DBR | ACTIVE | SSOP (DB) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.27 | 2000 | N/A* | 2000 \| 20 Sep | 5 WKS | | | |
| | | | | | | | | 29 \| 25 Sep | | | | |
| | | | | | | | | 1573 \| 07 Oct | | | | |
| SN74F373DW | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.27 | 25 | N/A* | 1573 \| 04 Oct | 5 WKS | Avnet \| AMERICA | >1k | BUY NOW |
| | | | | | | | | 1000 \| 21 Oct | | | | |
| SN74F373DWR | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.27 | 2000 | 2000 | 1573 \| 04 Oct | 5 WKS | | | |
| SN74F373N | ACTIVE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.27 | 20 | 330 | 1573 \| 07 Oct | 5 WKS | Avnet \| AMERICA | >1k | BUY NOW |

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74F373N3 | OBSOLETE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |
| SN74F373NSR | ACTIVE | SOP (NS) \| 20 | | View Contents | 1KU \| 0.48 | 2000 | N/A* | 7804 \| 25 Sep | 5 WKS | | | |
| | | | | | | | | 1573 \| 14 Oct | | | | |

**Table Data Updated on: 9/26/2002**