Signetics

Military Logic Products

54LS373, 54LS374, 54S373, 54S374

Latches/Flip-Flops

'373 Octal Transparent Latch with 3-State Outputs
'374 Octal D Flip-Flop with 3-State Outputs
Product Specification

FEATURES

- **8-bit transparent latch — '373**
- **8-bit positive, edge-triggered register — '374**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

DESCRIPTION

The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

ORDERING INFORMATION

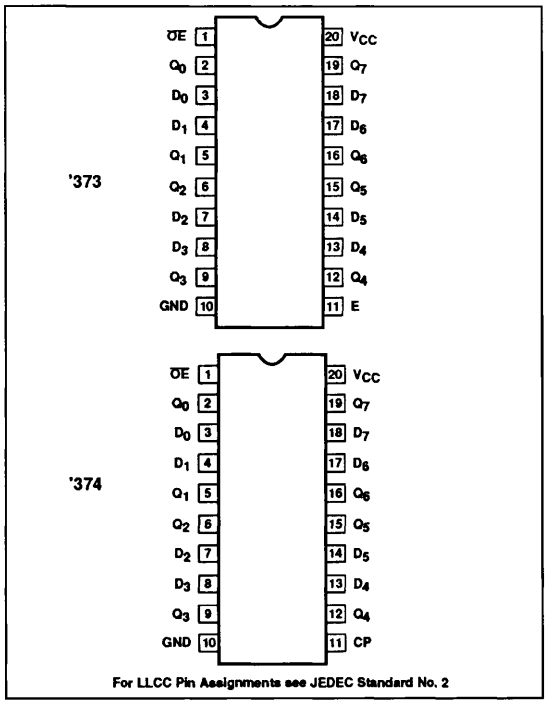
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54LS373/BRA 54S373/BRA 54LS374/BRA 54S374/BRA
20-Pin Ceramic FlatPack	54LS373/BSA 54S373/BSA 54LS374/BSA 54S374/BSA
20-Pin Ceramic LLCC	54LS373/B2A 54S373/B2A 54LS374/B2A 54S374/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S	54LS
All	Inputs	1SUL	1LSUL
All	Outputs	10SUL	30LSUL

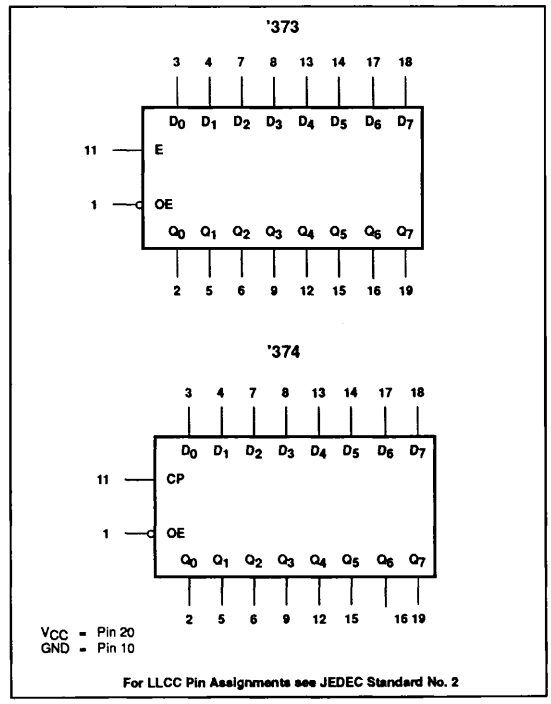
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL} and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data present one setup time before the High-to-Low enable transition. The enable gate has hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

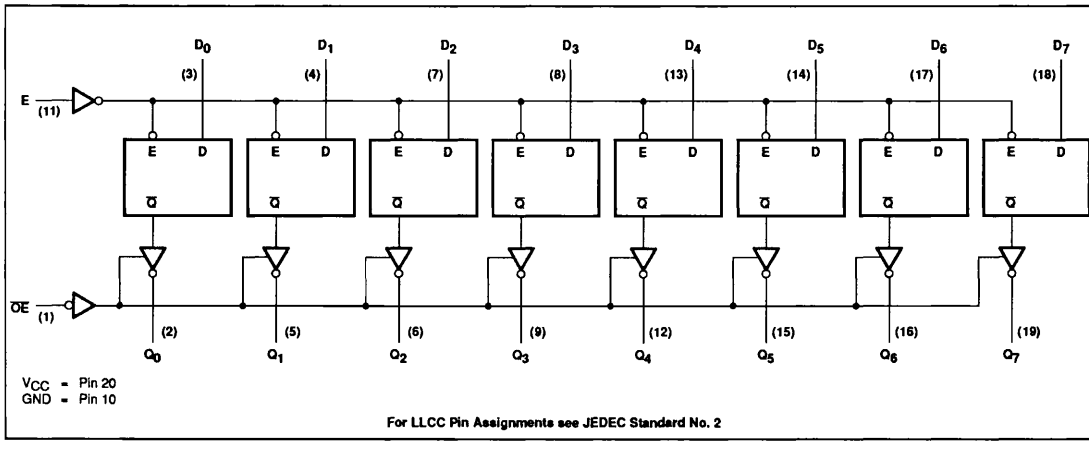
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

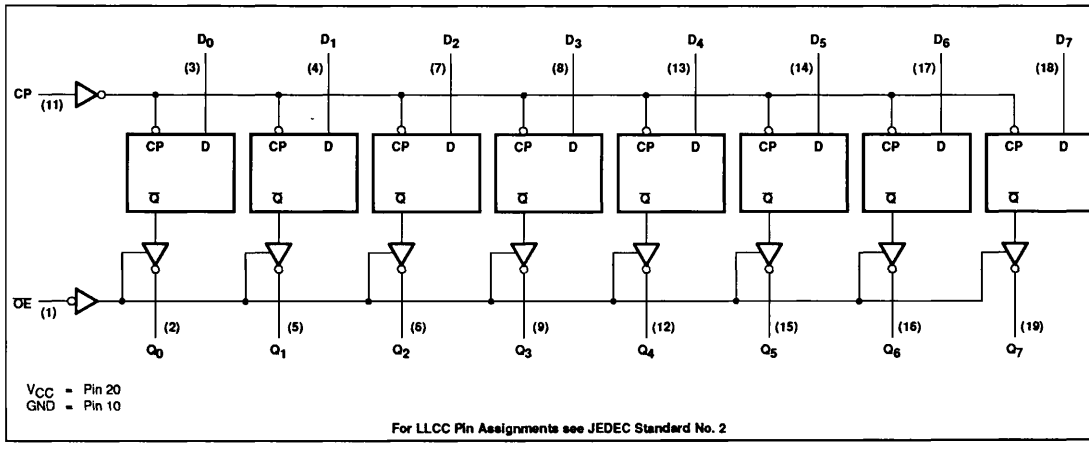
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC DIAGRAM, ' 374



For LLCC Pin Assignments see JEDEC Standard No. 2

MODE SELECT — FUNCTION TABLE '373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0 - Q_7
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

MODE SELECT — FUNCTION TABLE '374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 - Q_7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition or High-to-Low $\overline{OE}$ transition
L = Low voltage level
X = Don't care
l = Low voltage level one setup time prior to Low-to-High clock transition or High-to-Low $\overline{OE}$ transition
(Z) = High impedance "off" state
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.7			+0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-1.0			-2.0	mA
I_{OL}	Low-level output current			12			20	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54LS373, 374			54S373, 374			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.2	V
I_{IZH}	Off-state output current,	V_{CC} = Max, V_{IH} = Min	V_O = 2.7V			20				µA
	High-level voltage applied		V_O = 2.4V						50	µA
I_{IZL}	Off-state output current,	V_{CC} = Max, V_{IH} = Min	V_O = 0.4V			-20				µA
	Low-level voltage applied		V_O = 0.5V						-50	µA
I_{IH2}	Input current at	V_{CC} = Max	V_I = 7.0V			0.1				mA
	maximum input voltage		V_I = 5.5V						1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20			50	µA
I_{IL}	Low level input current	V_{CC} = Max	V_I = 0.4V			-400				µA
			V_I = 0.5V						0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-30		-130	-40		-100	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCZ} $\overline{OE}$ ≥4.0V 'LS373		24	40				mA
			I_{CCL} $\overline{OE}$ = 0V 'S373					105	160	mA
			I_{CCZ} $\overline{OE}$ ≥4.0V 'LS374		27	40				mA
			I_{CCL} All inputs grounded 'S374					102	140	mA
			I_{CCZ} CP, $\overline{OE}$ ≥4.0V 'S374 D inputs = GND					131	180	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54S373, 374 C_L = 15pF		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, '374	75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch enable to output	Waveform 1, '373		14 18	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, '373		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, '374		15 17	ns ns
t_{PZH}	Enable time to High level	Waveform 2		15	ns
t_{PZL}	Enable time to Low level	Waveform 3, '373, '374		18 18	ns ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 5pF[4]		9	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 5pF[4]		12	ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 50pF		14	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 50pF		13.5	ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS373, 374 C_L = 50pF		54S373, 374[5] C_L = 50pF		UNIT
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, '374	35		75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch enable to output	Waveform 1, '373		30 30		16.5 20.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, '373		18 18		14.5 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, '374		28 28		17.5 19.5	ns ns
t_{PZH}	Enable time to High level	Waveform 2		28		17.5	ns
t_{PZL}	Enable time to Low level	Waveform 3, '373, '374		36 28		20.5 20.5	ns ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 5pF[4]		20		9	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 5pF[4]		25		12	ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 50pF		36		14	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 50pF		27		13.5	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_{W(H)}$ $t_{W(L)}$	Latch enable pulse width	Waveform 1, '373	15 15		6 7.3		ns ns
t_s	Setup time, data to latch enable	Waveform 5, '373	5		0		ns
t_h	Hold time, data to latch enable	Waveform 5, '373	20		10		ns
$t_{W(H)}$ $t_{W(L)}$	Clock pulse width	Waveform 6, '374	15 15		6 7.3		ns ns
t_s	Setup time, data to clock	Waveform 7, '374	20		5		ns
t_h	Hold time, data to clock	Waveform 7, '374	0		2		ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

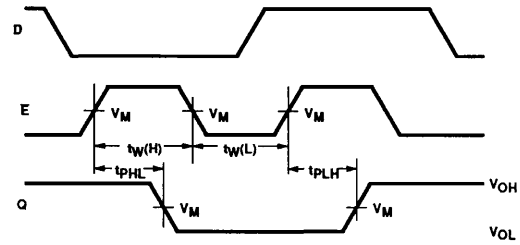
SYMBOL	PARAMETER	TEST CONDITIONS	54LS373, 374 C_L = 50pF		54S373, 374[5] C_L = 50pF		UNIT
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, '374	26		75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch enable to output	Waveform 1, '373		39 39		21 27	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, '373		23 23		16 16	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, '374		36 36		23 25	ns ns
t_{PZH}	Enable time to High level	Waveform 2		36		23	ns
t_{PZL}	Enable time to Low level	Waveform 3, '373, '374		47 36		27 27	ns ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 5pF[4]		25		12	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 5pF[4]		33		16	ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 50pF		47		18.5	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 50pF		35		18	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

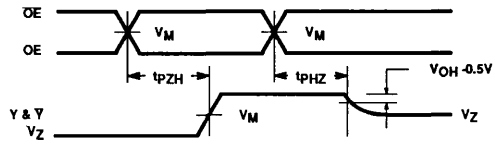
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_W(H)$ $t_W(L)$	Latch enable pulse width	Waveform 1, '373	15 15		6 7.3		ns ns
t_s	Setup time, data to latch enable	Waveform 5, '373	5		0		ns
t_h	Hold time, data to latch enable	Waveform 5, '373	20		15		ns
$t_W(H)$ $t_W(L)$	Clock pulse width	Waveform 6, '374	15 15		6 7.3		ns ns
t_s	Setup time, data to clock	Waveform 7, '374	20		5		ns
t_h	Hold time, data to clock	Waveform 7, '374	5		2		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Guaranteed by the 50pF limits, but not tested.
5. These parameters are guaranteed, but not tested.

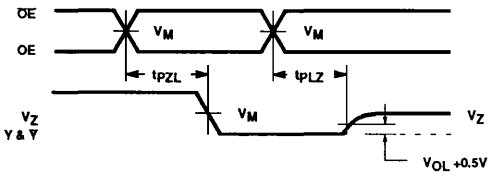
AC WAVEFORMS



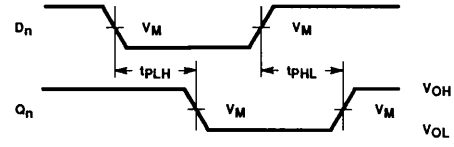
Waveform 1. Latch Enable to Output Delays and Latch Enable Pulse Width



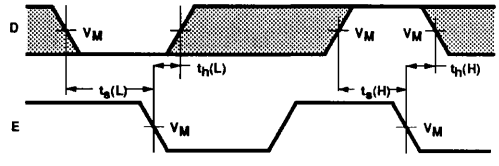
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



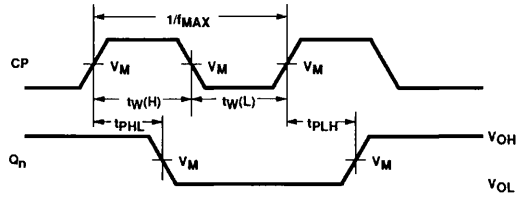
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level



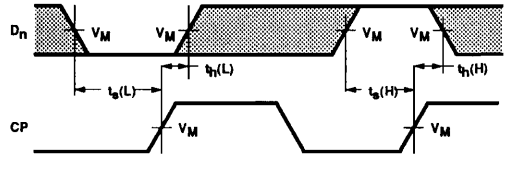
Waveform 4. Propagation Delay Data to Q Outputs



Waveform 5. Data Setup and Hold Times



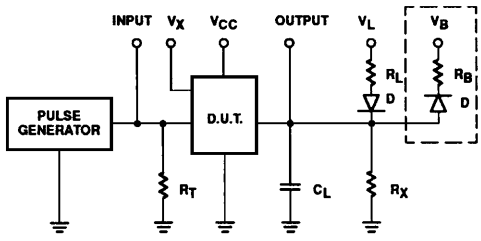
Waveform 6. Clock to Output Delays and Pulse Width



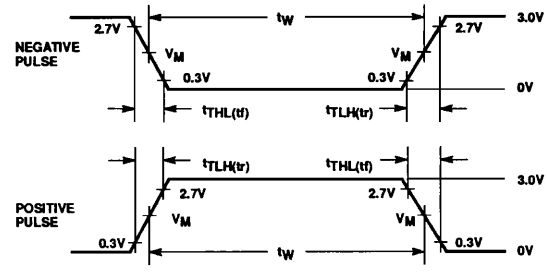
Waveform 7. Data Setup and Hold Times

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V
54SXXX	1.5V	0.7V	2.0V	1.65V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	82Ω	560Ω	2.5V	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.